

## 74ACQ543• 74ACTQ543

### Quiet Series™ Octal Registered Transceiver with 3-STATE Outputs

#### General Description

The ACQ/ACTQ543 is a non-inverting octal transceiver containing two sets of D-type registers for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow.

The ACQ/ACTQ utilizes Fairchild Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### Features

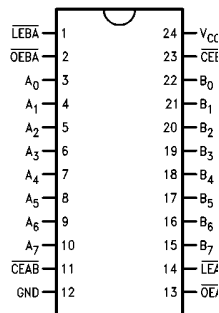
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- 8-bit octal latched transceiver
- Separate controls for data flow in each direction
- Back-to-back registers for storage
- Outputs source/sink 24 mA
- 300 mil slim PDIP/SOIC

#### Ordering Code:

Order Number	Package Number	Package Description
74ACQ543SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74ACQ543SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74ACTQ543SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74ACTQ543QSC	MQA24	24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
74ACTQ543SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the order code.

#### Connection Diagram

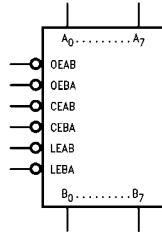


#### Pin Descriptions

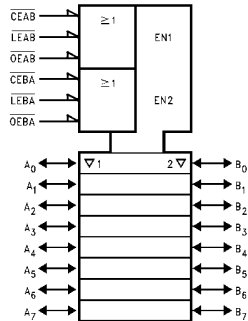
Pin Names	Description
OEAB	A-to-B Output Enable Input (Active LOW)
OEBA	B-to-A Output Enable Input (Active LOW)
CEAB	A-to-B Enable Input (Active LOW)
CEBA	B-to-A Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input (Active LOW)
LEBA	B-to-A Latch Enable Input (Active LOW)
A <sub>0</sub> -A <sub>7</sub>	A-to-B Data Inputs or B-to-A 3-STATE Outputs
B <sub>0</sub> -B <sub>7</sub>	B-to-A Data Inputs or A-to-B 3-STATE Outputs

FACT™, Quiet Series™, FACT Quiet Series™ and GTO™ are trademarks of Fairchild Semiconductor Corporation.

### Logic Symbols



IEEE/IEC



### Functional Description

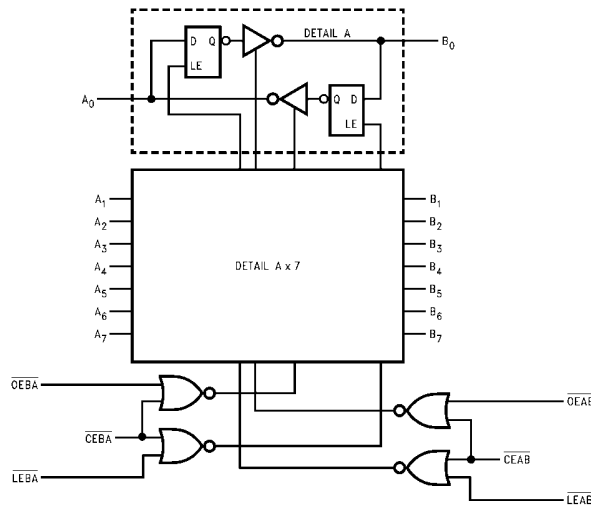
The ACQ/ACTQ543 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ( $\overline{CEAB}$ ) input must be LOW in order to enter data from  $A_0$ - $A_7$  or take data from  $B_0$ - $B_7$ , as indicated in the Data I/O Control Table. With  $\overline{CEAB}$  LOW, a LOW signal on the A-to-B Latch Enable ( $\overline{LEAB}$ ) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the  $\overline{LEAB}$  signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With  $\overline{CEAB}$  and  $\overline{OEAB}$  both LOW, the 3-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the  $\overline{CEBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$  inputs

### Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 A-to-B data flow shown; B-to-A flow control is the same, except using  $\overline{CEBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current	
per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-up Source or	
Sink Current	$\pm 300$ mA
Junction Temperature ( $T_J$ )	
PDIP	140°C

**Recommended Operating Conditions**

Supply Voltage $V_{CC}$	
ACQ	2.0V to 6.0V
ACTQ	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
ACQ Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate $\Delta V/\Delta t$	
ACTQ Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics for ACQ**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
$V_{IL}$	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
$V_{OH}$	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12$ mA $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 2)	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
$V_{OL}$	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 2)	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
$I_{IN}$ (Note 4)	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\mu A$	$V_I = V_{CC}$ , GND	
$I_{OLD}$	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max	
$I_{OHD}$	Output Current (Note 3)	5.5			-75	mA	$V_{OHD} = 3.85V$ Min	
$I_{CC}$ (Note 4)	Maximum Quiescent Supply Current	5.5		8.0	80.0	$\mu A$	$V_{IN} = V_{CC}$ or GND	
$I_{OZT}$	Maximum I/O Leakage Current	5.5		$\pm 0.6$	$\pm 6.0$	$\mu A$	$V_I$ (OE) = $V_{IL}$ , $V_{IH}$ $V_I = V_{CC}$ , GND $V_O = V_{CC}$ , GND	

**DC Electrical Characteristics for ACQ** (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V <sub>OLP</sub>	Quiet Output	5.0	1.1	1.5		V	Figures 1, 2 (Note 5)(Note 6)
	Maximum Dynamic V <sub>OL</sub>						
V <sub>OLV</sub>	Quiet Output	5.0	-0.6	-1.2		V	Figures 1, 2 (Note 5)(Note 6)
	Minimum Dynamic V <sub>OL</sub>						
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage	5.0	3.1	3.5		V	(Note 5)(Note 7)
V <sub>ILD</sub>	Maximum LOW Level	5.0	1.9	1.5		V	(Note 5)(Note 7)
	Dynamic Input Voltage						

**Note 2:** Maximum of 8 outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:** I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

**Note 5:** Plastic DIP package.

**Note 6:** Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

**Note 7:** Max number of Data Inputs (n) switching. (n-1) Inputs switching 0V to 5V (ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

**DC Electrical Characteristics for ACTQ**

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
	Input Voltage	5.5	1.5	2.0	2.0		
V <sub>IL</sub>	Maximum LOW Level	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
	Input Voltage	5.5	1.5	0.8	0.8		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	I <sub>OUT</sub> = -50 μA
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA (Note 8)
		5.5		4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I <sub>OUT</sub> = 50 μA
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA (Note 8)
		5.5		0.36	0.44		
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>OZT</sub>	Maximum I/O Leakage Current	5.5		± 0.6	6.0	μA	V <sub>(OE)</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> , GND
I <sub>CC1</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	Minimum Dynamic	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Output Current (Note 9)	5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
V <sub>OLP</sub>	Quiet Output	5.0	1.1	1.5		V	Figures 1, 2 (Note 10)(Note 11)
	Maximum Dynamic V <sub>OL</sub>						
V <sub>OLV</sub>	Quiet Output	5.0	-0.6	-1.2		V	Figures 1, 2 (Note 10)(Note 11)
	Minimum Dynamic V <sub>OL</sub>						
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage	5.0	1.9	2.2		V	(Note 10)(Note 12)
V <sub>ILD</sub>	Maximum LOW Level Dynamic Input Voltage	5.0	1.2	0.8		V	(Note 10)(Note 12)

**Note 8:** Maximum of 8 outputs loaded; thresholds on input associated with output under test.

**Note 9:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 10:** DIP package

**Note 11:** Max number of outputs defined as (n). (n-1) Data Inputs are driven 0V to 3V, one output @ GND.

**Note 12:** Max number of Data Inputs (n) switching. (n-1) Inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

AC Electrical Characteristics for AC								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 13)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	3.3	1.5	8.0	11.0	1.5	11.5	ns
t <sub>PHL</sub>	Transparent Mode A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	5.0	1.5	5.0	7.0	1.5	7.5	
t <sub>PLH</sub>	Propagation Delay	3.3	1.5	9.0	12.5	1.5	13.0	ns
t <sub>PHL</sub>	$\overline{\text{LEBA}}$ , $\overline{\text{LEAB}}$ to A <sub>n</sub> , B <sub>n</sub>	5.0	1.5	6.0	8.0	1.5	8.5	
t <sub>PZH</sub>	Output Enable Time	3.3	1.5	10.5	15.0	1.5	15.5	ns
t <sub>PZL</sub>	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to A <sub>n</sub> or B <sub>n</sub> $\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$ to A <sub>n</sub> or B <sub>n</sub>							
t <sub>PHZ</sub>	Output Disable Time	3.3	1.0	8.0	11.0	1.0	11.5	ns
t <sub>PLZ</sub>	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to A <sub>n</sub> or B <sub>n</sub> $\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$ to A <sub>n</sub> or B <sub>n</sub>							
t <sub>OSSL</sub>	Output to Output	3.3		1.0	1.5		1.5	ns
t <sub>OSLH</sub>	Skew (Note 14)	5.0		0.5	1.0		1.0	
<p><b>Note 13:</b> Voltage Range 5.0 is 5.0V ± 0.5V Voltage Range 3.3 is 3.3V ± 0.3V</p> <p><b>Note 14:</b> Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design. Not tested.</p>								
AC Operating Requirements for AC								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 15)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units	
			Typ	Guaranteed Minimum				
t <sub>S</sub>	Setup Time, HIGH or LOW A <sub>n</sub> or B <sub>n</sub> to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$	3.3 5.0		3.0	3.0		ns	
t <sub>H</sub>	Hold Time, HIGH or LOW A <sub>n</sub> or B <sub>n</sub> to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$	3.3 5.0		1.5	1.5		ns	
t <sub>W</sub>	Latch Enable Pulse Width, LOW	3.3 5.0		4.0	4.0		ns	
<p><b>Note 15:</b> Voltage Range 5.0 is 5.0V ± 0.5V Voltage Range 3.3 is 3.0V ± 0.3V</p>								

AC Electrical Characteristics for ACTQ								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 16)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Transparent Mode A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	5.0	1.5	5.5	7.5	1.5	8.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEBA, LEAB to A <sub>n</sub> , B <sub>n</sub>	5.0	1.5	6.5	8.5	1.5	9.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEBA or OEAB to A <sub>n</sub> or B <sub>n</sub> CEBA or CEAB to A <sub>n</sub> or B <sub>n</sub>	5.0	1.5	8.0	10.0	1.5	10.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEBA or OEAB to A <sub>n</sub> or B <sub>n</sub> CEBA or CEAB to A <sub>n</sub> or B <sub>n</sub>	5.0	1.0	5.5	7.5	1.0	8.0	ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output to Output Skew (Note 17)	5.0		0.5	1.0		1.0	ns
<p><b>Note 16:</b> Voltage Range 5.0 is 5.0V ± 0.5V</p> <p><b>Note 17:</b> Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design. Not tested.</p>								
AC Operating Requirements for ACTQ								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 18)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units	
			Typ	Guaranteed Minimum				
t <sub>S</sub>	Setup Time, HIGH or LOW A <sub>n</sub> or B <sub>n</sub> to LEBA or LEAB	5.0		3.0	3.0		ns	
t <sub>S</sub>	Hold Time, HIGH or LOW A <sub>n</sub> or B <sub>n</sub> to LEBA or LEAB	5.0		1.5	1.5		ns	
t <sub>W</sub>	Latch Enable Pulse Width, LOW	5.0		4.0	4.0		ns	
<p><b>Note 18:</b> Voltage Range 5.0 is 5.0V ± 0.5V</p>								
Capacitance								
Symbol	Parameter	Typ	Units	Conditions				
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN				
C <sub>PD</sub>	Power Dissipation Capacitance	70.0	pF	V <sub>CC</sub> = 5.0V				

## FACT Noise Characteristics

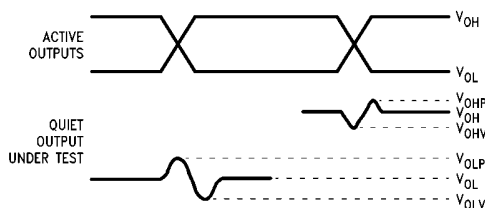
The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

### Equipment:

- Hewlett Packard Model 8180A Word Generator
- PC-163A Test Fixture
- Tektronics Model 7854 Oscilloscope

### Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.



**FIGURE 1. Quiet Output Noise Voltage Waveforms**

**Note 19:**  $V_{OHV}$  and  $V_{OLP}$  are measured with respect to ground reference.

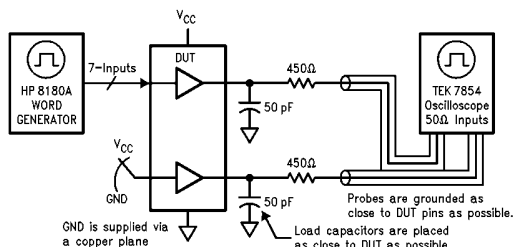
**Note 20:** Input pulses have the following characteristics:  $f = 1$  MHz,  $t_r = 3$  ns,  $t_f = 3$  ns, skew  $< 150$  ps.

$V_{OLP}/V_{OLV}$  and  $V_{OHP}/V_{OHV}$ :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure  $V_{OLP}$  and  $V_{OLV}$  on the quiet output during the worst case transition for active and enable. Measure  $V_{OHP}$  and  $V_{OHV}$  on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

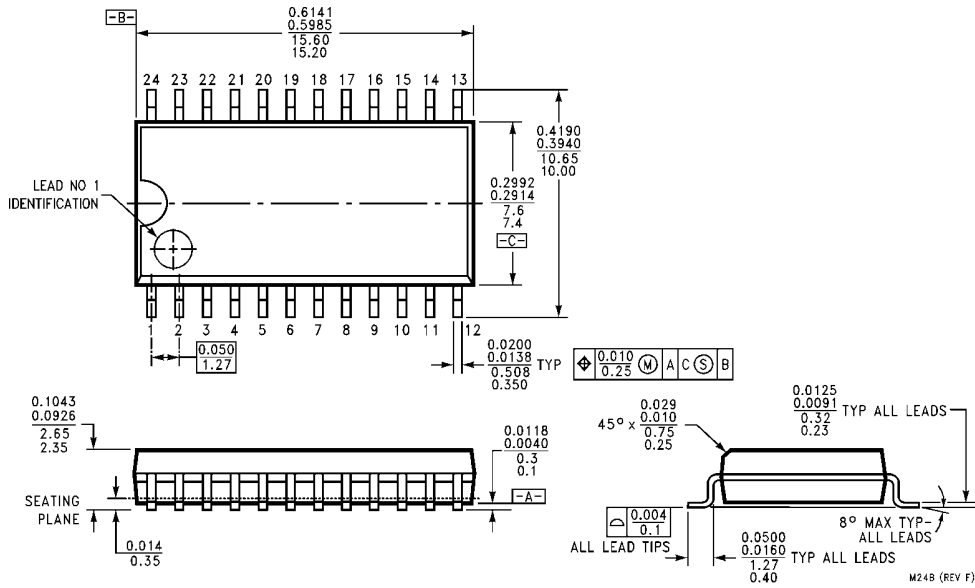
$V_{ILD}$  and  $V_{IHD}$ :

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level,  $V_{IL}$ , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input LOW voltage level at which oscillation occurs is defined as  $V_{ILD}$ .
- Next decrease the input HIGH voltage level,  $V_{IH}$ , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input HIGH voltage level at which oscillation occurs is defined as  $V_{IHD}$ .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability on the measurements.

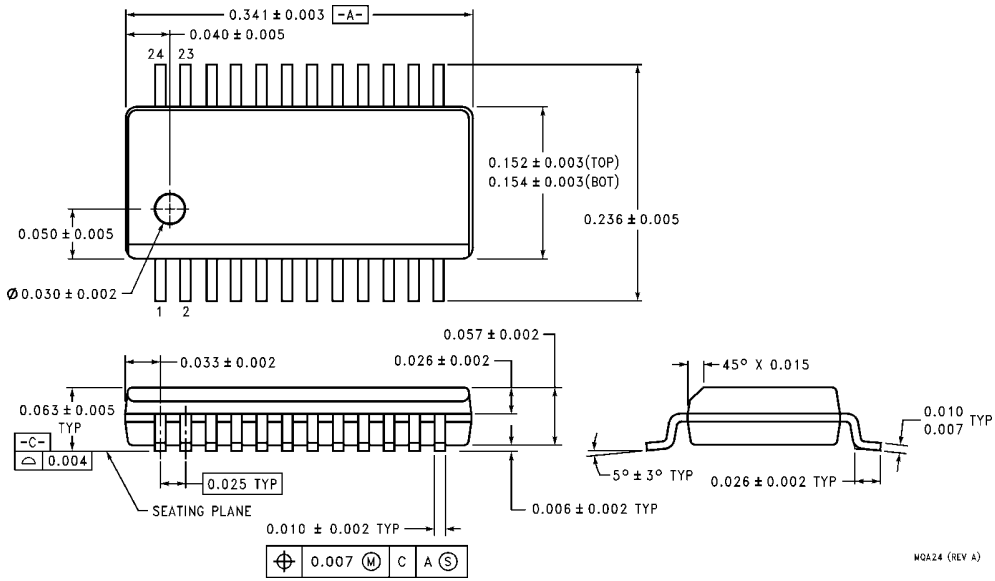


**FIGURE 2. Simultaneous Switching Test Circuit**

**Physical Dimensions** inches (millimeters) unless otherwise noted

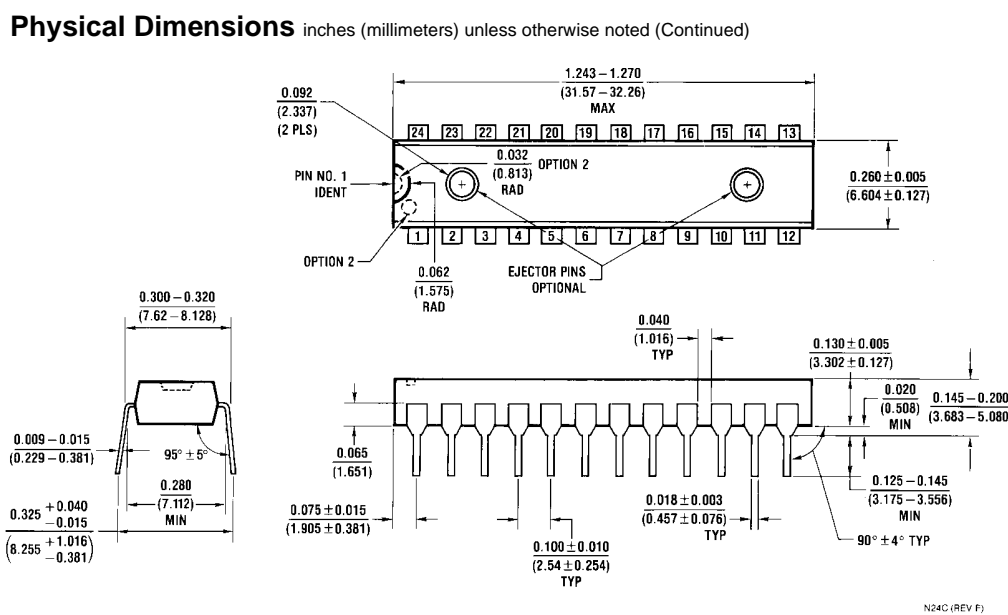


**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M24B**



**24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide Package Number MQA24**





**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N24C**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)