

April 1988 Revised July 1999

74F132

Quad 2-Input NAND Schmitt Trigger

General Description

The F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt Trigger followed by level shifting circuitry and a standard FAST™ output struc-

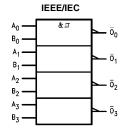
ture. The Schmitt Trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800 mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

Ordering Code:

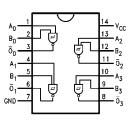
Order Number	Package Number	Package Description				
74F132SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow				
74F132SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide				
74F132PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide				

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Unit Loading/Fan Out

1	Dia Nama	D	U.L.	Input I _{IH} /I _{IL}		
	Pin Names	Description	HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}		
	A _n , B _n	Inputs		20 μA/-0.6 mA		
	\overline{O}_n	Outputs	50/33.3	-1 mA/20 mA		

Function Table

Inputs		Outputs		
Α	В	0		
L	L	Н		
L	Н	Н		
Н	L	Н		
Н	Н	L		

H = HIGH Voltage Level L = LOW Voltage Level

FAST® is a registered trademark of Fairchild Semiconductor Corporation

Absolute Maximum Ratings(Note 1)

-65°C to +150°C

Storage Temperature Ambient Temperature under Bias $-55^{\circ}C$ to $+125^{\circ}C$ Junction Temperature under Bias -55°C to +150°C

V_{CC} Pin Potential to Ground Pin -0.5V to +7.0V Input Voltage (Note 2) -0.5V to +7.0V

Input Current (Note 2) $-30\ \text{mA}$ to $+5.0\ \text{mA}$

Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)

Standard Output -0.5V to $V_{\mbox{\footnotesize CC}}$ 3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA) 4000V

ESD Last Passing Voltage (Min)

Recommended Operating Conditions

Free Air Ambient Temperature 0°C to $+70^{\circ}\text{C}$ Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

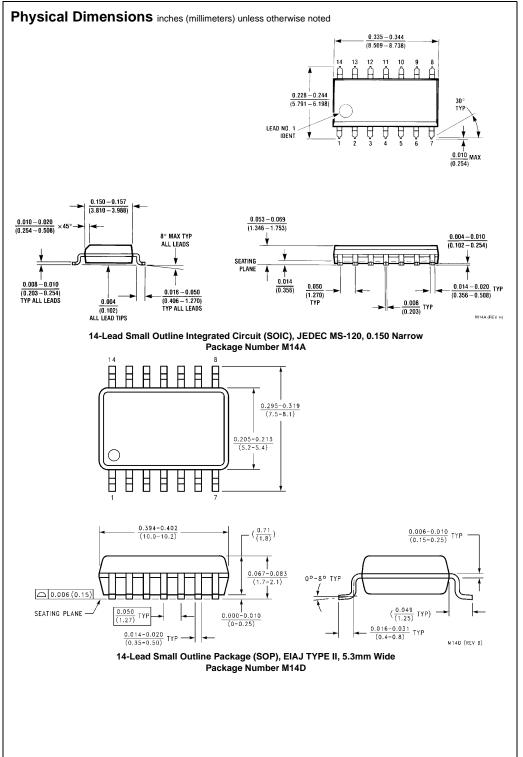
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Тур	Max	Units	v _{cc}	Conditions
V_{T+}	Positive-going Threshold		1.5		2.0	V	5.0	
V _{T-}	Negative-going Threshold		0.7		1.1	V	5.0	
ΔV_{T}	Hysteresis (V _T ⁺ – V _T ⁻)		0.4			V	5.0	
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH	10% V _{CC}	2.5			V	Min	I _{OH} = -1 mA
	Voltage 5% V _{CC}		2.7					$I_{OH} = -1 \text{ mA}$
V _{OL}	Output LOW Voltage	10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current				5.0	μΑ	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakd	own Test			7.0	μΑ	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Curr	ent			50	μΑ	Max	$V_{OUT} = V_{CC}$
V _{ID}	Input Leakage Test		4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Cur	rent			3.75	μА	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current				-0.6	mA	Max	V _{IN} = 0.5V
Ios	Output Short-Circuit Curren	t	-60		-150	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current				17.0	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current				18.0	mA	Max	V _O = LOW

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		Units	
		Min	Тур	Max	Min	Max		
t _{PLH}	Propagation Delay	4.0		10.5	3.5	12.0		
t _{PHL}	A_n , B_n to \overline{O}_n	5.0		12.5	5.0	13.0	ns	



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) $\frac{0.740 - 0.770}{(18.80 - 19.56)}$ 0.090 (2.286) 14 13 12 11 10 9 14 13 12 0.250 ± 0.010 (6.350 ± 0.254 PIN NO. 1 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX OPTION 1 OPTION 02 0.135±0.005 $\frac{0.300 - 0.320}{(7.620 - 8.128)}$ (3.429 ± 0.127) 0.065 (1.651) (3.683 - 5.080) $\frac{0.008 - 0.016}{(0.203 - 0.406)} \text{ TYP}$ 95°±5 0.020 $\frac{0.125 - 0.150}{(3.175 - 3.810)}$ 0.075 ±0.015 (1.905 ±0.381) 0.280 (7.112)-MIN $\frac{0.014 - 0.023}{(0.356 - 0.584)}$ TYP $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

1.270 ± 0.010 (1.270 − 0.254)

Fairchild does not assume any responsibility for use of any circuity described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

 $\frac{0.325 + 0.040 \\
- 0.015}{(8.255 + 1.016) \\
- 0.381)}$

N14A (REV F)

www.fairchildsemi.com