

74F283 4-Bit Binary Full Adder with Fast Carry

General Description

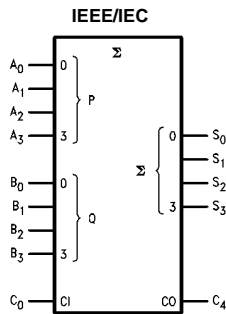
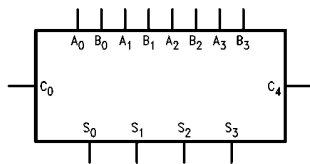
The 74F283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words (A_0 – A_3 , B_0 – B_3) and a Carry input (C_0). It generates the binary Sum outputs (S_0 – S_3) and the Carry output (C_4) from the most significant bit. The 74F283 will operate with either active HIGH or active LOW operands (positive or negative logic).

Ordering Code:

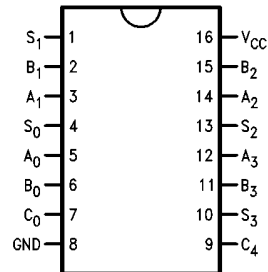
Order Number	Package Number	Package Description
74F283SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F283SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F283PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input I_H/I_L Output I_{OH}/I_{OL}
A_0 – A_3	A Operand Inputs	1.0/2.0	20 μ A/–1.2 mA
B_0 – B_3	B Operand Inputs	1.0/2.0	20 μ A/–1.2 mA
C_0	Carry Input	1.0/1.0	20 μ A/–0.6 mA
S_0 – S_3	Sum Outputs	50/33.3	–1 mA/20 mA
C_4	Carry Output	50/33.3	–1 mA/20 mA

Functional Description

The 74F283 adds two 4-bit binary words (A plus B) plus the incoming Carry (C₀). The binary sum appears on the Sum (S₀-S₃) and outgoing carry (C₄) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C₀, A₀, B₀ can be arbitrarily assigned to pins 5, 6 and 7 for DIPs, and 7, 8 and 9 for chip carrier packages. Due to the symmetry of the binary add function, the 74F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See Figure 1. Note that if C₀ is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

Due to pin limitations, the intermediate carries of the 74F283 are not brought out for use as inputs or outputs.

However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure 2 shows how to make a 3-bit adder. Figure 3 shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A₃, B₃) LOW makes S₃ dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure 3 shows a way of dividing the 74F283 into a 2-bit and a 1-bit adder. The third stage adder (A₂, B₂, S₂) is used merely as a means of getting a carry (C₁₀) signal into the fourth stage (via A₂ and B₂) and bringing out the carry from the second stage on S₂. Note that as long as A₂ and B₂ are the same, whether HIGH or LOW, they do not influence S₂. Similarly, when A₂ and B₂ are the same the carry into the third stage does not influence the carry out of the third stage. Figure 4 shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S₀, S₁ and S₂ present a binary number equal to the number of inputs I₁-I₅ that are true. Figure 5 shows one method of implementing a 5-input majority gate. When three or more of the inputs I₁-I₅ are true, the output M₅ is true.

	C ₀	A ₀	A ₁	A ₂	A ₃	B ₀	B ₁	B ₂	B ₃	S ₀	S ₁	S ₂	S ₃	C ₄
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16 Active LOW: 1 + 5 + 6 = 12 + 0

FIGURE 1. Active HIGH versus Active LOW Interpretation

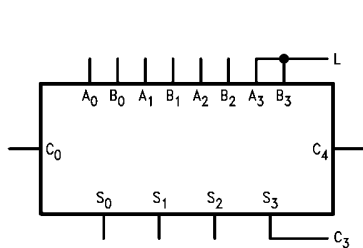


FIGURE 2. 3-Bit Adder

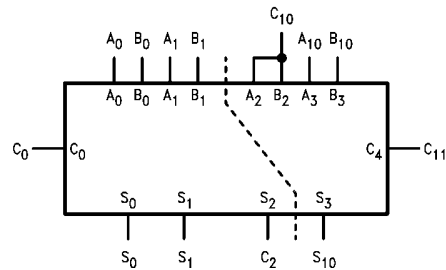


FIGURE 3. 2-Bit and 1-Bit Adders

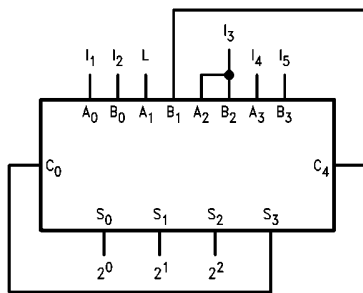


FIGURE 4. 5-Input Encoder

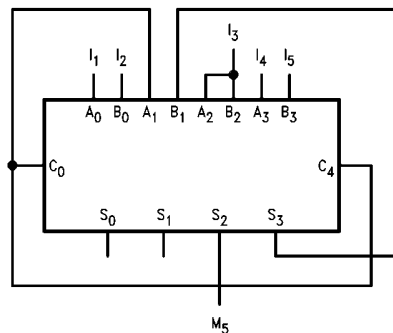
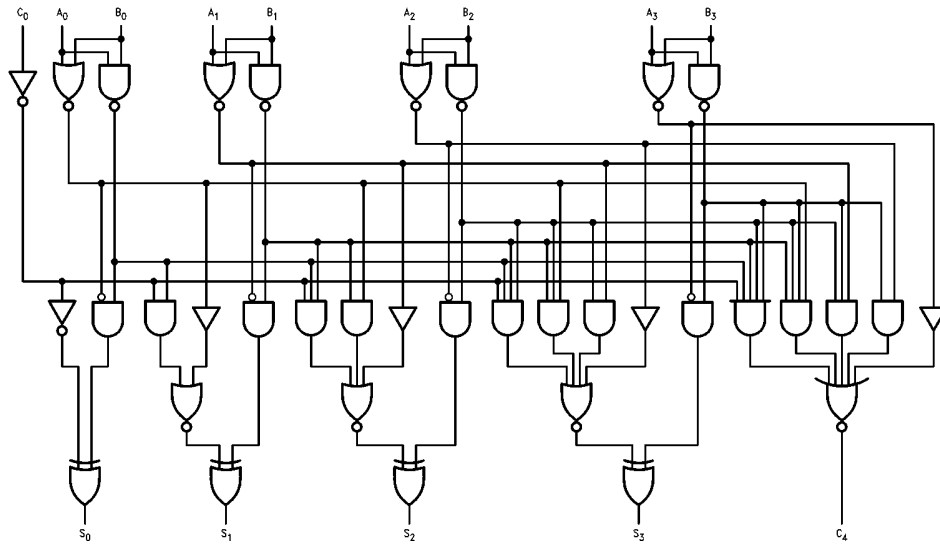


FIGURE 5. 5-Input Majority Gate

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions	
Storage Temperature	-65°C to +150°C	Free Air Ambient Temperature	0°C to +70°C
Ambient Temperature under Bias	-55°C to +125°C	Supply Voltage	+4.5V to +5.5V
Junction Temperature under Bias	-55°C to +150°C		
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V		
Input Voltage (Note 2)	-0.5V to +7.0V		
Input Current (Note 2)	-30 mA to +5.0 mA		
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)			
Standard Output	-0.5V to V _{CC}		
3-STATE Output	-0.5V to +5.5V		
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)		
ESD Last Passing Voltage (Min)	4000V		

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

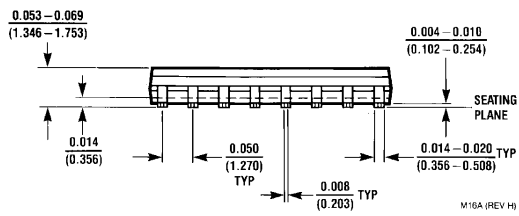
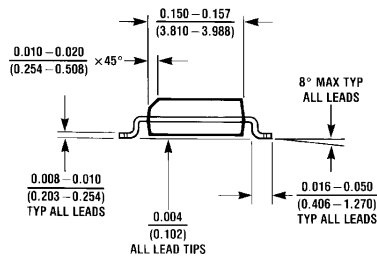
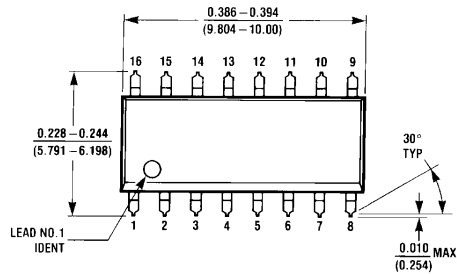
DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 5% V _{CC}	2.5 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6 -1.2	mA	Max	V _{IN} = 0.5V (C ₀) V _{IN} = 0.5V (A _n , B _n)
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current		36	55	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		36	55	mA	Max	V _O = LOW

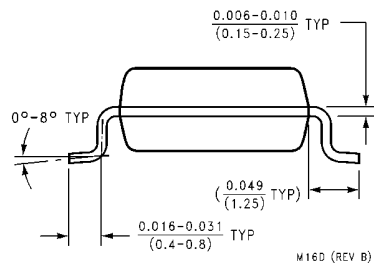
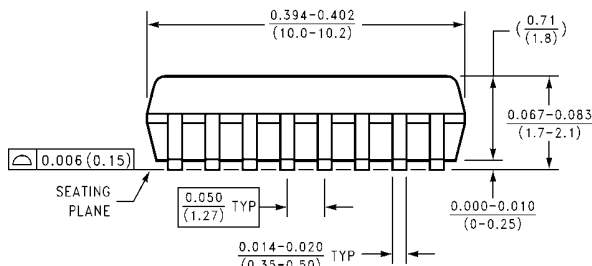
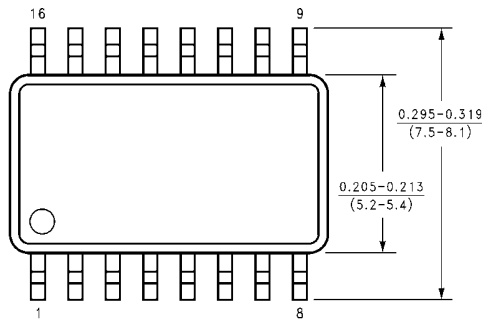
AC Electrical Characteristics

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.5	7.0	9.5	3.5	14.0	3.5	11.0	ns
t _{PHL}	C ₀ to S _n	3.0	7.0	9.5	3.0	14.0	3.0	11.0	
t _{PLH}	Propagation Delay	3.0	7.0	9.5	3.0	17.0	3.0	13.0	ns
t _{PHL}	A _n or B _n to S _n	3.0	7.0	9.5	3.0	14.0	3.0	11.5	
t _{PLH}	Propagation Delay	3.0	5.7	7.5	3.0	10.5	3.0	8.5	ns
t _{PHL}	C ₀ to C ₄	3.0	5.4	7.0	2.5	10.0	3.0	8.0	
t _{PLH}	Propagation Delay	3.0	5.7	7.5	3.0	10.5	3.0	8.5	ns
t _{PHL}	A _n or B _n to C ₄	2.5	5.3	7.0	2.5	10.0	2.5	8.0	

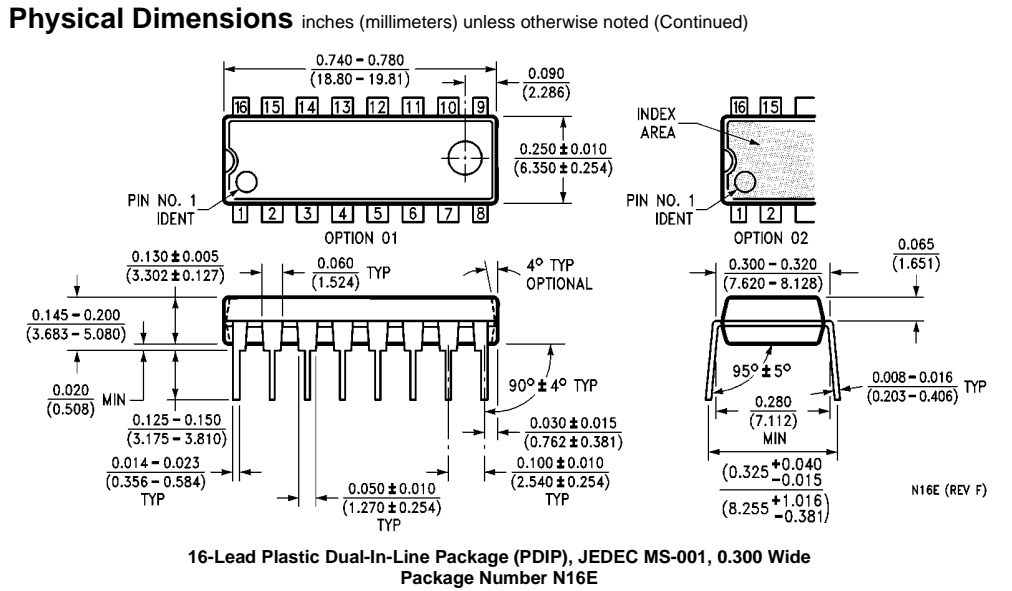
Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com