

74F299 Octal Universal Shift/Storage Register with Common Parallel I/O Pins

General Description

The 74F299 is an 8-bit universal shift/storage register with 3-STATE outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs, Q_0 – Q_7 , are provided to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

Features

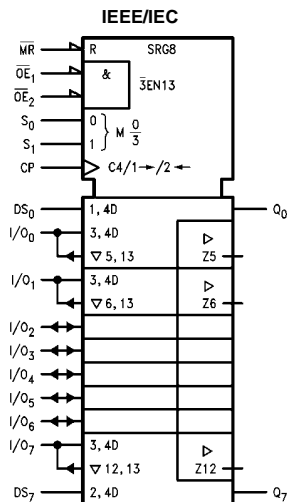
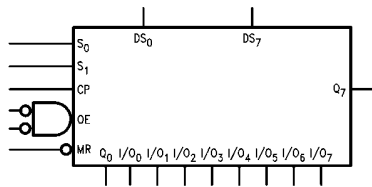
- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- 3-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

Ordering Code:

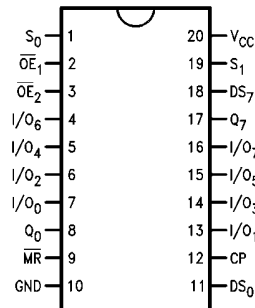
Order Number	Package Number	Package Description
74F299SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F299SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F299PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/-0.6 mA
DS ₀	Serial Data Input for Right Shift	1.0/1.0	20 μ A/-0.6 mA
DS ₇	Serial Data Input for Left Shift	1.0/1.0	20 μ A/-0.6 mA
S ₀ , S ₁	Mode Select Inputs	1.0/2.0	20 μ A/-1.2 mA
\overline{MR}	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 μ A/-0.6 mA
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs (Active LOW)	1.0/1.0	20 μ A/-0.6 mA
I/O ₀ -I/O ₇	Parallel Data Inputs or 3-STATE Parallel Outputs	3.5/1.083 150/40(33.3)	70 μ A/-0.65 mA -3 mA/24 mA (20 mA)
Q ₀ , Q ₇	Serial Outputs	50/33.3	-1 mA/20 mA

Functional Description

The 74F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S₀ and S₁, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q₀ and Q₇ are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on \overline{MR} overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

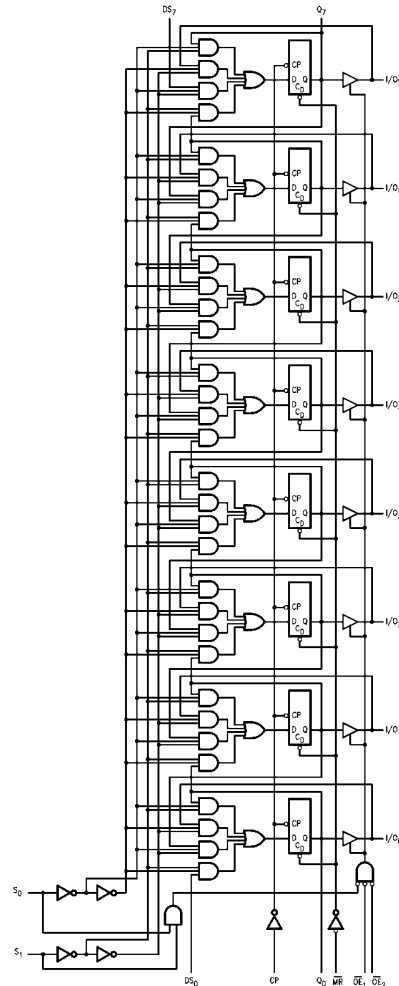
A HIGH signal on either \overline{OE}_1 or \overline{OE}_2 disables the 3-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-STATE outputs are also disabled by HIGH signals on both S₀ and S₁ in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
MR	S ₁	S ₀	CP	
L	X	X	X	Asynchronous Reset; Q ₀ -Q ₇ = LOW
H	H	H	↗	Parallel Load; I/O _n → Q _n
H	L	H	↗	Shift Right; DS ₀ → Q ₀ , Q ₀ → Q ₁ , etc.
H	H	L	↗	Shift Left; DS ₇ → Q ₇ , Q ₇ → Q ₆ , etc.
H	L	L	X	Hold

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ↗ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
ESD Last Passing Voltage (Min)	4000V
Voltage Applied to Output	
in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	
Current Applied to Output	-0.5V to +5.5V
in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

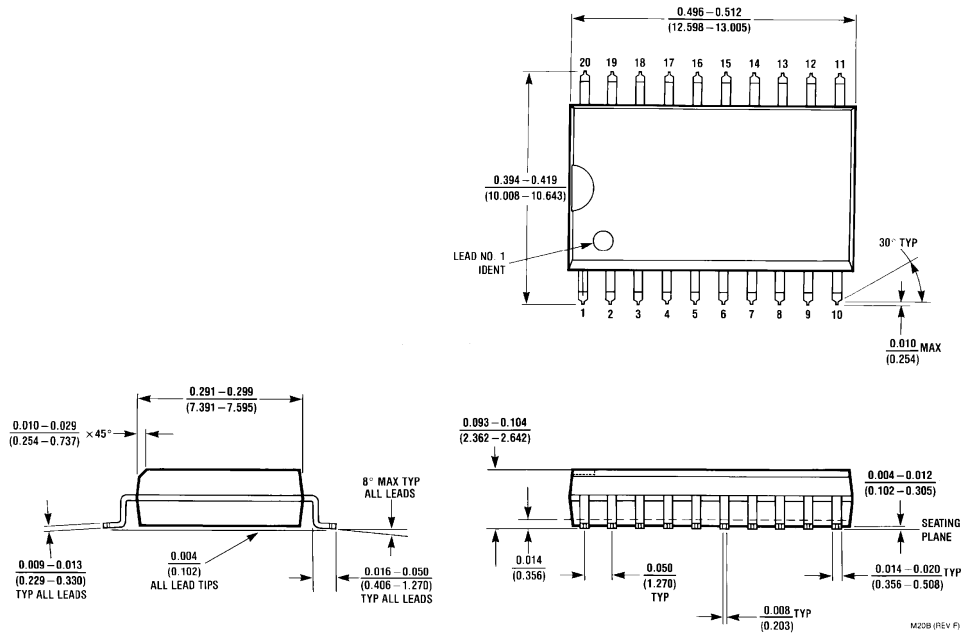
DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA (Q ₀ , Q ₇ , I/O _n)
		10% V _{CC}	2.4				I _{OH} = -3 mA (I/O _n)
		5% V _{CC}	2.7				I _{OH} = -1 mA (Q ₀ , Q ₇ , I/O _n)
		5% V _{CC}	2.7				I _{OH} = -3 mA (I/O _n)
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA (Q ₀ , Q ₇)
		10% V _{CC}		0.5			I _{OL} = 24 mA (I/O _n)
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V (CP, DS ₀ , DS ₇ , S ₀ , S ₁ , MR, OE ₁ , OE ₂)
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V (CP, DS ₀ , DS ₇ , S ₀ , S ₁ , MR, OE ₁ , OE ₂)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)			0.5	mA	Max	V _{IN} = 5.5V (I/O _n)
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6 -1.2	mA	Max	V _{IN} = 0.5V (CP, DS ₀ , DS ₇ , MR, OE ₁ , OE ₂) V _{IN} = 0.5V (S ₀ , S ₁)
I _{IH+} I _{OZH}	Output Leakage Current			70	μA	Max	V _{I/O} = 2.7V (I/O _n)
I _{IL+} I _{OZL}	Output Leakage Current			-650	μA	Max	V _{I/O} = 0.5V (I/O _n)
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CCH}	Power Supply Current		68	95	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		68	95	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		68	95	mA	Max	V _O = HIGH Z

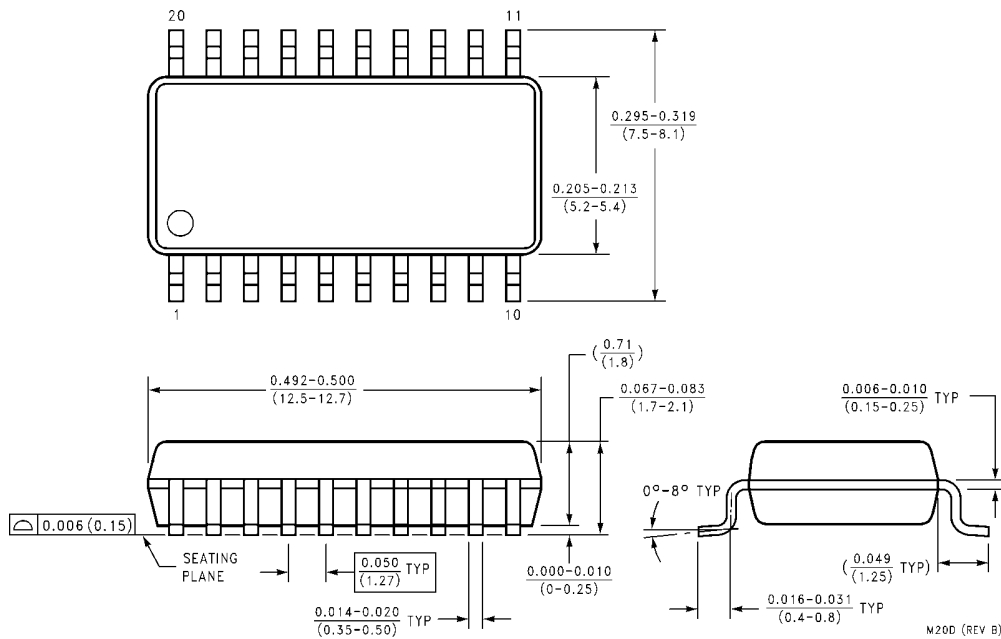
AC Electrical Characteristics									
Symbol	Parameter	T _A = +25°C V _{CC} = 5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0V C _L = 50 pF		T _A = 0 to +70°C V _{CC} = 5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t _{MAX}	Maximum Input Frequency	70	100		85		70		MHz
t _{PLH}	Propagation Delay CP to Q ₀ or Q ₇	4.0	7.0	8.0	4.0	9.0	4.0	8.5	ns
t _{PHL}	Propagation Delay CP to I/O _n	4.5	6.5	8.0	4.5	9.5	4.5	8.5	
t _{PLH}	Propagation Delay CP to I/O _n	3.5	7.0	9.0	3.5	10.0	3.5	10.0	ns
t _{PHL}	Propagation Delay MR to Q ₀ or Q ₇	5.5	7.5	9.5	5.5	12.5	5.5	10.5	
t _{PHL}	Propagation Delay MR to I/O _n	5.5	11.0	10.0	5.5	12.0	5.5	10.5	ns
t _{PZH}	Output Enable Time OE to I/O _n	3.5	6.0	8.0	3.0	9.5	3.5	9.0	ns
t _{PZL}	Output Disable Time OE to I/O _n	4.0	7.0	10.0	4.0	13.0	4.0	11.0	
t _{PHZ}	Output Enable Time S _n to I/O _n	2.0	4.5	6.0	1.5	7.0	2.0	7.0	ns
t _{PLZ}	Output Disable Time S _n to I/O _n	1.0	4.0	5.5	1.0	6.5	1.0	6.5	
t _{PZH}	Output Enable Time S _n to I/O _n	3.5		9.0	3.0	10.5	3.5	10.0	ns
t _{PZL}	Output Disable Time S _n to I/O _n	4.0		10.0	4.0	13.0	4.0	11.0	ns
t _{PHZ}	Output Enable Time S _n to I/O _n	2.5		6.0	1.5	7.0	2.5	7.0	ns
t _{PLZ}	Output Disable Time S _n to I/O _n	1.5		5.5	1.0	6.5	1.5	6.5	

AC Operating Requirements								
Symbol	Parameter	T _A = +25°C V _{CC} = 5.0V		T _A = -55°C to +125°C V _{CC} = 5.0V		T _A = 0 to +70°C V _{CC} = 5.0V		Units
		Min	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	8.5		10.0		8.5		ns
t _S (L)	S ₀ or S ₁ to CP	8.5		7.5		8.5		
t _H (H)	Hold Time, HIGH or LOW	0		0		0		ns
t _H (L)	S ₀ or S ₁ to CP	0		0		0		
t _S (H)	Setup Time, HIGH or LOW	5.0		5.0		5.0		ns
t _S (L)	I/O _n , DS ₀ or DS ₇ to CP	5.0		5.0		5.0		
t _H (H)	Hold Time, HIGH or LOW	2.0		2.0		2.0		ns
t _H (L)	I/O _n , DS ₀ or DS ₇ to CP	2.0		2.0		2.0		
t _W (H)	CP Pulse Width	5.0		5.0		5.0		ns
t _W (L)	HIGH or LOW	5.0		5.0		5.0		ns
t _W (L)	MR Pulse Width, LOW	5.0		6.0		5.0		ns
t _{REC}	Recovery Time, MR to CP	7.0		12.0		7.0		ns

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B**



**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number MD20D**

