

74F544 Octal Registered Transceiver

General Description

The 74F544 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 24 mA while the B outputs are rated for 64 mA. The 74F544 inverts data in both directions.

Features

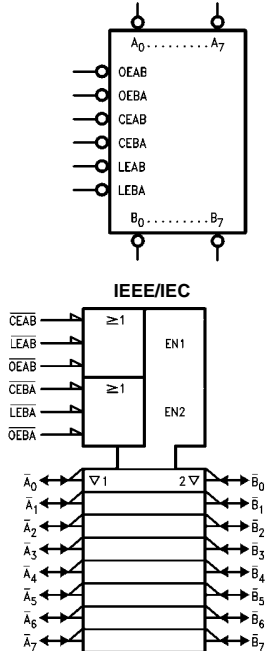
- 8-bit octal transceiver
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 24 mA, B outputs sink 64 mA

Ordering Code:

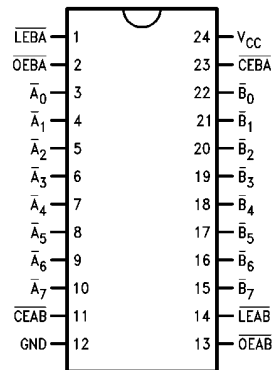
Order Number	Package Number	Package Description
74F544SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F544MSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74F544SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L.	Input I_{IH}/I_{IL}
		HIGH/LOW	Output I_{OH}/I_{OL}
\overline{OEAB}	A-to-B Output Enable Input (Active LOW)	1.0/1.0	20 μ A/-0.6 mA
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)	1.0/1.0	20 μ A/-0.6 mA
\overline{CEAB}	A-to-B Enable Input (Active LOW)	1.0/2.0	20 μ A/-1.2 mA
\overline{CEBA}	B-to-A Enable Input (Active LOW)	1.0/2.0	20 μ A/-1.2 mA
\overline{LEAB}	A-to-B Latch Enable Input (Active LOW)	1.0/1.0	20 μ A/-0.6 mA
\overline{LEBA}	B-to-A Latch Enable Input (Active LOW)	1.0/1.0	20 μ A/-0.6 mA
$\overline{A_0}-\overline{A_7}$	A-to-B Data Inputs or	3.5/1.083	70 μ A/-650 μ A
$\overline{B_0}-\overline{B_7}$	B-to-A 3-STATE Outputs	150/40(33.3)	-3 mA/24 mA (20 mA)
$\overline{B_0}-\overline{B_7}$	B-to-A Data Inputs or	3.5/1.083	70 μ A/-650 μ A
	A-to-B 3-STATE Outputs	600/106.6(80)	-12 mA/64 mA (48 mA)

Functional Description

The 74F544 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable (\overline{CEAB}) input must be LOW in order to enter data from $\overline{A_0}-\overline{A_7}$ or take data from $\overline{B_0}-\overline{B_7}$, as indicated in the Data I/O Control Table. With \overline{CEAB} LOW, a LOW signal on the A-to-B Latch Enable (\overline{LEAB}) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the \overline{LEAB} signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With \overline{CEAB} and \overline{OEAB} both LOW, the 3-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the \overline{CEBA} , \overline{LEBA} and \overline{OEBA} inputs.

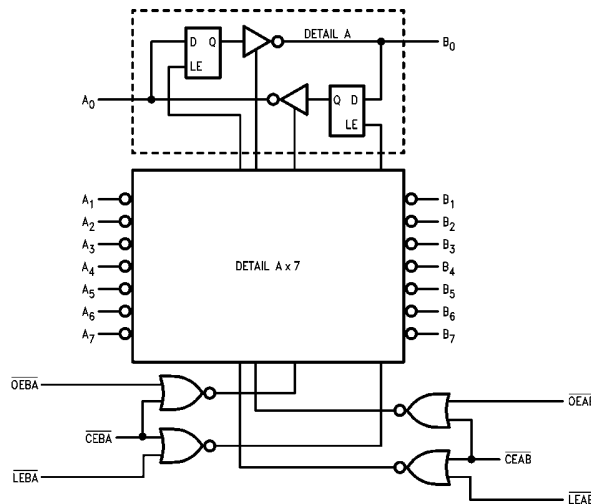
Data I/O Control Table

Inputs			Latch Status	Output Buffers
\overline{CEAB}	\overline{LEAB}	\overline{OEAB}		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Note: A-to-B data flow shown; B-to-A flow control is the same, except using \overline{CEBA} , \overline{LEBA} and \overline{OEBA}

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA, (except \bar{A}_n, \bar{B}_n)
V _{OH}	Output HIGH Voltage	10% V _{CC} 10% V _{CC} 10% V _{CC} 5% V _{CC} 5% V _{CC}	2.5 2.4 2.0 2.7 2.7		V	Min	I _{OH} = -1 mA (\bar{A}_n) I _{OH} = -3 mA (\bar{A}_n, \bar{B}_n) I _{OH} = -15 mA (\bar{B}_n) I _{OH} = -1 mA (\bar{A}_n) I _{OH} = -3 mA (\bar{A}_n, \bar{B}_n)
V _{OL}	Output LOW Voltage	10% V _{CC} 10% V _{CC}		0.5 0.55	V	Min	I _{OL} = 24 mA (\bar{A}_n) I _{OL} = 64 mA (\bar{B}_n)
I _{IH}	Input HIGH Current			20.0 5.0	μA	Max	V _{IN} = 2.7V (except \bar{A}_n, \bar{B}_n)
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V (except \bar{A}_n, \bar{B}_n)
I _{BVIT}	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V _{IN} = 5.5V (\bar{A}_n, \bar{B}_n)
I _{CEX}	Output HIGH Leakage Current			250	μA	Max	V _{OUT} = V _{CC} (\bar{A}_n, \bar{B}_n)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6 -1.2	mA	Max	V _{IN} = 0.5V (OEAB, OEBA) V _{IN} = 0.5V (CEAB, CEBA)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (\bar{A}_n, \bar{B}_n)
I _{IL} + I _{OZL}	Output Leakage Current			-650	μA	Max	V _{OUT} = 0.5V (\bar{A}_n, \bar{B}_n)
I _{OS}	Output Short-Circuit Current	-60 -100		-150 -225	mA	Max	V _{OUT} = 0V (\bar{A}_n) V _{OUT} = 0V (\bar{B}_n)
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V (\bar{A}_n, \bar{B}_n)
I _{CCH}	Power Supply Current		70	105	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		85	130	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		83	125	mA	Max	V _O = HIGH Z

Absolute Maximum Ratings (Note 1)	
Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions	
Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

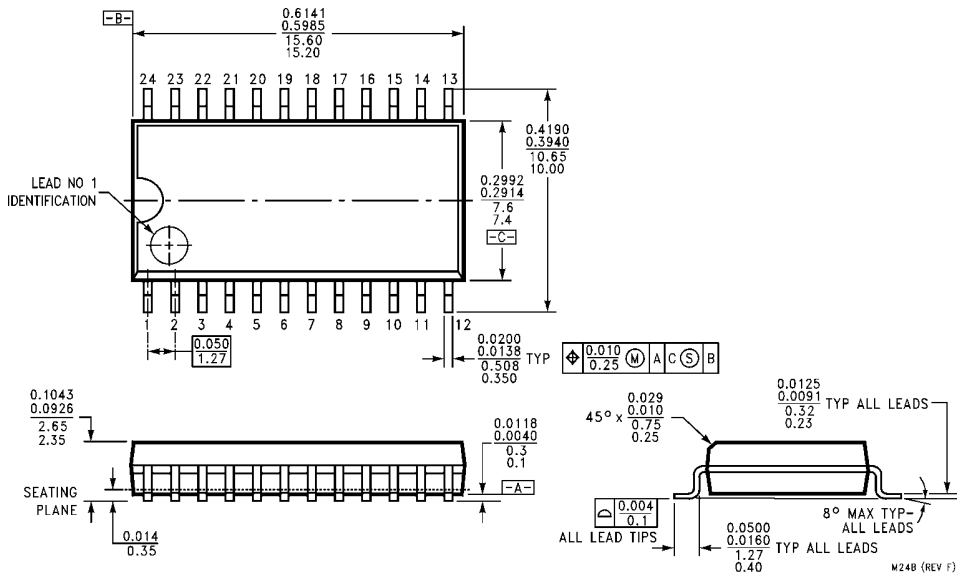
Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

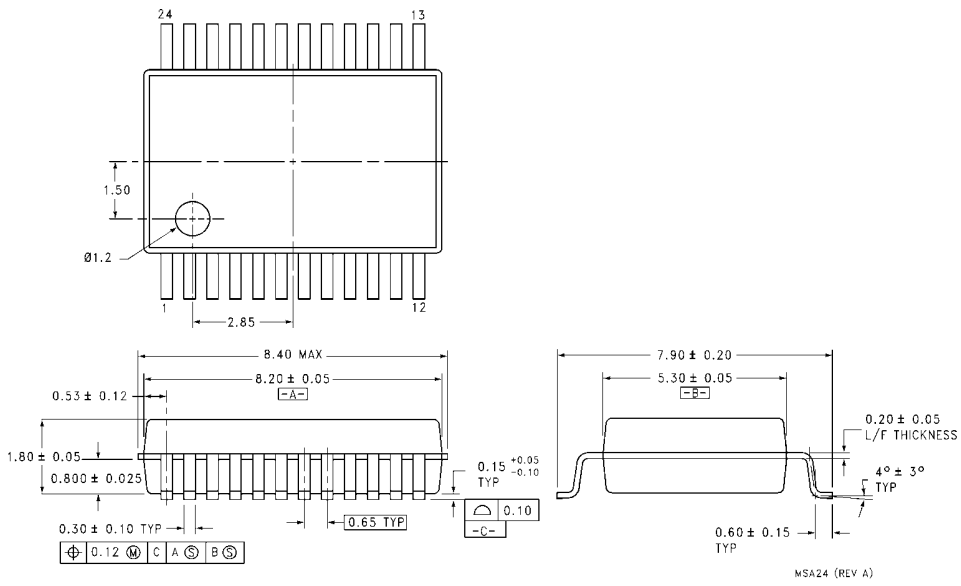
DC Electrical Characteristics

AC Electrical Characteristics									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	3.0	7.0	9.5	3.0	12.0	3.0	10.5	ns
t_{PHL}	Transparent Mode \overline{A}_n to \overline{B}_n or \overline{B}_n to \overline{A}_n	3.0	5.0	6.5	2.5	8.5	3.0	7.5	
t_{PLH}	Propagation Delay	6.0	10.0	13.0	6.0	18.0	6.0	14.5	ns
t_{PHL}	\overline{LEBA} to \overline{A}_n	4.0	7.0	9.5	4.0	11.5	4.0	10.5	
t_{PLH}	Propagation Delay	6.0	10.0	13.0	6.0	18.0	6.0	14.5	ns
t_{PHL}	\overline{LEAB} to \overline{B}_n	4.0	7.0	9.5	4.0	11.5	4.0	10.5	
t_{PZH}	Output Enable Time	3.0	7.0	9.0	3.0	11.0	3.0	10.0	ns
t_{PZL}	\overline{OEBA} or \overline{OEAB} to \overline{A}_n or \overline{B}_n \overline{CEBA} or \overline{CEAB} to \overline{A}_n or \overline{B}_n	4.0	7.5	10.5	4.0	13.0	4.0	12.0	
t_{PHZ}	Output Disable Time	1.0	6.0	8.0	2.0	10.0	1.0	9.0	
t_{PLZ}	\overline{OEBA} or \overline{OEAB} to \overline{A}_n or \overline{B}_n \overline{CEBA} or \overline{CEAB} to \overline{A}_n or \overline{B}_n	2.5	5.5	10.5	2.0	9.5	2.5	11.5	
AC Operating Requirements									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		Units	
		Min	Max	Min	Max	Min	Max		
$t_S(H)$	Setup Time, HIGH or LOW	3.0		3.0		3.0		ns	
$t_S(L)$	\overline{A}_n or \overline{B}_n to \overline{LEBA} or \overline{LEAB}	3.0		3.0		3.0			
$t_H(H)$	Hold Time, HIGH or LOW	3.0		3.0		3.0			
$t_H(L)$	\overline{A}_n or \overline{B}_n to \overline{LEBA} or \overline{LEAB}	3.0		3.0		3.0			
$t_W(L)$	Latch Enable, B to A Pulse Width, LOW	6.0		9.0		7.5		ns	

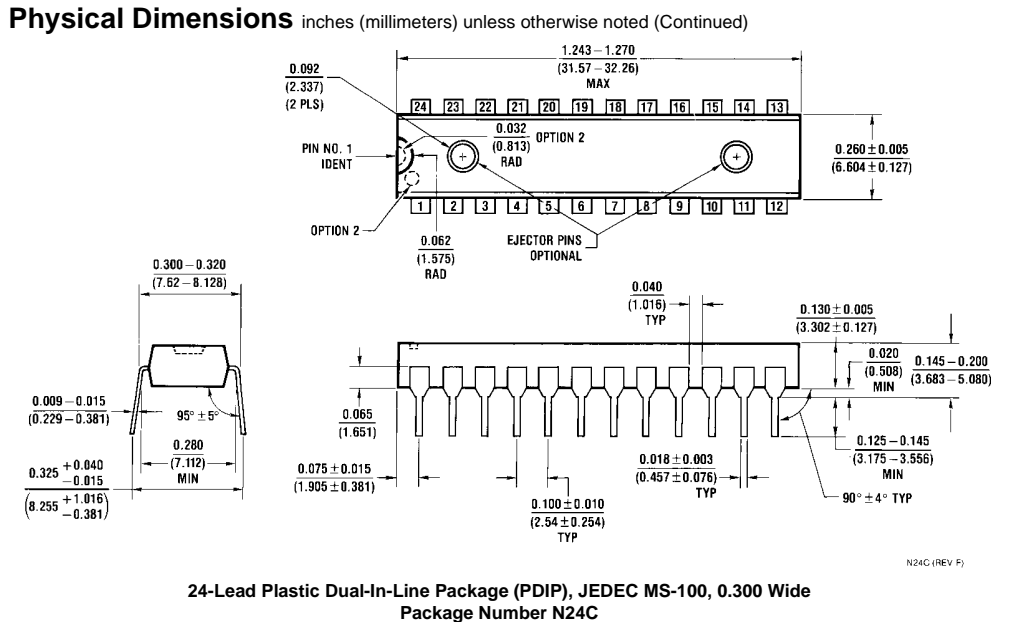
Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M24B



24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide Package Number MSA24



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