

## 74F676

### 16-Bit Serial/Parallel-In, Serial-Out Shift Register

#### General Description

The 74F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is HIGH, information present on the parallel data ( $P_0$ - $P_{15}$ ) inputs is entered on the falling edge of the Clock Pulse ( $\overline{CP}$ ) input signal. When M is LOW, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A HIGH signal on the Chip Select ( $\overline{CS}$ ) input prevents both parallel and serial operations.

#### Features

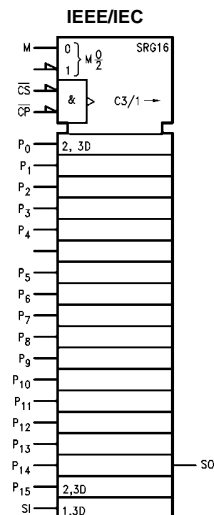
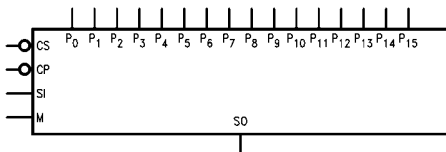
- 16-bit parallel-to-serial conversion
- 16-bit serial-in, serial-out
- Chip select control
- Slim 24 lead 300 mil package

#### Ordering Code:

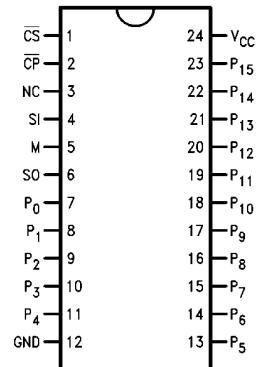
Order Number	Package Number	Package Description
74F676SC	M24B	28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F676PC	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600 Wide
74F676SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Logic Symbols



#### Connection Diagram



## Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$P_0$ - $P_{15}$	Parallel Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{CP}$	Clock Pulse Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
M	Mode Select Input	1.0/1.0	20 $\mu$ A/-0.6 mA
SI	Serial Data Input	1.0/1.0	20 $\mu$ A/-0.6 mA
SO	Serial Output	50/33.3	-1 mA/20 mA

## Functional Description

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

**HOLD**— a HIGH signal on the Chip Select ( $\overline{CS}$ ) input prevents clocking, and data is stored in the sixteen registers.

**Shift/Serial Load**— data present on the SI pin shifts into the register on the falling edge of  $\overline{CP}$ . Data enters the  $Q_0$  position and shifts toward  $Q_{15}$  on successive clocks, finally appearing on the SO pin.

**Parallel Load**— data present on  $P_0$ - $P_{15}$  are entered into the register on the falling edge of  $\overline{CP}$ . The SO output represents the  $Q_{15}$  register output.

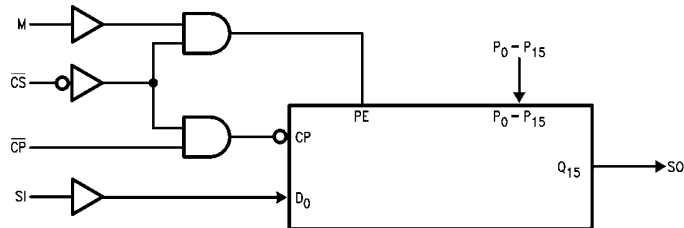
To prevent false clocking,  $\overline{CP}$  must be LOW during a LOW-to-HIGH transition of  $\overline{CS}$ .

## Shift Register Operations Table

Control Input			Operating Mode
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	$\sim$	Shift/Serial Load
L	H	$\sim$	Parallel Load

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
 $\sim$  = HIGH-to-LOW Transition

## Block Diagram



**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

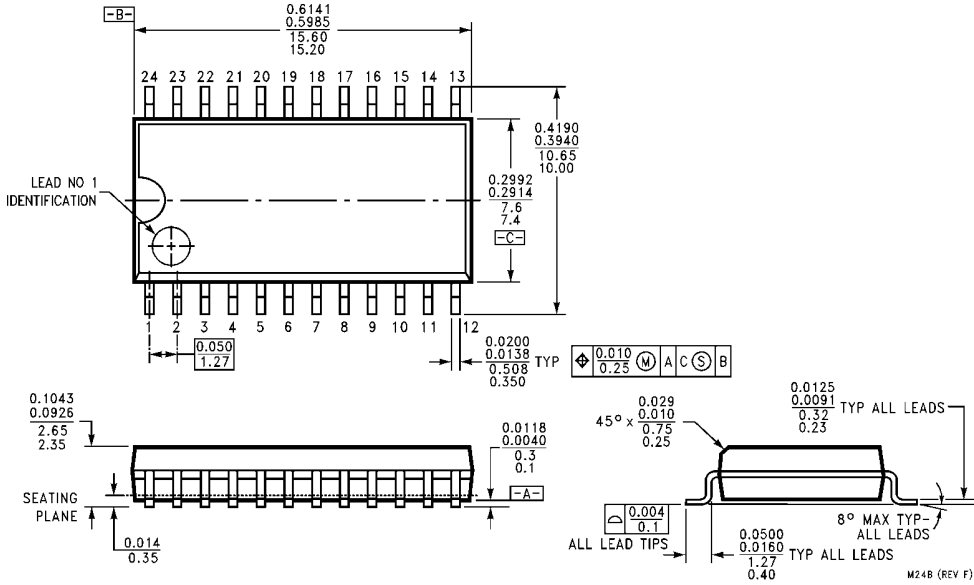
**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

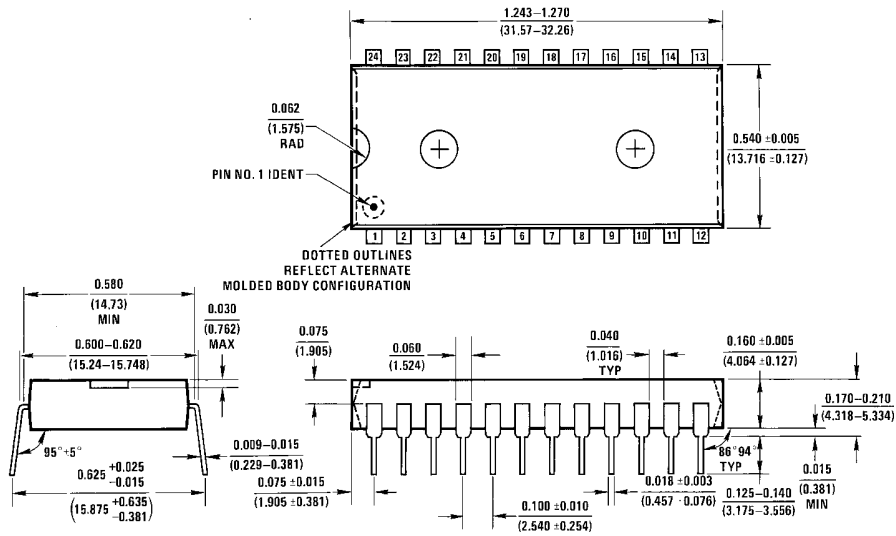
Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 5% V <sub>CC</sub>	2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA, All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>ID</sub> = 150 mV, All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current			72	mA	Max	

AC Electrical Characteristics									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } 125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency	100	110		45		90		MHz
$t_{PLH}$	Propagation Delay	4.5	9.0	11.0	4.5	17.0	4.5	12.0	ns
$t_{PHL}$	$\overline{CP}$ to SO	5.0	9.0	12.5	5.0	14.5	5.0	13.5	
AC Operating Requirements									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = -55^\circ\text{C to } 125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{---}$ $V_{CC} = +5.0\text{V}$		Units	
		Min	Max	Min	Max	Min	Max		
$t_S(H)$	Setup Time, HIGH or LOW	4.0		4.0		4.0		ns	
$t_S(L)$	SI to $\overline{CP}$	4.0		4.0		4.0			
$t_H(H)$	Hold Time, HIGH or LOW	4.0		4.0		4.0			
$t_H(L)$	SI to $\overline{CP}$	4.0		4.0		4.0			
$t_S(H)$	Setup Time, HIGH or LOW	3.0		3.0		3.0		ns	
$t_S(L)$	$P_n$ to $\overline{CP}$	3.0		3.0		3.0			
$t_H(H)$	Hold Time, HIGH or LOW	4.0		4.0		4.0			
$t_H(L)$	$P_n$ to $\overline{CP}$	4.0		4.0		4.0			
$t_S(H)$	Setup Time, HIGH or LOW	8.0		8.0		8.0		ns	
$t_S(L)$	M to $\overline{CP}$	8.0		8.0		8.0			
$t_H(H)$	Hold Time, HIGH or LOW	2.0		2.0		2.0			
$t_H(L)$	M to $\overline{CP}$	2.0		2.0		2.0			
$t_S(L)$	Setup Time, LOW $\overline{CS}$ to $\overline{CP}$	10.0		12.0		10.0		ns	
$t_H(H)$	Hold Time, HIGH $\overline{CS}$ to $\overline{CP}$	10.0		10.0		10.0			
$t_W(H)$	$\overline{CP}$ Pulse Width	4.0		5.0		4.0		ns	
$t_W(L)$	HIGH or LOW	6.0		9.0		6.0			

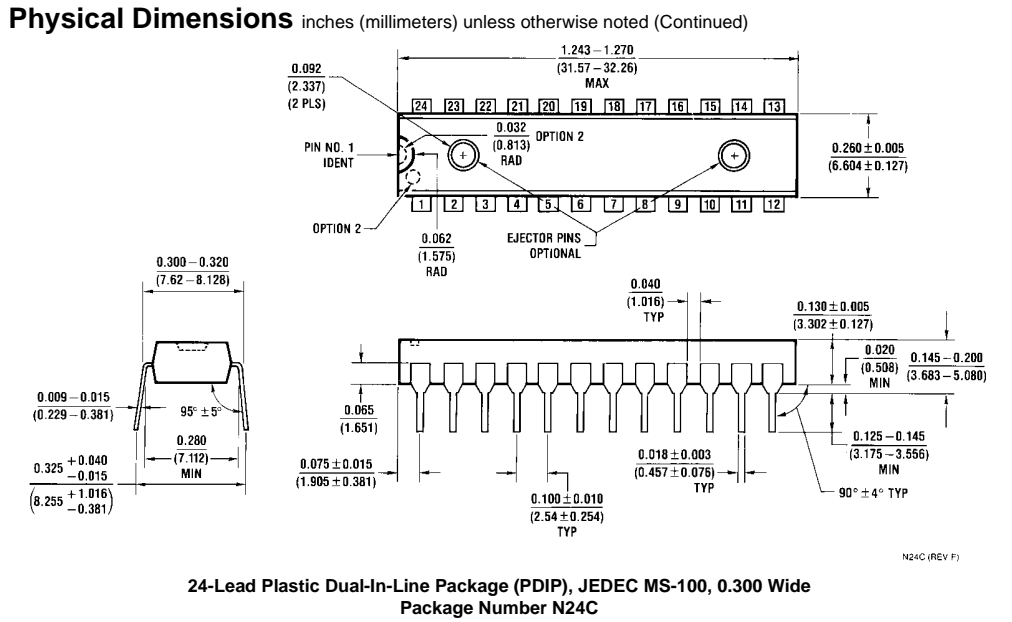
**Physical Dimensions** inches (millimeters) unless otherwise noted



**28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M24B**



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600 Wide Package Number N24A**



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)