FAIRCHILD SEMICONDUCTOR™

March 1990
Revised August 1999

74F794
8-Bit Register with Readback

General Description

The 74F794 is an 8-bit register with readback capability designed to store data as well as read the register information back onto the data bus. The I/O bus (D bus) has 3-STATE outputs. Current sinking capability is 64 mA on both the D and Q busses.

Data is loaded into the registers on the LOW-to-HIGH transition of the clock (CP). The output enable ($\overline{OE}$) is used to enable data on D_0–D_7. When $\overline{OE}$ is LOW, the output of the registers is enabled on D_0–D_7, enabling D as an output bus. When OE is HIGH, D_0–D_7 are inputs to the registers configuring D as an input bus.

Features

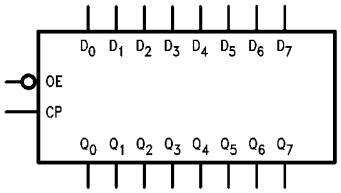
- 3-STATE outputs on the I/O port
- D and Q output sink capability of 64 mA
- Functionally and pin equivalent to the 74LS794

Ordering Code:

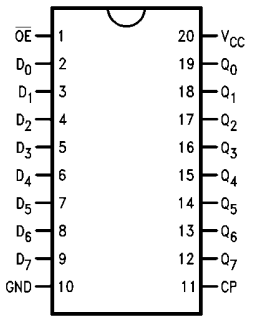
Order Number	Package Number	Package Description
74F794SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F794PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



© 1999 Fairchild Semiconductor Corporation

Input Loading/Fan-Out

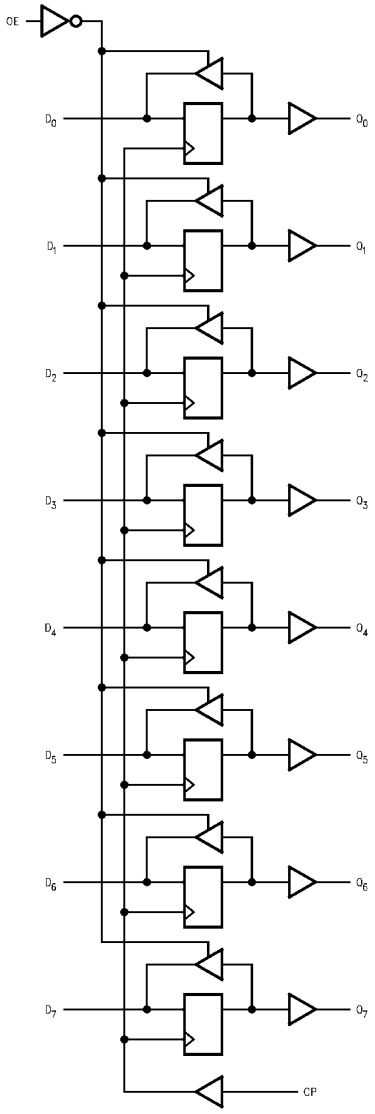
Pin Names	Description	HIGH/LOW	
		(U.L.)	Current
$\overline{OE}$	Output Enable Input	1.0/1.0	20 µA/–0.6 mA
CP	Clock Pulse Inputs	1.0/1.0	20 µA/–0.6 mA
D_0–D_7	D Bus Inputs/	3.5/1.083	70 µA/–650 µA
	3-STATE Outputs	750/106.6	–15 mA/64 mA
Q_0–Q_7	Q Bus Outputs	750/106.6	–15 mA/64 mA

Truth Table

Inputs		Outputs	
CP	$\overline{OE}$	Q	D
L or H or ↓	L	Q_n	Output, Q
L or H or ↓	H	Q_n	Input
↑	L	Q_n	Output, Q (Note 1)
↑	H	D	Input

Note 1: In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q_n.

Logic Diagram



Absolute Maximum Ratings(Note 2)

Storage Temperature	−65°C to + 150°C
Ambient Temperature under Bias	−55° to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
ESD Last Passing Voltage (Min)	4000V
Voltage Applied to Output	
In HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	Twice the Rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to 70°C
Supply Voltage	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q_n.

Note 4: Either voltage limit or current limit is sufficient to protect inputs.

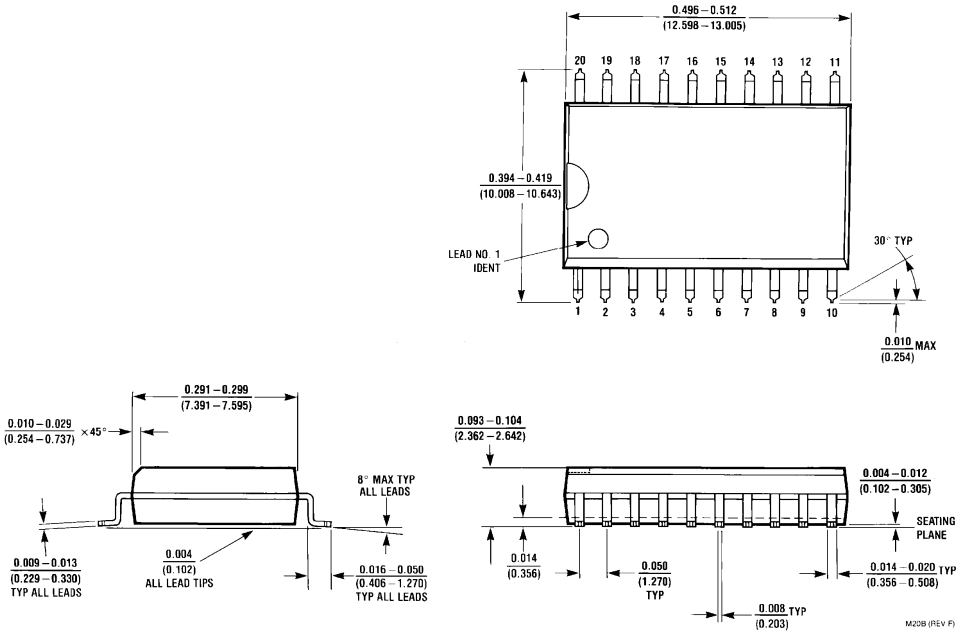
DC Electrical Characteristics over Operating Temperature Range unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0	2.8 2.44		V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage		0.45	0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7.0	µA	Max	V_{IN} = 7.0V ($\overline{OE}$, CP)
I_{BVIT}	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V_{IN} = 5.5V (D_n)
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current			3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current			−0.6	mA	Max	V_{IN} = 0.5V ($\overline{OE}$, CP)
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{IH} + I_{OZH}	Output Leakage Current			70	µA	Max	V_{OUT} = 2.7V (Dn)
I_{IL} + I_{OZL}	Output Leakage Current			−650	µA	Max	V_{OUT} = 0.5V (Dn)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Circuit Leakage Current			3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	µA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current			65	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			80	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			80	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

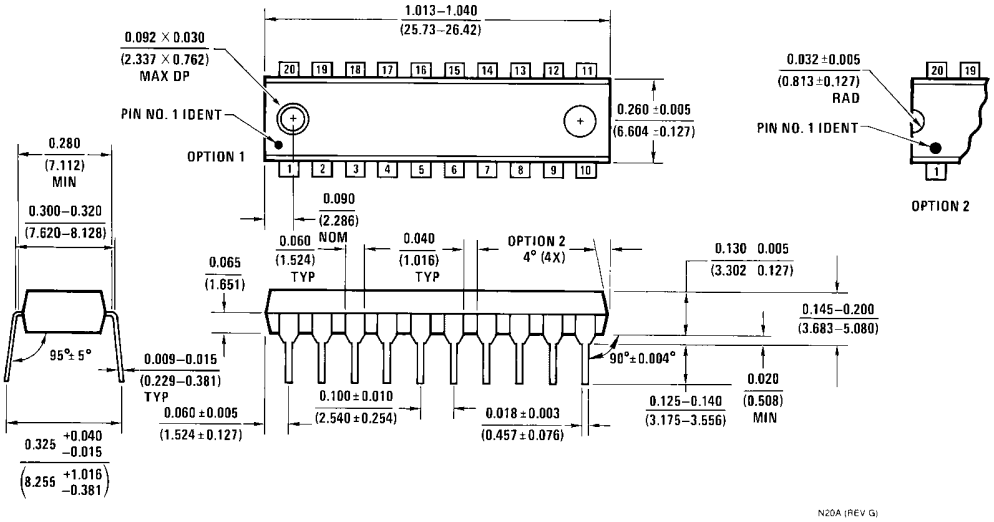
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	90			90		MHz
t_{PLH}	Propagation Delay	2.5		7.0	2.5	8.0	ns
t_{PHL}	CP to Q_n	2.5		8.0	2.5	9.0	
t_{PZH}	Output Enable Time	2.3		8.5	2.0	9.0	ns
t_{PZL}		2.0		10.0	2.0	10.5	
t_{PHZ}	Output Disable Time	1.0		7.0	1.0	8.0	ns
t_{PLZ}		1.0		7.0	1.0	8.0	
t_S(H)	Setup Time, HIGH or LOW	4.0			4.0		ns
t_S(L)	Bus to Clock	4.0			4.0		
t_H(H)	Hold Time, HIGH or LOW	1.5			1.5		ns
t_H(L)	Bus to Clock	1.5			1.5		
t_W(H	Clock Pulse Width	5.8			5.8		ns
	HIGH or LOW	5.8			5.8		

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com