

74F899

9-Bit Latchable Transceiver with Parity Generator/Checker

General Description

The 74F899 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data busses in either direction. It has a guaranteed current sinking capability of 24 mA at the A-bus and 64 mA at the B-bus.

The 74F899 features independent latch enables for the A-to-B direction and the B-to-A direction, a select pin for ODD/EVEN parity, and separate error signal output pins for checking parity.

Features

- Latchable transceiver with output sink of 24 mA at the A-bus and 64 mA at the B-bus
- Option to select generate parity and check or "feed-through" data/parity in directions A-to-B or B-to-A
- Independent latch enables for A-to-B and B-to-A directions
- Select pin for ODD/EVEN parity
- $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ output pins for parity checking
- Ability to simultaneously generate and check parity
- May be used in systems applications in place of the 74F543 and 74F280
- May be used in system applications in place of the 74F657 and 74F373 (no need to change T/R to check parity)

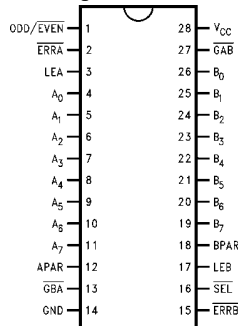
Ordering Code:

Order Number	Package Number	Package Description
74F899SC	M28B	28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F899QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square

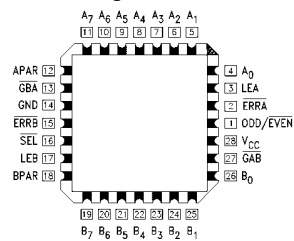
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

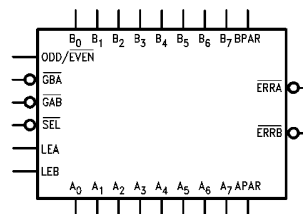
Pin Assignment for SOIC



Pin Assignment for PCC



Logic Symbol



Input Loading/Fan-Out

Pin Names	Description	HIGH/LOW	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A ₀ –A ₇	Data Inputs/ Data Outputs	1.0/1.0 150/40	20 μ A/–0.6 mA –3 mA/24 mA
B ₀ –B ₇	Data Inputs/ Data Outputs	1.0/1.0 600/106.6	20 μ A/–0.6 mA –12 mA/64 mA
APAR	A Bus Parity Input/Output	1.0/1.0 150/40	20 μ A/–0.6 mA –3 mA/24 mA
BPAR	B Bus Parity Input/Output	1.0/1.0 600/106.6	20 μ A/–0.6 mA –12 mA/64 mA
$\overline{ODD/EVEN}$	Parity Select Input	1.0/1.0	20 μ A/–0.6 mA
\overline{GBA} , \overline{GAB}	Output Enable Inputs	1.0/1.0	20 μ A/–0.6 mA
\overline{SEL}	Mode Select Input	1.0/1.0	20 μ A/–0.6 mA
LEA, LEB	Latch Enable Inputs	1.0/1.0	20 μ A/–0.6 mA
\overline{ERRA} , \overline{ERRB}	Error Signal Outputs	50/33.3	–1 mA/20 mA

Pin Descriptions

Pin Names	Description
A ₀ –A ₇	A Bus Data Inputs/Data Outputs
B ₀ –B ₇	B Bus Data Inputs/Data Outputs
APAR, BPAR	A and B Bus Parity Inputs
$\overline{ODD/EVEN}$	$\overline{ODD/EVEN}$ Parity Select, Active LOW for EVEN Parity
\overline{GBA} , \overline{GAB}	Output Enables for A or B Bus, Active LOW
\overline{SEL}	Select Pin for Feed-Through or Generate Mode, LOW for Generate Mode
LEA, LEB	Latch Enables for A and B Latches, HIGH for Transparent Mode
\overline{ERRA} , \overline{ERRB}	Error Signals for Checking Generated Parity with Parity In, LOW if Error Occurs

Functional Description

The 74F899 has three principal modes of operation which are outlined below. These modes apply to both the A-to-B and B-to-A directions.

- Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select (\overline{SEL}) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by \overline{ERRB} (\overline{ERRA}).
- Bus A (B) communicates to Bus B (A) in a feed-through mode if \overline{SEL} is HIGH. Parity is still generated and checked as \overline{ERRA} and \overline{ERRB} in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).
- Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking (see Function Table).

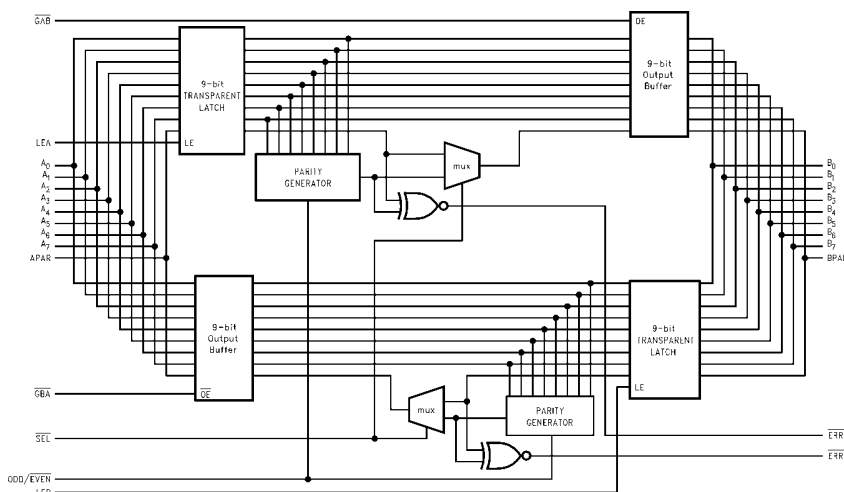
Function Table

Inputs					Operation
$\overline{\text{GAB}}$	$\overline{\text{GBA}}$	$\overline{\text{SEL}}$	LEA	LEB	
H	H	X	X	X	Busses A and B are 3-STATE.
H	L	L	L	H	Generates parity from B[0:7] based on $\text{O}/\overline{\text{E}}$ (Note 1). Generated parity \rightarrow APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$.
H	L	L	H	H	Generates parity from B[0:7] based on $\text{O}/\overline{\text{E}}$. Generated parity \rightarrow APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$. Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$.
H	L	L	X	L	Generates parity from B latch data based on $\text{O}/\overline{\text{E}}$. Generated parity \rightarrow APAR. Generated parity checked against latched BPAR and output as $\overline{\text{ERRB}}$.
H	L	H	X	H	BPAR/B[0:7] \rightarrow APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$.
H	L	H	H	H	BPAR/B[0:7] \rightarrow APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$. Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$.
L	H	L	H	L	Generates parity for A[0:7] based on $\text{O}/\overline{\text{E}}$. Generated parity \rightarrow BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$.
L	H	L	H	H	Generates parity from A[0:7] based on $\text{O}/\overline{\text{E}}$. Generated parity \rightarrow BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$. Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$.
L	H	L	L	X	Generates parity from A latch data based on $\text{O}/\overline{\text{E}}$. Generated parity \rightarrow BPAR. Generated parity checked against latched APAR and output as $\overline{\text{ERRA}}$.
L	H	H	H	L	APAR/A[0:7] \rightarrow BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$.
L	H	H	H	H	APAR/A[0:7] \rightarrow BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$. Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$.

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

Note 1: $\text{O}/\overline{\text{E}}$ = ODD/EVEN

Functional Block Diagram



Absolute Maximum Ratings (Note 2)				Recommended Operating Conditions			
Storage Temperature		-65°C to +150°C		Free Air Ambient Temperature		0°C to +70°C	
Ambient Temperature under Bias		-55°C to +125°C		Supply Voltage		+4.5V to +5.5V	
Junction Temperature under Bias		-55°C to +150°C					
V _{CC} Pin Potential to Ground Pin		-0.5V to +7.0V					
Input Voltage (Note 3)		-0.5V to +7.0V					
Input Current (Note 3)		-30 mA to +5.0 mA					
Voltage Applied to Output							
in HIGH State (with V _{CC} = 0V)							
Standard Output		-0.5V to V _{CC}					
3-STATE Output		-0.5V to +5.5V					
Current Applied to Output							
in LOW State (Max)		Twice the Rated I _{OL} (mA)					
ESD Last Passing Voltage (Min)		4000V					
Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.							
Note 3: Either voltage limit or current limit is sufficient to protect inputs.							
DC Electrical Characteristics							
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC}	2.5		V		I _{OH} = -1 mA
		10% V _{CC}	2.4				I _{OH} = -3 mA
		10% V _{CC}	2.0				I _{OH} = -15 mA (B _n , B _{PAR})
		5% V _{CC}	2.7				I _{OH} = -1 mA
		5% V _{CC}	2.7				I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V		I _{OL} = 20 mA
		5% V _{CC}		0.55			(A _n , APAR, <u>ERRA</u> , <u>ERRB</u>)
		10% V _{CC}		0.55			I _{OL} = 24 mA
							(A _n , APAR, <u>ERRA</u> , <u>ERRB</u>)
							I _{OL} = 64 mA (B _n , B _{PAR})
V _{TH}	Input Threshold Voltage		1.45		V		±0.1V, Sweep Edge Rate must be > 1V/50 ns
V _{OLV}	Negative Ground Bounce Voltage		1.0		V		Observed on "quiet" output during simultaneous switching of remaining outputs
V _{OLP}	Positive Ground Bounce Voltage		1.0		V		Observed on "quiet" output during simultaneous switching of remaining outputs
I _{IL}	Input Low Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V (<u>ODD/EVEN</u> , <u>GAB</u> , <u>GAB</u> , <u>SEL</u> , <u>LEA</u> , <u>LEB</u>)
I _{BVIT}	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V _{IN} = 5.5V (A _n , B _n , A _{PAR} , B _{PAR})
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input Low Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{IH+}	Output Leakage Current			70	μA	Max	V _{I/O} = 2.7V (A _n , B _n , APAR, BPAR)
I _{OZH}	Output Leakage Current						

DC Electrical Characteristics (Continued)								
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions	
I _{IL+} I _{OZL}	Output Leakage Current			-650	μA	Max	V _{I/O} = 0.5V (A _n , B _n , APAR, BPAR)	
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V (A _n , APAR, \overline{ERRA} , \overline{ERRB})	
		-100		-225	mA	Max	V _{OUT} = 0V (B _n , BPAR)	
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V	
I _{CCH}	Power Supply Current		132	155	mA	Max	V _O = HIGH	
I _{CCL}	Power Supply Current		178	210	mA	Max	V _O = LOW, GAB = LOW, GBA = HIGH, V _{IL} = LOW	
I _{CCZ}	Power Supply Current		160	190	mA	Max	V _O = HIGH Z	
AC Electrical Characteristics								
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units	Figure Number
		Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	4.0	7.5	13.0	4.0	14.0	ns	Figure 1
t _{PHL}	A _n , APAR to B _n , BPAR	4.0	8.5	13.0	4.0	14.0		
t _{PLH}	Propagation Delay	7.5	12.0	17.0	7.5	18.0	ns	Figure 2
t _{PHL}	A _n , B _n to BPAR, APAR	7.5	12.5	17.0	7.5	18.0		
t _{PLH}	Propagation Delay	7.5	12.0	17.0	7.5	18.0	ns	Figure 3
t _{PHL}	A _n , B _n to \overline{ERRA} , \overline{ERRB}	7.5	12.5	17.0	7.5	18.0		
t _{PLH}	Propagation Delay	4.5	7.5	11.0	4.5	12.0	ns	Figure 4
t _{PHL}	ODD/ \overline{EVEN} to \overline{ERRA} , \overline{ERRB}	4.5	8.0	11.0	4.5	12.0		
t _{PLH}	Propagation Delay	4.5	7.5	11.5	4.5	12.5	ns	Figure 5
t _{PHL}	ODD/ \overline{EVEN} to APAR, BPAR	4.5	8.5	11.5	4.5	12.5		
t _{PLH}	Propagation Delay	5.5	9.0	13.0	5.5	14.0	ns	Figure 6
t _{PHL}	APAR, BPAR to \overline{ERRA} , \overline{ERRB}	5.5	9.5	13.0	5.5	14.0		
t _{PLH}	LEA/LEB to	9.5	13.0	17.5	7.5	18.0	ns	Figure 7
t _{PHL}	\overline{ERRA} / \overline{ERRB}	9.7		17.5	7.5	18.0		
t _{PLH}	Propagation Delay	3.0	6.0	10.0	3.0	11.0	ns	Figure 10
t _{PHL}	SEL to APAR, BPAR	3.0	7.0	10.0	3.0	11.0		
t _{PLH}	Propagation Delay	3.5	7.0	10.0	3.5	11.0	ns	Figure 11
t _{PHL}	LEB to A _n , APAR	3.5	8.0	10.0	3.5	11.0		
t _{PLH}	Propagation Delay	3.5	6.5	10.0	3.5	11.0	ns	Figure 11
t _{PHL}	LEA to B _n , BPAR	3.5	7.5	10.0	3.5	11.0		
t _{PZH}	Output Enable Time	1.0	4.5	10.0	1.0	11.0	ns	Figure 8, Figure 9
t _{PZL}	GBA or \overline{GAB} to A _n , APAR or B _n , BPAR	1.0	6.5	10.0	1.0	11.0		
t _{PHZ}	Output Disable Time	1.0	4.0	7.0	1.0	8.0	ns	Figure 8, Figure 9
t _{PLZ}	GBA or \overline{GAB} to A _n , APAR or B _n , BPAR	1.0	4.0	7.0	1.0	8.0		
t _S (H)	Setup Time, HIGH or LOW	5.0	1.6		5.0		ns	Figure 12, Figure 13
t _S (L)	A _n , B _n to LEA, LEB	5.0	1.8		5.0			
t _H (H)	Hold Time, HIGH or LOW	0	-1.7		0		ns	Figure 12, Figure 13
t _H (L)	A _n , B _n to LEA, LEB	0	-1.5		0			
t _W	Pulse Width for LEA, LEB	6.0	2.0		6.0		ns	Figure 14

AC Path

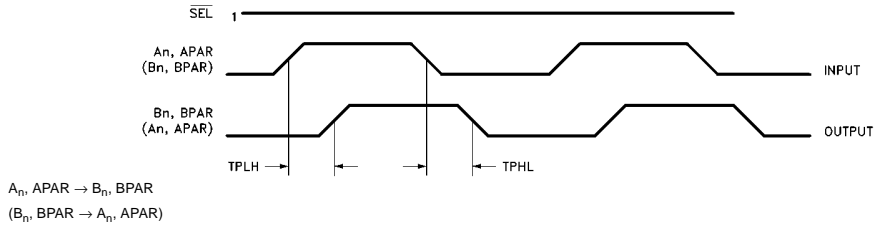


FIGURE 1.

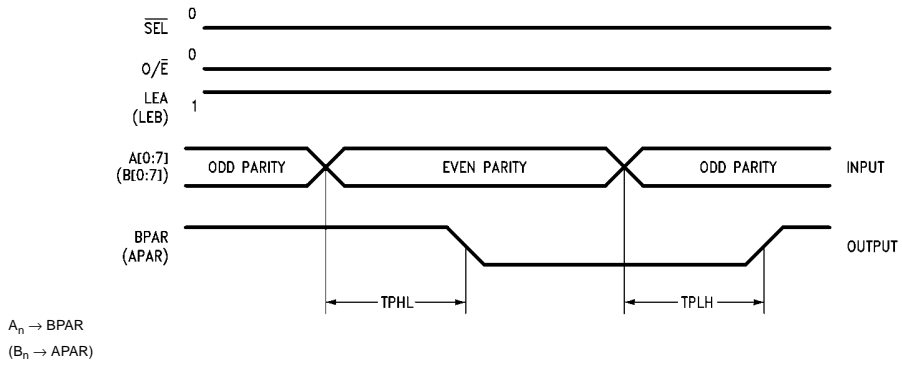


FIGURE 2.

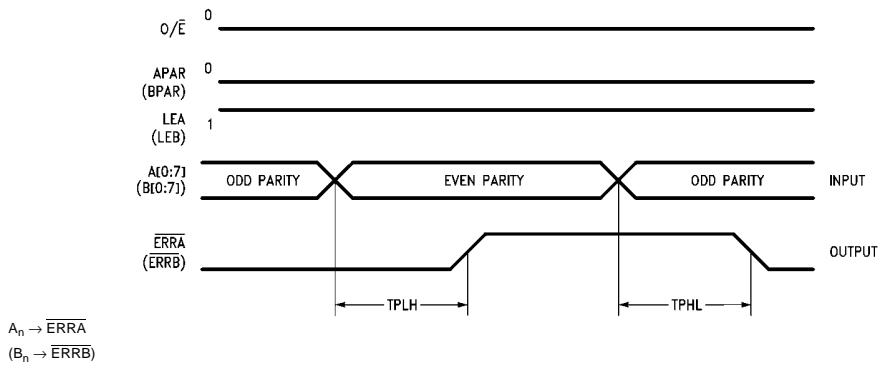


FIGURE 3.

AC Path (Continued)

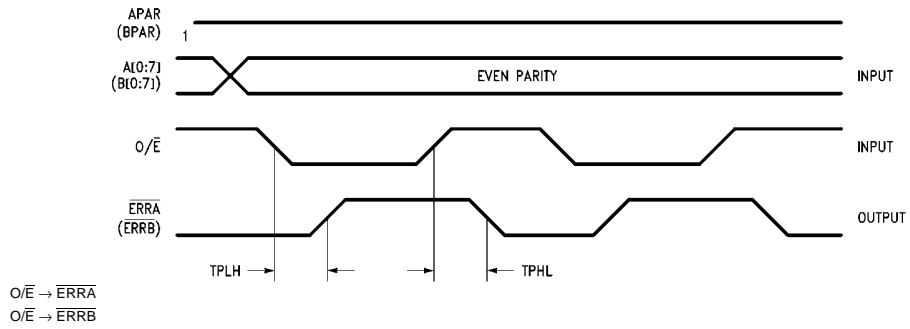


FIGURE 4.

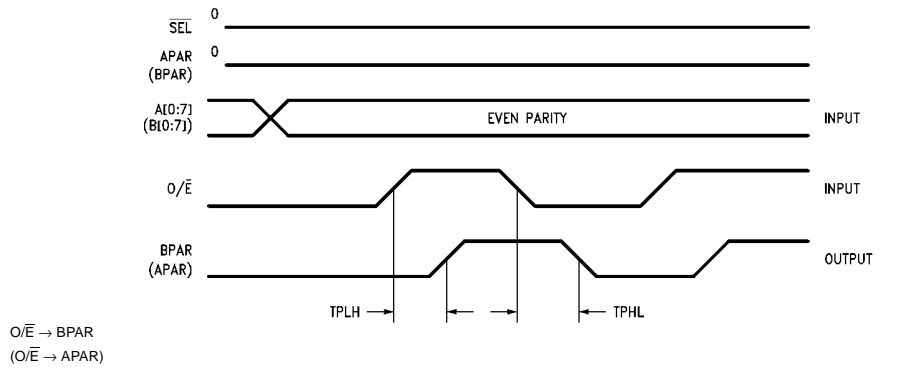


FIGURE 5.

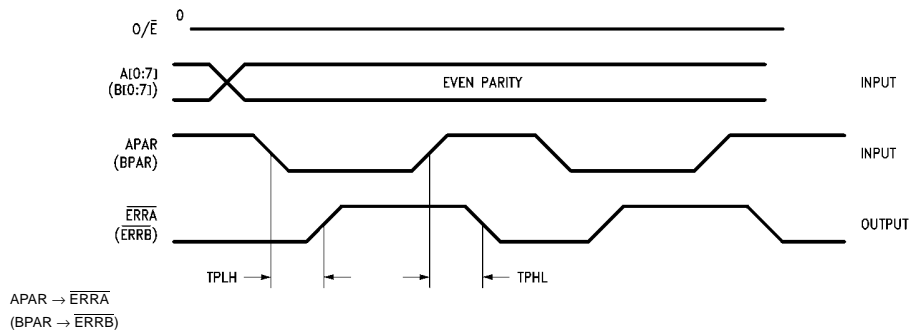


FIGURE 6.

AC Path (Continued)

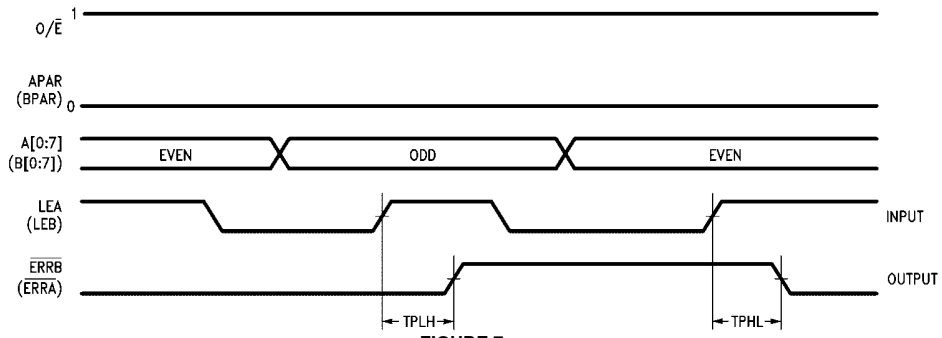


FIGURE 7.

ZH, HZ

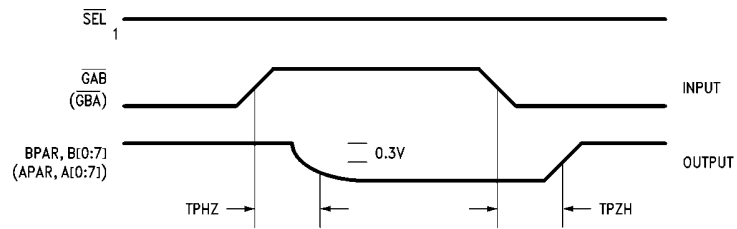


FIGURE 8.

ZL, LZ

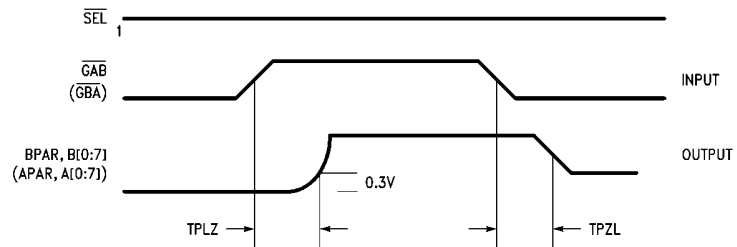


FIGURE 9.

AC Path (Continued)

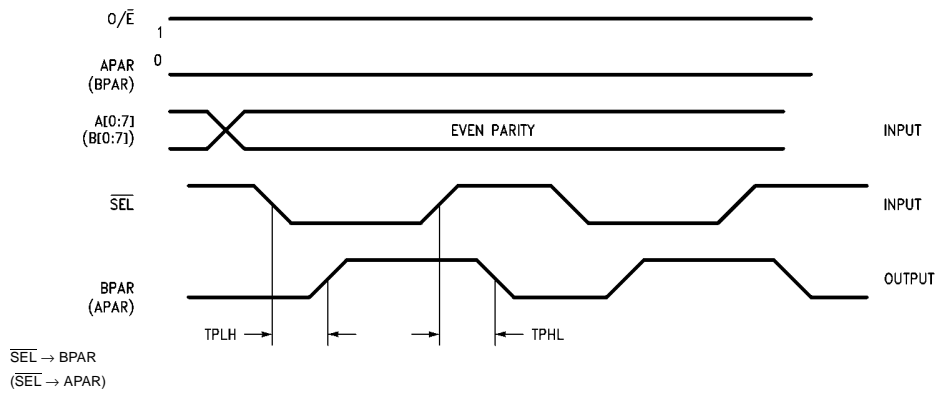


FIGURE 10.

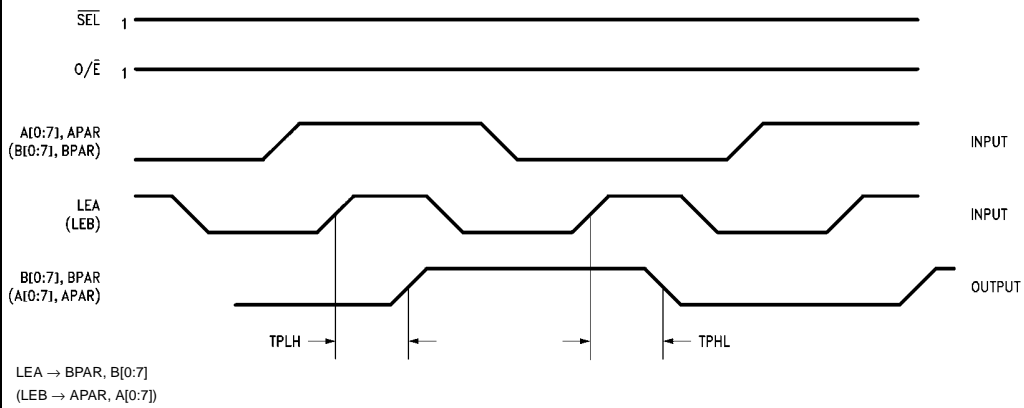


FIGURE 11.

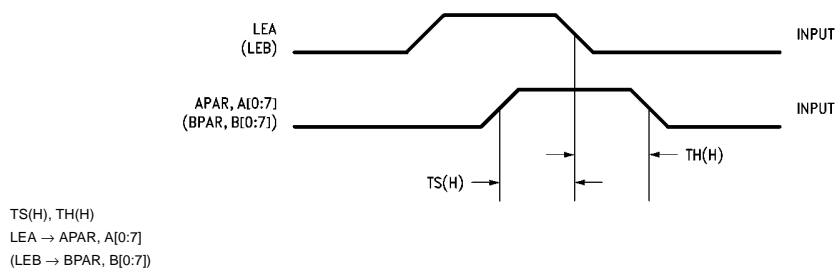
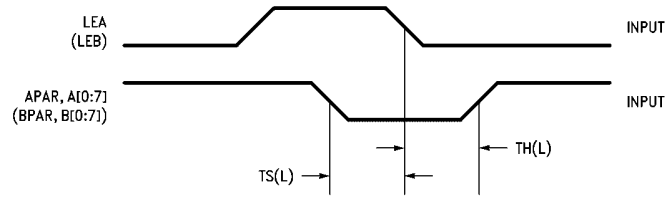


FIGURE 12.

AC Path (Continued)



TS(L), TH(L)
 LEA → APAR, A[0:7]
 (LEB → BPAR, B[0:7])

FIGURE 13.

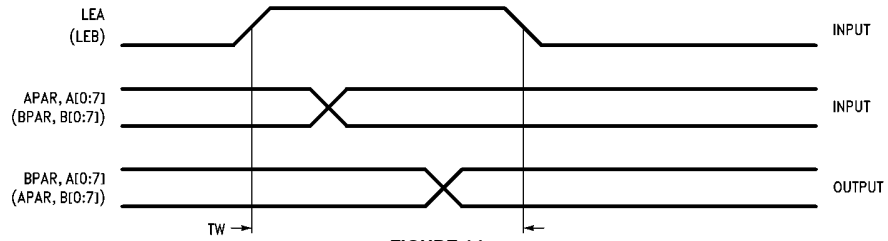
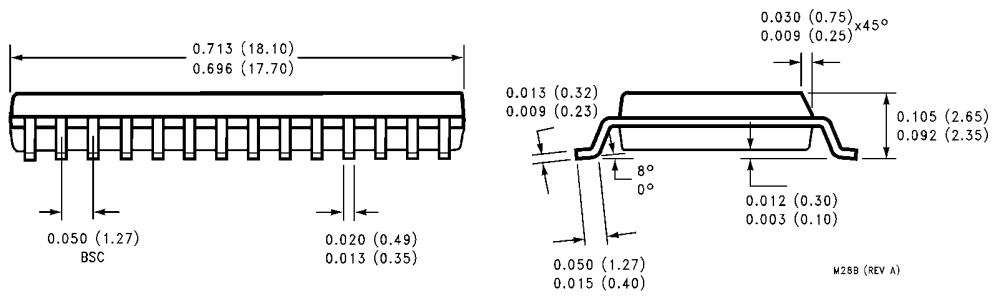
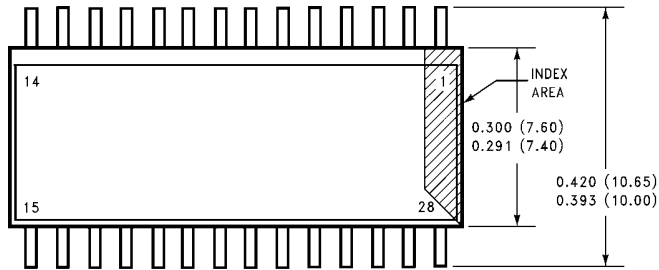


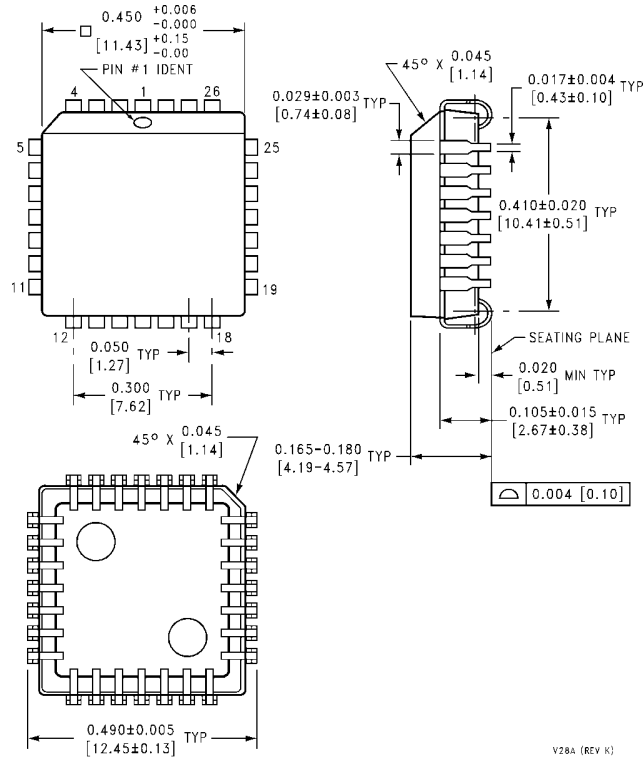
FIGURE 14.

Physical Dimensions inches (millimeters) unless otherwise noted



**28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M28B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Package Number V28A

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