

## 74FR16541

### 16-Bit Buffer/Line Driver with 3-STATE Outputs

#### General Description

The 74FR16541 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is byte controlled. Each byte has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

#### Features

- Non-inverting buffers
- 3-STATE outputs drive bus lines
- Output sink capability of 64 mA, source capability of 15 mA
- Separate 3-STATE control pins for each byte
- Guaranteed multiple output switching, 250 pF delays and pin-to-pin skew
- 16-bit version of the 74F541, 74F244 or 74FR244

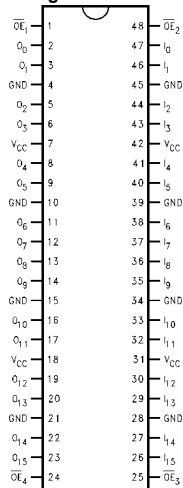
#### Ordering Code:

Order Number	Package Number	Package Description
74FR16541QC	V44A	44-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.650 Square
74FR16541SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide

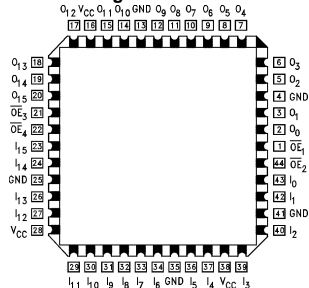
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagrams

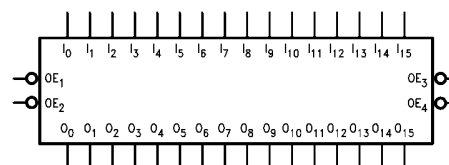
Pin Assignment for SSOP



Pin Assignment for PLCC



#### Logic Symbol



Pin Descriptions

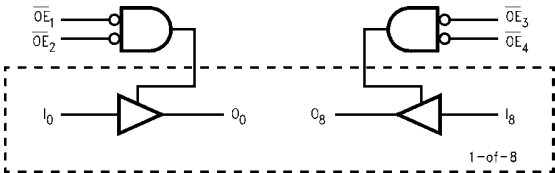
Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	3-STATE Outputs

Truth Table

Inputs						Outputs	
Byte1 [0:7]		Byte2 [8:15]		$I_0-I_7$	$I_8-I_{15}$	$O_0-O_7$	$O_8-O_{15}$
$\overline{OE}_1$	$\overline{OE}_2$	$\overline{OE}_3$	$\overline{OE}_4$				
L	L	L	L	H	H	H	H
H	X	L	L	X	L	Z	L
X	H	L	L	X	H	Z	H
L	L	H	X	L	X	L	Z
L	L	X	H	H	X	H	Z
H	H	H	H	X	X	Z	Z
L	L	L	L	L	L	L	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

Logic Diagram



**Absolute Maximum Ratings**(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
3-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	Twice the Rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4 2.0			V	Min	I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −15 mA
V <sub>OL</sub>	Output LOW Voltage			0.55	V	Min	I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V ( $\overline{OE_n}$ )
I <sub>IL</sub>	Input LOW Current			−120	μA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	−100		−225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>OZH</sub>	Output Leakage Current		0	20	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current		0	−20	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Circuit Leakage Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		35	50	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		92	110	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		36	50	mA	Max	V <sub>O</sub> = HIGH Z
C <sub>IN</sub>	Input Capacitance		8		pF	5.0	

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay I <sub>n</sub> to O <sub>n</sub>	1.5	2.8	4.3	1.5	4.3	ns
t <sub>PHL</sub>		1.5	2.4	4.3	1.5	4.3	
t <sub>PZH</sub>	Output Enable Time	3.6	5.8	11.6	3.6	11.6	ns
t <sub>PZL</sub>		3.6	6.6	11.6	3.6	11.6	
t <sub>PHZ</sub>	Output Disable Time	1.8	4.0	6.6	1.8	6.6	ns
t <sub>PLZ</sub>		1.8	4.1	6.6	1.8	6.6	

## Extended AC Characteristics

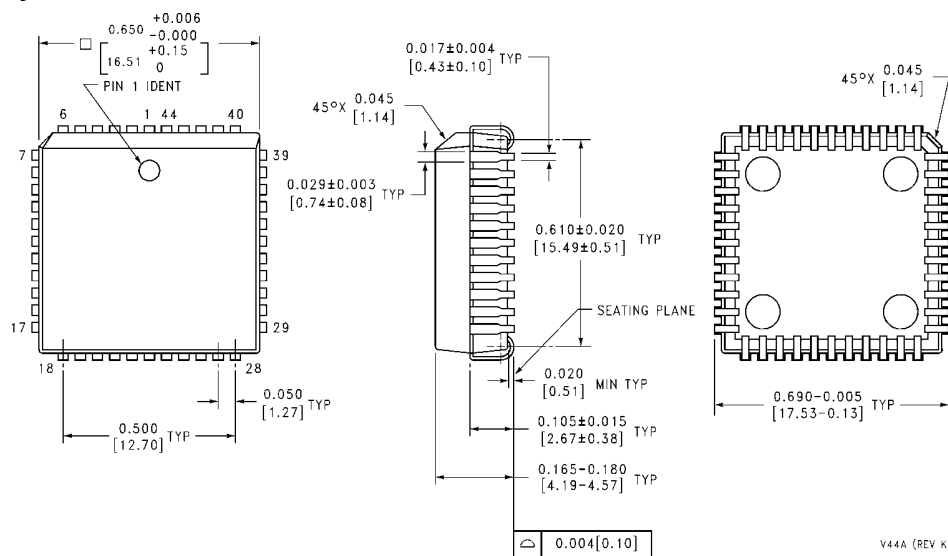
Symbol	Parameter	T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF 16 Outputs Switching (Note 4)		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 250 pF (Note 5)		Units
		Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	1.5	5.7	3.0	9.0	ns
t <sub>PHL</sub>		1.5	5.7	3.0	9.0	
t <sub>PZH</sub>	Output Enable Time	3.6	12.5			ns
t <sub>PZL</sub>		3.6	12.5			
t <sub>PHZ</sub>	Output Disable Time	1.8	6.6			ns
t <sub>PLZ</sub>		1.8	6.6			
t <sub>osHL</sub> (Note 3)	Pin-to-Pin Skew for HL Transitions		1.5			ns
t <sub>osLH</sub> (Note 3)	Pin-to-Pin Skew for LH Transitions		1.3			ns
t <sub>ost</sub> (Note 3)	Pin-to-Pin Skew for HL/LH Transitions		2.0			ns

**Note 3:** Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW, (t<sub>osHL</sub>), LOW-to-HIGH, (t<sub>osLH</sub>), or HIGH-to-LOW and/or LOW-to-HIGH, (t<sub>ost</sub>). Specifications guaranteed with all outputs switching in phase.

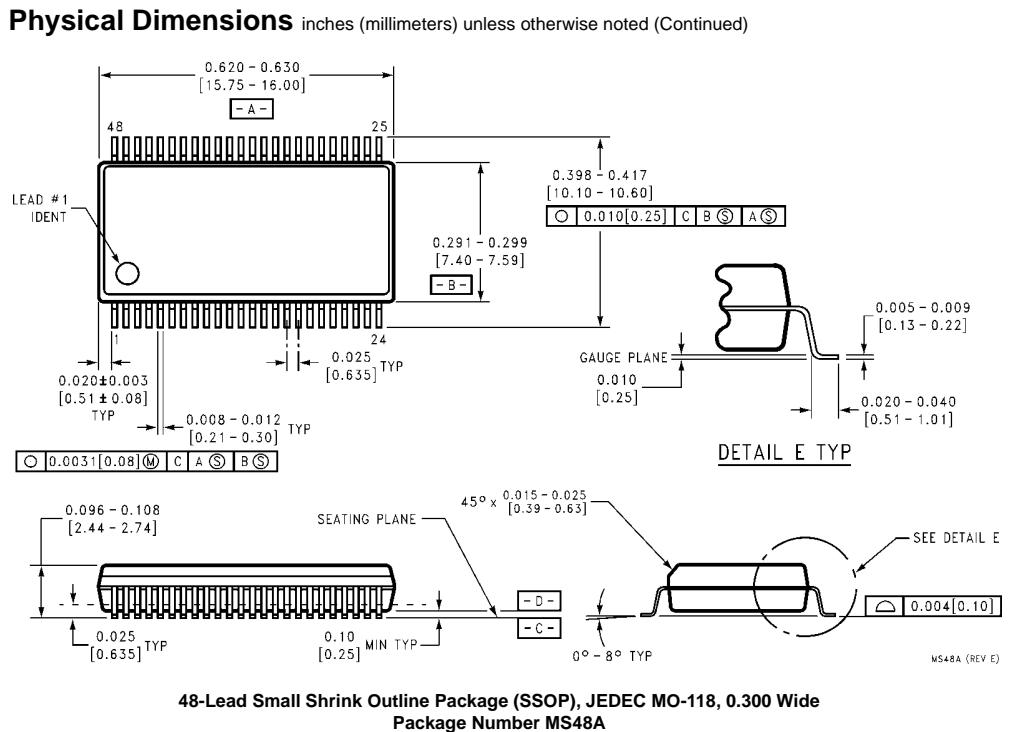
**Note 4:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all LOW-to-HIGH, HIGH-to-LOW, 3-STATE-to-HIGH, etc.

**Note 5:** These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

# Physical Dimensions inches (millimeters) unless otherwise noted



**44-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.650 Square  
Package Number V44A**



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