

May 1992 Revised August 1999

74FR900

9-Bit, 3-Port Latchable Datapath Multiplexer

General Description

The 74FR900 is a data bus multiplexer routing any of three 9-bit ports to any other one of the three ports. Readback of data latched from any port onto itself is also possible. The 74FR900 maintains separate control of all latch-enable, output enable and select inputs for maximum flexibility. PINV allows inversion of the data from the C_8 to A_8 or B_8 path. This is useful for control of the parity bit in systems diagnostics.

Fairchild's 74FR25900 includes 25Ω resistors in series with port A and B outputs. Resistors minimize undershoot and ringing which may damage or corrupt sensitive device inputs driven by these ports.

Features

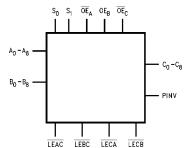
- 9-bit data ports for systems carrying parity bits
- Readback capability for system self checks.
- Independent control lines for maximum flexibility
- Guaranteed multiple output switching and 250 pF load delays
- Outputs optimized for dynamic bus drive capability
- PINV parity control facilitates system diagnostics
- FR25900 resistor option for driving MOS inputs such as DRAM arrays

Ordering Code:

Order Number	Package Number	Package Description
74FR900SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

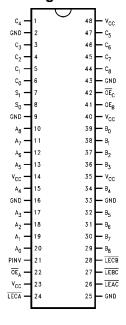
Logic Symbol



Pin Description

Pin Names	Description				
LExx	Latch Enable Inputs				
OE _x	Output Enable Inputs				
PINV	Parity Invert Input				
S ₀ , S ₁	Select Inputs				
$A_0 - A_8$	Port A Inputs or 3-STATE Outputs				
B ₀ -B ₈	Port B Inputs or 3-STATE Outputs				
C ₀ –C ₈	Port C Inputs or 3-STATE Outputs				

Connection Diagram



Functional Description

The 74FR900 allows 9-bit data to be transferred from any of three 9-bit I/O ports to either of the two remaining I/O ports. The device employs latches in all paths for either transparent or synchronous operation. Readback capability from any port to itself is also possible.

Data transfer within the 74FR900 is controlled through use of the select $(S_0$ and $S_1)$ and output-enable $(\overline{OE}_A,\,OE_B$ and $\overline{OE}_C)$ inputs as described in Table 1. Additional control is available by use of the latch-enable inputs $(\overline{LEAC},\,\overline{LECA},\,\overline{LECA},\,\overline{LECB})$ allowing either synchronous or transparent transfers (see Table 2). Table 1 indicates several readback conditions. By latching data on a given port and initiating the readback control configuration, previous data may be read for system verification or diagnostics. This mode may be useful in implementing system diagnostics.

Data at the port to be readback must be latched prior to enabling the outputs on that port. If this is not done, a closed data loop will result causing possible data integrity problems. Note that the A and B ports allow readback without affecting any other port. Port C, however, requires interruption of either port A or B to complete its readback path.

PINV controls inversion of the C_8 bit. A low on PINV allows C_8 data to pass unaltered. A high causes inversion of the data. See Table 3. This feature allows forcing of parity errors for use in system diagnostics. This is particularly helpful in 486 processor designs as the 486 does not provide odd/even parity selection internally.

TABLE 2. Latch-Enable Control

LExx	Input	Output
L	L	L
L	Н	Н
Н	Х	Q_0

L = LOW Voltage

H = HIGH Voltage Level

TABLE 1. Datapath Control

		Inputs	- :		
S ₀	$S_1 \overline{OE}_A \overline{OE}_B \overline{OE}_C$		OE _C	Function	
L	Χ	Н	L	L	Port A to Port C
L	L	Н	Н	Н	Port A to Port B
L	0	Н	Н	L	Port A to B+C
Н	L	L	L	Н	Port B to Port A
Н	Χ	Н	L	L	Port B to Port C
Н	0	L	L	L	Port B to A+C
Х	Н	L	L	Н	Port C to Port A
Χ	Н	Н	Н	Н	Port C to Port B
Χ	Н	L	Н	Н	Port C to A+B
Х	Χ	Н	L	Н	Outputs Disabled
L	L	L	Χ	Χ	(Readback to A) (Note 1)
L	Н	L	Χ	L	(Readback to A or C) (Note 1)
Н	L	Х	Н	X	(Readback to B) (Note 1)
Н	Н	Х	Н	L	(Readback to B or C) (Note 1)

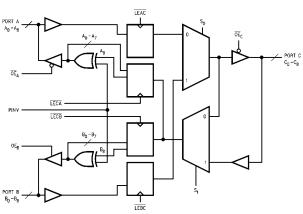
Note 1: Readback operation in latched mode only. Transparent operation could result in unpredictable results.

TABLE 3. PINV Control

PINV	C ₈	A ₈ or B ₈
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

Q₀ = Output state prior to LExx LOW-to-HIGH transition

Logic Diagram



Absolute Maximum Ratings(Note 2)

Storage Temperature -65°C to +150°C Ambient Temperature under Bias -55°C to +125°C

Junction Temperature under Bias -55°C to +150°C V_{CC} Pin Potential to Ground Pin -0.5V to +7.0V Input Voltage (Note 3) -0.5V to +7.0VInput Current (Note 3) $-30\ \text{mA}$ to $+5.0\ \text{mA}$

Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)

Standard Output -0.5 V to $V_{\mbox{\footnotesize CC}}$ 3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA) ESD Last Passing Voltage (Min) 4000V

Recommended Operating Conditions

Free Air Ambient Temperature 0°C to +70°C +4.5V to +5.5V Supply Voltage

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

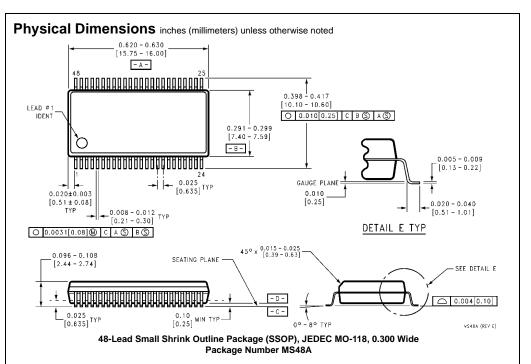
Symbol	Parameter	Min	Тур	Max	Units	v _{cc}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.4			V	Min	$I_{OH} = -3 \text{ mA } (A_n, B_n, C_n)$
		2.0			V	Min	$I_{OH} = -15 \text{ mA } (A_n, B_n, C_n)$
V _{OL}	Output LOW Voltage			0.50	V	Min	$I_{OL} = 24 \text{ mA } (A_n, B_n, C_n)$
I _{IH}	Input HIGH Current			5	μΑ	Max	V _{IN} = 2.7V (Control Inputs)
I _{BVI}	Input HIGH Current Breakdown Test			7	μА	Max	V _{IN} = 7.0V (Control Inputs)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μА	Max	$V_{IN} = 5.5V (A_n, B_n, C_n)$
I _{IL}	Input LOW Current			-150	μΑ	Max	V _{IN} = 0.5V (Control Inputs)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA, All Other Pins Grounded
I _{OD}	Output Circuit Leakage Test			3.75	V	0.0	V _{IOD} = 150 mV, All Other Pins Grounded
I _{IH} + I _{OZH}	Output Leakage Current			25	μА	Max	$V_{OUT} = 2.7V (A_n, B_n, C_n)$
I _{IIL} + I _{OZL}	Output Leakage Current			-150	μА	Max	$V_{OUT} = 0.5V (A_n, B_n, C_n)$
Ios	Output Short Circuit Current	-100		-225	mA	Max	$V_{OUT} = 0.0V (A_n, B_n, C_n)$
I _{CEX}	Output HIGH Leakage Current			50	μА	Max	$V_{OUT} = V_{CC} (A_n, B_n, C_n)$
I _{ZZ}	Bus Drainage Test			100	μА	0.0	$V_{OUT} = 5.25V (A_n, B_n, C_n)$
I _{CCH}	Power Supply Current		115	150	mA	Max	All Outputs HIGH (Note 4)
I _{CCL}	Power Supply Current		170	200	mA	Max	All Outputs LOW (Note 4)
I _{CCZ}	Power Supply Current		147	175	mA	Max	Outputs in 3-STATE

Note 4: 2 ports active only

Symbol	Parameter		$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_A = 0$ °C to +70°C $V_{CC} = +5.0$ V $C_L = 50$ pF	
		Min	Тур	Max	Min	Max	
PLH	Propagation Delay						
PHL	A_n or B_n to C_n	2.0	4.2	7.0	2.0	7.0	ns
	C _n to A _n or B _n						
PLH	Propagation Delay	2.5	4.8	7.5	2.5	7.5	ns
PHL	C ₈ to A ₈ or B ₈ (PINV HIGH)						
PLH	Propagation Delay	4.5	6.4	10.0	4.5	10.0	ns
PHL	A_n to B_n , B_n to A_n						
PLH	Propagation Delay	4.5	6.8	10.0	4.5	10.0	ns
PHL	LEAC to C _n , LEBC to C _n						
PLH	Propagation Delay	3.0	6.0	9.5	3.0	9.5	ns
t _{PHL}	LECA to A _n , LECB to B _n						
t _{PLH}	Propagation Delay	3.0	6.0	10.0	3.0	10.0	ns
t _{PHL}	S ₀ to C _n						
t _{PLH}	Propagation Delay	3.5	6.5	11.0	3.5	11.0	ns
t _{PHL}	S ₁ to A _n or B _n						
t _{PLH}	Propagation Delay	2.0	5.0	9.0	2.0	9.0	ns
t _{PHL}	PINV to A ₈ or B ₈						
t _{PZH}	Output Enable Time	2.0	4.0	6.5	2.0	6.5	ns
t _{PZL}	A _n , C _n						
t _{PHZ}	Output Disable Time	1.5	4.0	6.0	1.5	6.0	ns
t _{PLZ}	A _n , C _n						
t _{PZH}	Output Enable Time	2.0	5.0	7.0	2.0	7.0	ns
t _{PZL}	B _n						
t _{PHZ}	Output Disable Time B _n	2.0	5.0	7.0	2.0	7.0	ns
			1				
AC O	perating Requirements		T			7000	l
AC O	perating Requirements		T _A = +25°C			to +70°C	
AC O	perating Requirements		V _{CC} = +5.0\	/	V _{CC} =	= +5.0V	Unit
			V _{CC} = +5.0\ C _L = 50 pF		V _{CC} =	+5.0V 50 pF	Unit
Symbol	Parameter	Min	V _{CC} = +5.0\	/	V _{CC} =	= +5.0V	Unit
Symbol $t_S(H)$	Parameter Setup Time, HIGH or LOW		V _{CC} = +5.0\ C _L = 50 pF		V _{CC} =	+5.0V 50 pF	
Symbol t _S (H)	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC	Min 4.0	V _{CC} = +5.0\ C _L = 50 pF		V _{CC} =	+5.0V 50 pF	Unit
Symbol t _S (H) t _S (L) t _H (H)	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC Hold Time, HIGH or LOW	4.0	V _{CC} = +5.0\ C _L = 50 pF Typ 2.0		V _{CC} = C _L = Min 4.0	+5.0V 50 pF	ns
Symbol t _S (H) t _S (L) t _H (H)	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC Hold Time, HIGH or LOW A _n to LEAC, B _n to LEBC		V _{CC} = +5.0\ C _L = 50 pF		V _{CC} =	+5.0V 50 pF	
Symbol is(H) is(L) it _H (H) it _H (L)	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC Hold Time, HIGH or LOW	1.0	V _{CC} = +5.0\ C _L = 50 pF Typ 2.0		V _{CC} = C _L = Min 4.0	+5.0V 50 pF	ns
$\begin{array}{c} \textbf{Symbol} \\ \\ t_S(\textbf{H}) \\ t_S(\textbf{L}) \\ \\ t_H(\textbf{H}) \\ \\ t_H(\textbf{L}) \\ \\ t_S(\textbf{H}) \\ \\ t_S(\textbf{L}) \end{array}$	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC Hold Time, HIGH or LOW A _n to LEAC, B _n to LEBC Setup Time, HIGH or LOW C _n to LECA or LECB	4.0	V _{CC} = +5.0\ C _L = 50 pF Typ 2.0		V _{CC} = C _L = Min 4.0	+5.0V 50 pF	ns
Symbol ts(H) ts(L) tH(H) tH(L) ts(H)	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC Hold Time, HIGH or LOW A _n to LEAC, B _n to LEBC Setup Time, HIGH or LOW	4.0 1.0 3.0	$V_{CC} = +5.0 \text{ N}$ $C_L = 50 \text{ pF}$ Typ 2.0 -2.0		V _{CC} = C _L = Min 4.0 1.0 3.0	+5.0V 50 pF	ns ns
Symbol S(H) S(L) H(H) S(L) S(H) S(L) H(H)	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC Hold Time, HIGH or LOW A _n to LEAC, B _n to LEBC Setup Time, HIGH or LOW C _n to LECA or LECB	1.0	V _{CC} = +5.0\ C _L = 50 pF Typ 2.0		V _{CC} = C _L = Min 4.0	+5.0V 50 pF	ns
Symbol S(H) S(L) H(H) S(L) H(L) S(H) S(H) S(H) H(L) H(H) H(L)	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC Hold Time, HIGH or LOW A _n to LEAC, B _n to LEBC Setup Time, HIGH or LOW C _n to LECA or LECB Hold Time, HIGH or LOW	4.0 1.0 3.0	$V_{CC} = +5.0 \text{ N}$ $C_L = 50 \text{ pF}$ Typ 2.0 -2.0		V _{CC} = C _L = Min 4.0 1.0 3.0	+5.0V 50 pF	ns ns
$\begin{array}{c} \textbf{Symbol} \\ \\ S(H) \\ S(L) \\ H(H) \\ H(L) \\ S(H) \\ S(L) \\ H(H) \\ H(L) \\ H(H) \\ H(L) \\ M(H) \end{array}$	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC Hold Time, HIGH or LOW A _n to LEAC, B _n to LEBC Setup Time, HIGH or LOW C _n to LECA or LECB Hold Time, HIGH or LOW C _n to LECA or LECB	4.0 1.0 3.0 1.0 8.0	$V_{CC} = +5.0$ \ $C_L = 50 \text{ pF}$ Typ 2.0 -2.0 1.0		V _{CC} = C _L = Min 4.0 1.0 3.0	+5.0V 50 pF	ns ns
Symbol (S(H) (S(L) (H(H) (H(L) (S(H) (S(L) (H(H) (H(L) (S(H) (H(H) (H(H) (H(L) (H(H) (H(L) (H(H) (H(L) (H(H) (H(H	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC Hold Time, HIGH or LOW A _n to LEAC, B _n to LEBC Setup Time, HIGH or LOW C _n to LECA or LECB Hold Time, HIGH or LOW C _n to LECA or LECB TECB Hold Time, HIGH or LOW C _n to LECA or LECB	4.0 1.0 3.0 1.0 8.0	$V_{CC} = +5.0$ \ $C_L = 50 \text{ pF}$ Typ 2.0 -2.0 1.0 4.0	Max	V _{CC} = C _L = Min 4.0 1.0 3.0 1.0 8.0	= +5.0V 50 pF Max	ns ns
Symbol (S(H) (S(L) (H(H) (H(L) (S(H) (S(L) (H(H) (H(L) (S(H) (H(H) (H(H) (H(L) (H(H) (H(L) (H(H) (H(L) (H(H) (H(H	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC Hold Time, HIGH or LOW A _n to LEAC, B _n to LEBC Setup Time, HIGH or LOW C _n to LECA or LECB Hold Time, HIGH or LOW C _n to LECA or LECB TECB Hold Time, HIGH or LOW C _n to LECA or LECB	4.0 1.0 3.0 1.0 8.0	$V_{CC} = +5.0$ \ $C_L = 50 \text{ pF}$ Typ 2.0 -2.0 1.0 -1.0 4.0	Max Max to +70°C	V _{CC} = C _L = Min 4.0 1.0 3.0 1.0 8.0	= +5.0V 50 pF Max	ns ns
Symbol S(H) S(L) H(H) S(L) S(H) S(L) H(H) S(L) H(H) H(L) S(H) S(L)	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC Hold Time, HIGH or LOW A _n to LEAC, B _n to LEBC Setup Time, HIGH or LOW C _n to LECA or LECB Hold Time, HIGH or LOW C _n to LECA or LECB TECB Hold Time, HIGH or LOW C _n to LECA or LECB	4.0 1.0 3.0 1.0 8.0	$V_{CC} = +5.0V$ $C_{L} = 50 \text{ pF}$ Typ 2.0 -2.0 1.0 -1.0 4.0 $T_{A} = 0^{\circ}C$ $V_{CC} = -1.0$	Max Max to +70°C +5.0V	V _{CC} = C _L = Min 4.0 1.0 3.0 1.0 8.0 V _{CC} =	= +5.0V 50 pF Max Max : to +70°C = +5.0V	ns ns
Symbol (S(H) (S(L) (H(H) (H(L) (S(H) (S(L) (H(H) (H(L) (S(H) (H(H) (H(H) (H(L) (H(H) (H(L) (H(H) (H(L) (H(H) (H(H	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC Hold Time, HIGH or LOW A _n to LEAC, B _n to LEBC Setup Time, HIGH or LOW C _n to LECA or LECB Hold Time, HIGH or LOW C _n to LECA or LECB TECB Hold Time, HIGH or LOW C _n to LECA or LECB	4.0 1.0 3.0 1.0 8.0	$V_{CC} = +5.0V$ $C_{L} = 50 \text{ pF}$ Typ 2.0 -2.0 1.0 -1.0 4.0 $V_{CC} = C_{L}$	Max Max to +70°C +5.0V 50 pF	V _{CC} = C _L = Min 4.0 1.0 3.0 1.0 8.0 V _{CC} = C _L = :	= +5.0V 50 pF Max 	ns ns ns ns
Symbol S(H) S(L) H(H) H(L) S(L) H(H) H(L) S(L) H(H) H(L) S(H) H(L) H(L) H(L) H(L) H(L) H(L) H(L) H	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC Hold Time, HIGH or LOW A _n to LEAC, B _n to LEBC Setup Time, HIGH or LOW C _n to LECA or LECB Hold Time, HIGH or LOW C _n to LECA or LECB TE Pulse Width LOW ded AC Electrical Chara	4.0 1.0 3.0 1.0 8.0	V _{CC} = +5.0\ C _L = 50 pF Typ 2.0 -2.0 1.0 -1.0 4.0 T _A = 0°C V _{CC} = C _L = Nine Output	Max to +70°C +5.0V 50 pF ts Switching	V _{CC} = C _L = Min 4.0 1.0 3.0 1.0 8.0 V _{CC} = C _L = :	= +5.0V 50 pF Max Max : to +70°C = +5.0V	ns ns
Symbol ts(H) ts(L) tt _H (H) tt _H (L) ts(H) ts(L) tt _H (H) ts(L) tt _H (H) tt _H (L) tt _H (H) tt _H (L)	Parameter Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC Hold Time, HIGH or LOW A _n to LEAC, B _n to LEBC Setup Time, HIGH or LOW C _n to LECA or LECB Hold Time, HIGH or LOW C _n to LECA or LECB TE Pulse Width LOW ded AC Electrical Chara	4.0 1.0 3.0 1.0 8.0	V _{CC} = +5.0\ C _L = 50 pF Typ 2.0 -2.0 1.0 -1.0 4.0 T _A = 0°C V _{CC} = C _L = Nine Output	Max Max to +70°C +5.0V 50 pF	V _{CC} = C _L = Min 4.0 1.0 3.0 1.0 8.0 V _{CC} = C _L = :	= +5.0V 50 pF Max 	ns ns ns ns

Extended AC Electrical Characteristics (Continued)

		T _A = 0°C	to +70°C	T _A = 0°C to +70°C		
			V _{CC} = +5.0V		V _{CC} = +5.0V	
		•••				
Symbol	Parameter	-	C _L = 50 pF		C _L = 250 pF	
		Nine Outputs Switching (Note 5)		(Note 6)		
		Min	Max	Min	Max	
t _{PHL}	A_n or B_n to C_n	2.0	9.0	2.5	10.5	ns
	C_n to A_n or B_n					
t _{PLH}	Propagation Delay			3.5	11.0	ns
t_{PHL}	C ₈ to A ₈ or B ₈ (PINV HIGH)			5.5	11.0	113
t _{PLH}	Propagation Delay	4.5	12.0	5.5	13.5	ns
t _{PHL}	A_n to B_n , B_n to A_n	4.5	12.0	5.5	15.5	113
t _{PLH}	Propagation Delay	4.5	12.0	5.5	13.5	ns
t_{PHL}	LEAC to C _n , LEBC to C _n	4.5	12.0	5.5	13.3	115
t _{PLH}	Propagation Delay	3.0	11.5	4.0	40.5	
t _{PHL}	LECA to A _n , LECB to B _n	3.0	11.5	4.0	13.5	ns
t _{PLH}	Propagation Delay	3.0	11.0	3.0	14.0	ns
t _{PHL}	S ₀ to C _n	3.0	11.0	5.0	14.0	113
t _{PLH}	Propagation Delay	3.5	12.0	4.5	15.0	ns
t _{PHL}	S ₁ to A _n or B _n	3.3	12.0	4.5	13.0	115
t _{PLH}	Propagation Delay			2.5	12.0	ns
t _{PHL}	PINV to A ₈ or B ₈			2.5	12.0	115
t _{PZH}	Output Enable Time	2.0	8.0			ns
t_{PZL}	A_n, C_n	2.0	0.0			115
t _{PHZ}	Output Disable Time	1.5	6.0			ns
t_{PLZ}	A _n , C _n	1.5	6.0			115
t _{PZH}	Output Enable Time	2.0	8.0			nc
t_{PZL}	B _n	2.0	0.0			ns
t _{PHZ}	Output Disable Time	2.0	7.0			ns
t _{PLZ}	B _n	2.0	7.0			115



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- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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