FAIRCHILD SEMICONDUCTOR™

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# 74LCX16373

# Low Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

## General Description

The LCX16373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state.

The LCX16373 is designed for low voltage (2.5V or 3.3V) $V_{CC}$ applications with capability of interfacing to a 5V signal environment.

The LCX16373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

## Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V $V_{CC}$ specifications provided
- 5.4 ns $t_{PD}$ max ($V_{CC}$ = 3.3V), 20 µA $I_{CC}$ max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA output drive ($V_{CC}$ = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

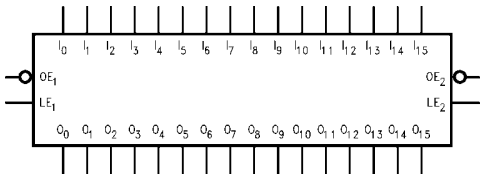
**Note 1:** To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to $V_{CC}$ through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 74LCX16373MEA | MS48A | 48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide |
| 74LCX16373MTD | MTD48 | 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Logic Symbol

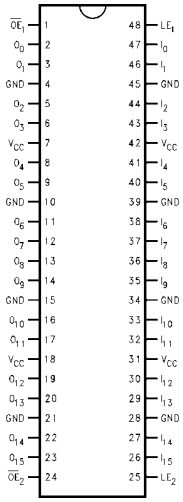



## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{OE}_n$ | Output Enable Input (Active LOW) |
| $LE_n$ | Latch Enable Input |
| $I_0$–$I_{15}$ | Inputs |
| $O_0$–$O_{15}$ | Outputs |

## Connection Diagram




## Truth Tables

| Inputs | | | Outputs |
|---|---|---|---|
| $LE_1$ | $\overline{OE}_1$ | $I_0$–$I_7$ | $O_0$–$O_7$ |
| X | H | X | Z |
| H | L | L | L |
| H | L | H | H |
| L | L | X | $O_0$ |

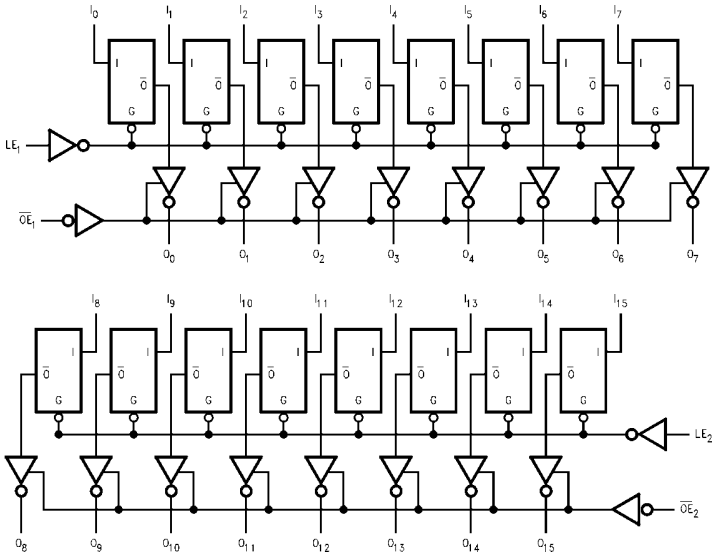
| Inputs | | | Outputs |
|---|---|---|---|
| $LE_2$ | $\overline{OE}_2$ | $I_8$–$I_{15}$ | $O_8$–$O_{15}$ |
| X | H | X | Z |
| H | L | L | L |
| H | L | H | H |
| L | L | X | $O_0$ |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
$O_0$ = Previous $O_0$ before HIGH-to-LOW transition of Latch Enable

## Functional Description

The LCX16373 contains sixteen D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable ($LE_n$) input is HIGH, data on the $I_n$ enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its I input changes. When $LE_n$ is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition of $LE_n$. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

## Logic Diagrams




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings(Note 2)

| Symbol | Parameter | Value | Conditions | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | −0.5 to +7.0 | | V |
| $V_I$ | DC Input Voltage | −0.5 to +7.0 | | V |
| $V_O$ | DC Output Voltage | −0.5 to +7.0<br>−0.5 to $V_{CC}$ + 0.5 | Output in 3-STATE<br>Output in HIGH or LOW State (Note 3) | V |
| $I_{IK}$ | DC Input Diode Current | −50 | $V_I$ < GND | mA |
| $I_{OK}$ | DC Output Diode Current | −50<br>+50 | $V_O$ < GND<br>$V_O$ > $V_{CC}$ | mA |
| $I_O$ | DC Output Source/Sink Current | ±50 | | mA |
| $I_{CC}$ | DC Supply Current per Supply Pin | ±100 | | mA |
| $I_{GND}$ | DC Ground Current per Ground Pin | ±100 | | mA |
| $T_{STG}$ | Storage Temperature | −65 to +150 | | °C |

## Recommended Operating Conditions (Note 4)

| Symbol | Parameter | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Operating | 2.0 | 3.6 | V |
| | | Data Retention | 1.5 | 3.6 | |
| $V_I$ | Input Voltage | | 0 | 5.5 | V |
| $V_O$ | Output Voltage | HIGH or LOW State | 0 | $V_{CC}$ | V |
| | | 3-STATE | 0 | 5.5 | |
| $I_{OH}/I_{OL}$ | Output Current | $V_{CC}$ = 3.0V − 3.6V | | ±24 | mA |
| | | $V_{CC}$ = 2.7V − 3.0V | | ±12 | |
| | | $V_{CC}$ = 2.3V − 2.7V | | ±8 | |
| $T_A$ | Free-Air Operating Temperature | | −40 | 85 | °C |
| $\Delta t/\Delta V$ | Input Edge Rate, $V_{IN}$ = 0.8V–2.0V, $V_{CC}$ = 3.0V | | 0 | 10 | ns/V |

**Note 2:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:** $I_O$ Absolute Maximum Rating must be observed.

**Note 4:** Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = −40°C to +85°C | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage | | 2.3 – 2.7 | 1.7 | | V |
| | | | 2.7 – 3.6 | 2.0 | | |
| $V_{IL}$ | LOW Level Input Voltage | | 2.3 – 2.7 | | 0.7 | V |
| | | | 2.7 – 3.6 | | 0.8 | |
| $V_{OH}$ | HIGH Level Output Voltage | $I_{OH}$ = −100 µA | 2.3 – 3.6 | $V_{CC}$ − 0.2 | | V |
| | | $I_{OH}$ = 8 mA | 2.3 | 1.8 | | |
| | | $I_{OH}$ = −12 mA | 2.7 | 2.2 | | |
| | | $I_{OH}$ = −18 mA | 3.0 | 2.4 | | |
| | | $I_{OH}$ = −24 mA | 3.0 | 2.2 | | |
| $V_{OL}$ | LOW Level Output Voltage | $I_{OL}$ = 100 µA | 2.3 – 3.6 | | 0.2 | V |
| | | $I_{OL}$ = 8 mA | 2.3 | | 0.6 | |
| | | $I_{OL}$ = 12 mA | 2.7 | | 0.4 | |
| | | $I_{OL}$ = 16 mA | 3.0 | | 0.4 | |
| | | $I_{OL}$ = 24 mA | 3.0 | | 0.55 | |
| $I_I$ | Input Leakage Current | 0 ≤ $V_I$ ≤ 5.5V | 2.3 – 3.6 | | ±5.0 | µA |
| $I_{OZ}$ | 3-STATE Output Leakage | 0 ≤ $V_O$ ≤ 5.5V<br>$V_I$ = $V_{IH}$ or $V_{IL}$ | 2.3 – 3.6 | | ±5.0 | µA |
| $I_{OFF}$ | Power-Off Leakage Current | $V_I$ or $V_O$ = 5.5V | 0 | | 10 | µA |

## DC Electrical Characteristics (Continued)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = -40°C$ to $+85°C$ | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $I_{CC}$ | Quiescent Supply Current | $V_I = V_{CC}$ or GND | 2.3 – 3.6 | | 20 | μA |
| | | $3.6V \le V_I$, $V_O \le 5.5V$ (Note 5) | 2.3 – 3.6 | | ±20 | |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | $V_{IH} = V_{CC} - 0.6V$ | 2.3 – 3.6 | | 500 | μA |

**Note 5:** Outputs disabled or 3-STATE only.

## AC Electrical Characteristics

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$ | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | $V_{CC} = 3.3V \pm 0.3V$ | | $V_{CC} = 2.7V$ | | $V_{CC} = 2.5V \pm 0.2V$ | | |
| | | $C_L = 50$ pF | | $C_L = 50$ pF | | $C_L = 30$ pF | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{PHL}$ | Propagation Delay | 1.5 | 5.4 | 1.5 | 5.9 | 1.5 | 6.5 | ns |
| $t_{PLH}$ | $I_n$ to $O_n$ | 1.5 | 5.4 | 1.5 | 5.9 | 1.5 | 6.5 | |
| $t_{PHL}$ | Propagation Delay | 1.5 | 5.5 | 1.5 | 6.4 | 1.5 | 6.6 | ns |
| $t_{PLH}$ | LE to $O_n$ | 1.5 | 5.5 | 1.5 | 6.4 | 1.5 | 6.6 | |
| $t_{PZL}$ | Output Enable Time | 1.5 | 6.1 | 1.5 | 6.5 | 1.5 | 7.9 | ns |
| $t_{PZH}$ | | 1.5 | 6.1 | 1.5 | 6.5 | 1.5 | 7.9 | |
| $t_{PLZ}$ | Output Disable Time | 1.5 | 6.0 | 1.5 | 6.3 | 1.5 | 7.2 | ns |
| $t_{PHZ}$ | | 1.5 | 6.0 | 1.5 | 6.3 | 1.5 | 7.2 | |
| $t_S$ | Setup Time, $I_n$ to LE | 2.5 | | 2.5 | | 3.0 | | ns |
| $t_H$ | Hold Time, $I_n$ to LE | 1.5 | | 1.5 | | 2.0 | | ns |
| $t_W$ | LE Pulse Width | 3.0 | | 3.0 | | 3.5 | | ns |
| $t_{OSHL}$ | Output to Output Skew (Note 6) | | 1.0 | | | | | ns |
| $t_{OSLH}$ | | | 1.0 | | | | | |

**Note 6:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$). Parameter guaranteed by design.

## Dynamic Switching Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = 25°C$ | Units |
|---|---|---|---|---|---|
| | | | | Typical | |
| $V_{OLP}$ | Quiet Output Dynamic Peak $V_{OL}$ | $C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | 3.3 | 0.8 | V |
| | | $C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$ | 2.5 | 0.6 | |
| $V_{OLV}$ | Quiet Output Dynamic Valley $V_{OL}$ | $C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | 3.3 | −0.8 | V |
| | | $C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$ | 2.5 | −0.6 | |

## Capacitance

| Symbol | Parameter | Conditions | Typical | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = Open, $V_I = 0V$ or $V_{CC}$ | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$ | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$, f = 10 MHz | 20 | pF |

## AC LOADING and WAVEFORMS Generic for LCX Family

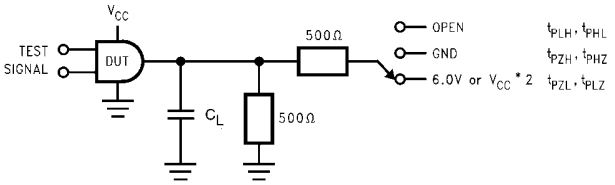
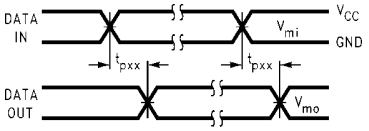
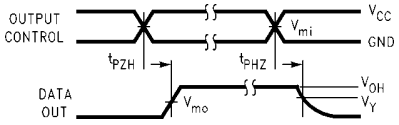



**FIGURE 1. AC Test Circuit ($C_L$ includes probe and jig capacitance)**

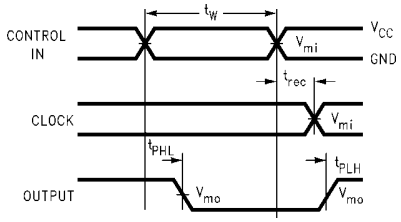
| Test | Switch |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | 6V at $V_{CC}$ = 3.3 ± 0.3V<br>$V_{CC}$ x 2 at $V_{CC}$ = 2.5 ± 0.2V |
| $t_{PZH}$,$t_{PHZ}$ | GND |



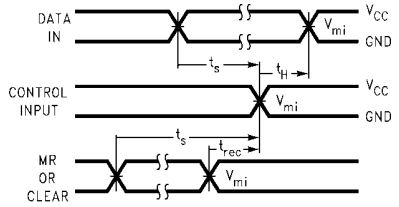

**Waveform for Inverting and Non-Inverting Functions**



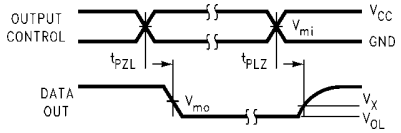

**3-STATE Output High Enable and Disable Times for Logic**



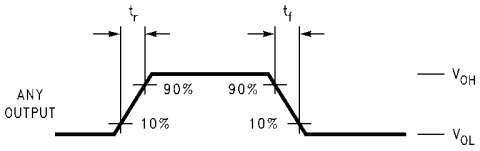

**Propagation Delay. Pulse Width and $t_{rec}$ Waveforms**




**Setup Time, Hold Time and Recovery Time for Logic**




**3-STATE Output Low Enable and Disable Times for Logic**

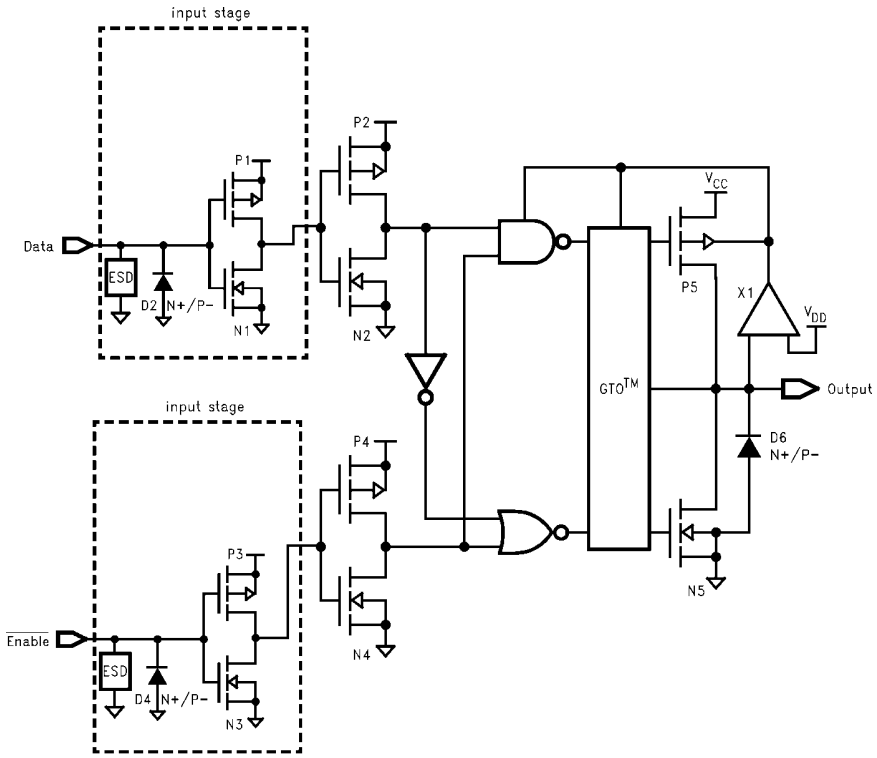



**$t_{rise}$ and $t_{fall}$**

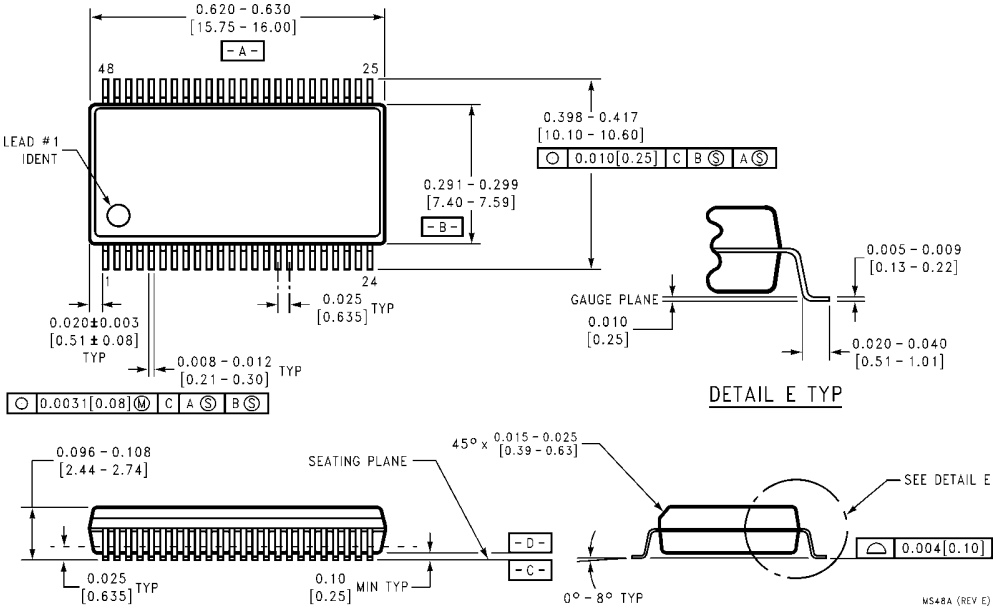
**FIGURE 2. Waveforms**
**(Input Characteristics; f =1MHz, $t_R$ = $t_F$ = 3ns)**

| Symbol | $V_{CC}$ | | |
|---|---|---|---|
| | **3.3V ± 0.3V** | **2.7V** | **2.5V ± 0.2V** |
| $V_{mi}$ | 1.5V | 1.5V | $V_{CC}$/2 |
| $V_{mo}$ | 1.5V | 1.5V | $V_{CC}$/2 |
| $V_x$ | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.15V |
| $V_y$ | $V_{OH}$ − 0.3V | $V_{OH}$ − 0.3V | $V_{OH}$ − 0.15V |

## Schematic Diagram Generic for LCX Family

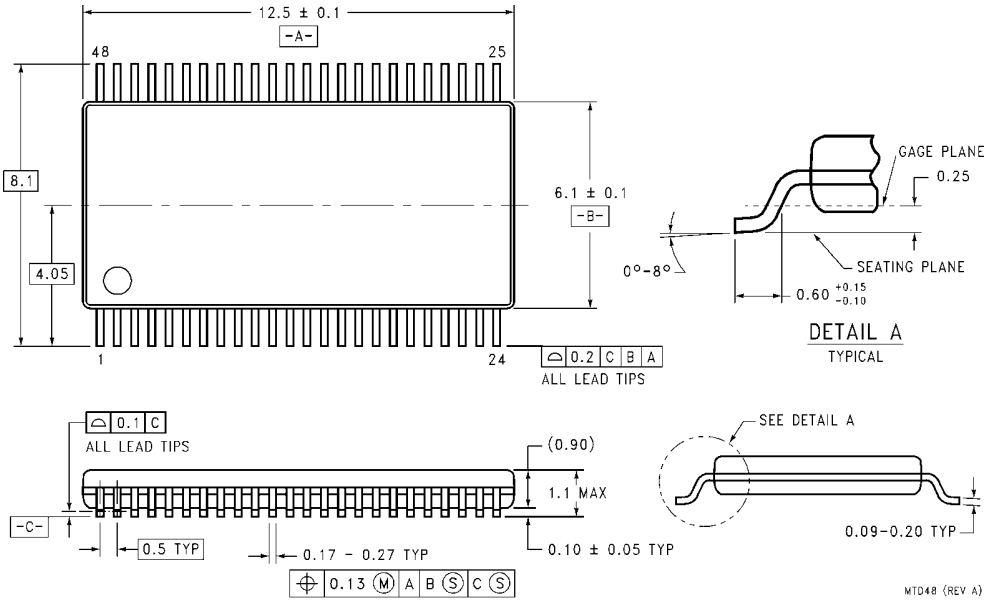


## Physical Dimensions inches (millimeters) unless otherwise noted




**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide**
**Package Number MS48A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide**
**Package Number MTD48**

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