FAIRCHILD

SEMICONDUCTOR™

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74LCX543
Low Voltage Octal Registered Transceiver with 5V Tolerant Inputs and Outputs

General Description

The LCX543 is a non-inverting octal transceiver containing two sets of D-type registers for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow.

The LCX543 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX543 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

■ 5V tolerant inputs and outputs

■ 2.3V – 3.6V V_{CC} specifications provided

■ 7.0 ns t_{PD} max (V_{CC} = 3.3V), 10 µA I_{CC} max

■ Power down high impedance inputs and outputs

■ Supports live insertion/withdrawal (Note 1)

■ ±24 mA Output Drive (V_{CC} = 3.0V)

■ Implements patented noise/EMI reduction circuitry

■ Latch-up performance exceeds 500 mA

■ ESD performance:
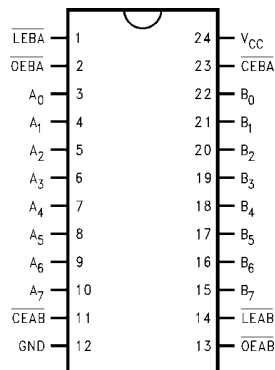   Human body model > 2000V
   Machine model > 200V

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74LCX543WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX543MSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LCX543MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

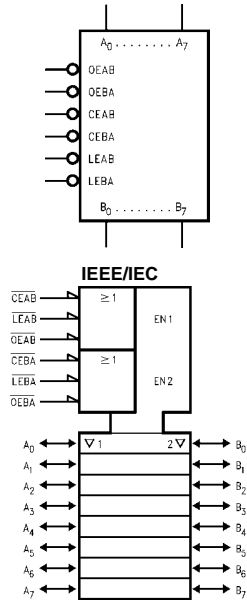Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

$\overline{LEBA}$	1	24	V_{CC}
$\overline{OEBA}$	2	23	$\overline{CEBA}$
A_0	3	22	B_0
A_1	4	21	B_1
A_2	5	20	B_2
A_3	6	19	B_3
A_4	7	18	B_4
A_5	8	17	B_5
A_6	9	16	B_6
A_7	10	15	B_7
$\overline{CEAB}$	11	14	$\overline{LEAB}$
GND	12	13	$\overline{OEAB}$

Pin Descriptions

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or
	B-to-A 3-STATE Outputs
B_0–B_7	B-to-A Data Inputs or
	A-to-B 3-STATE Outputs

DS012463.prf

Logic Symbols

A_0 . . . . A_7
OEAB
OEBA
CEAB
CEBA
LEAB
LEBA
B_0 . . . . B_7

IEEE/IEC

$\overline{CEAB}$ ≥1 EN1
$\overline{LEAB}$
$\overline{OEAB}$
$\overline{CEBA}$ ≥1 EN2
$\overline{LEBA}$
$\overline{OEBA}$

A_0 ▽1 2▽ B_0
A_1 B_1
A_2 B_2
A_3 B_3
A_4 B_4
A_5 B_5
A_6 B_6
A_7 B_7

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

Functional Description

The LCX543 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0–A_7 or take data from B_0–B_7, as indicated in the Data I/O Control Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Logic Diagram

DETAIL A
D Q
LE B_0
A_0
Q D
LE

A_1 B_1
A_2 B_2
A_3 B_3
A_4 DETAIL A x 7 B_4
A_5 B_5
A_6 B_6
A_7 B_7

$\overline{OEBA}$
$\overline{OEAB}$
$\overline{CEBA}$
$\overline{CEAB}$
$\overline{LEBA}$
$\overline{LEAB}$
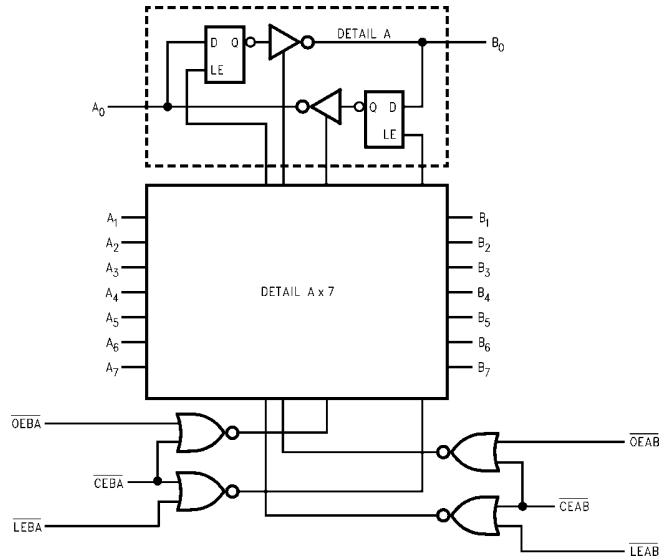
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 3)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 4)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V		±24	mA
		V_{CC} = 2.7V − 3.0V		±12	
		V_{CC} = 2.3V − 2.7V		±8	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V − 2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Unused inputs or I/O's must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.3 – 3.6	V_{CC} − 0.2		V
		I_{OH} = −8 mA	2.3	1.8		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.3 – 3.6		0.2	V
		I_{OL} = 8mA	2.3		0.6	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.3 – 3.6		±5.0	μA
I_{OZ}	3-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V	2.3 – 3.6		±5.0	μA
		V_I = V_{IH} or V_{IL}				
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_CC (V)	T_A = −40°C to +85°C		Units
				Min	Max	
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.3 – 3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V (Note 5)	2.3 – 3.6		±10	
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.3 – 3.6		500	μA

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	T_A = −40°C to +85°C, R_L = 500Ω						Units
		V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V		V_{CC} = 2.5V ± 0.2V		
		C_L = 50 pF		C_L = 50 pF		C_L = 30 pF		
		Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	7.0	1.5	8.0	1.5	8.4	ns
t_{PLH}	A_n to B_n or B_n to A_n	1.5	7.0	1.5	8.0	1.5	8.4	
t_{PHL}	Propagation Delay	1.5	8.5	1.5	9.5	1.5	10.5	ns
t_{PLH}	$\overline{LEBA}$ to A_n or $\overline{LEAB}$ to B_n	1.5	8.5	1.5	9.5	1.5	10.5	
t_{PZL}	Output Enable Time	1.5	9.0	1.5	10.0	1.5	11.0	ns
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.5	9.0	1.5	10.0	1.5	11.0	
	$\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n							
t_{PLZ}	Output Disable Time	1.5	7.0	1.5	7.5	1.5	8.4	ns
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.5	7.0	1.5	7.5	1.5	8.4	
	$\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n							
t_S	Setup Time, HIGH or LOW Data to $\overline{LEXX}$	2.5		2.5		4.0		ns
t_H	Hold Time, HIGH or LOW Data to $\overline{LEXX}$	1.5		1.5		2.0		ns
t_W	Pulse Width, Latch Enable, LOW	3.3		3.3		3.3		ns
t_{OSHL}	Output to Output Skew		1.0					ns
t_{OSLH}	(Note 6)		1.0					

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_CC (V)	T_A = 25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V
		C_L = 30 pF, V_{IH} = 2.5V, V_{IL} = 0V	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	−0.8	V
		C_L = 30 pF, V_{IH} = 2.5V, V_{IL} = 0V	2.5	−0.6	

Capacitance

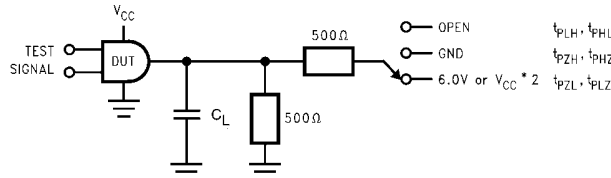| Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, f = 10 MHz	25	pF

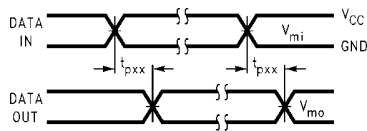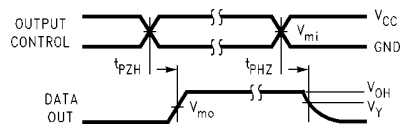# AC LOADING and WAVEFORMS Generic for LCX Family

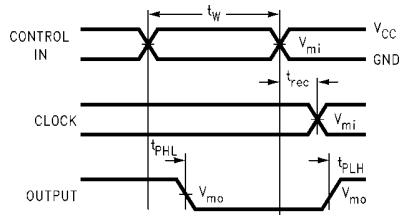

FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

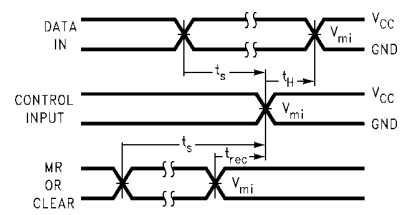| Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ V_{CC} x 2 at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH}, t_{PHZ}	GND

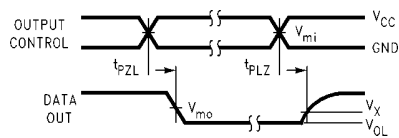**Waveform for Inverting and Non-Inverting Functions**

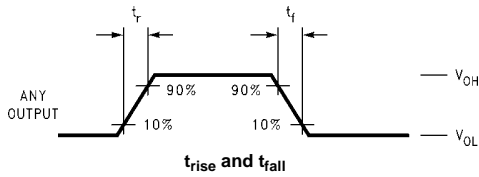**3-STATE Output High Enable and Disable Times for Logic**

Propagation Delay. Pulse Width and t_{rec} Waveforms

Setup Time, Hold Time and Recovery Time for Logic
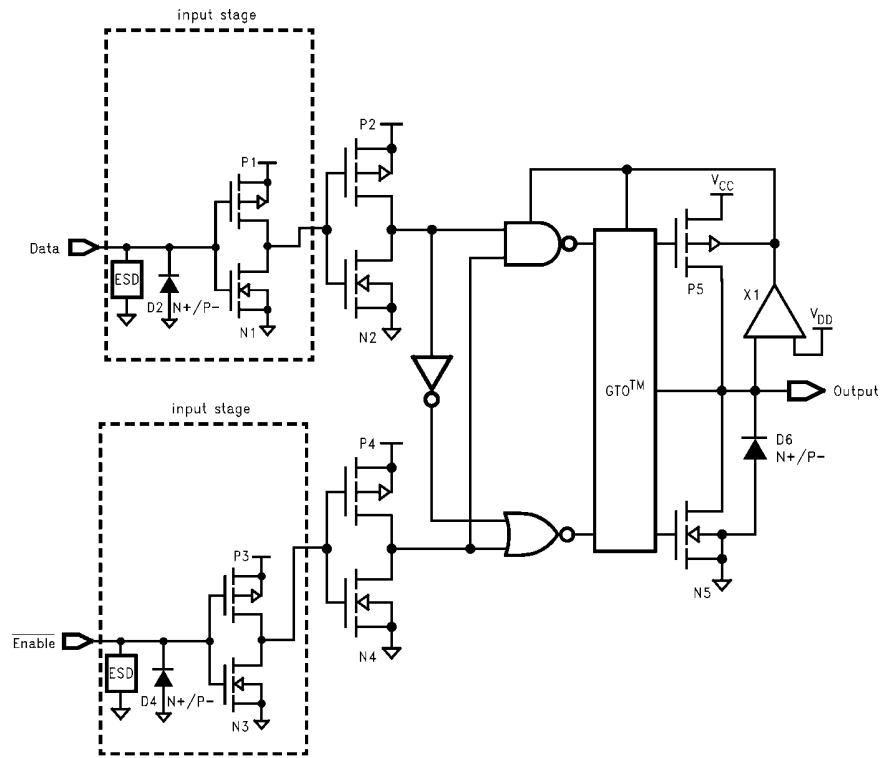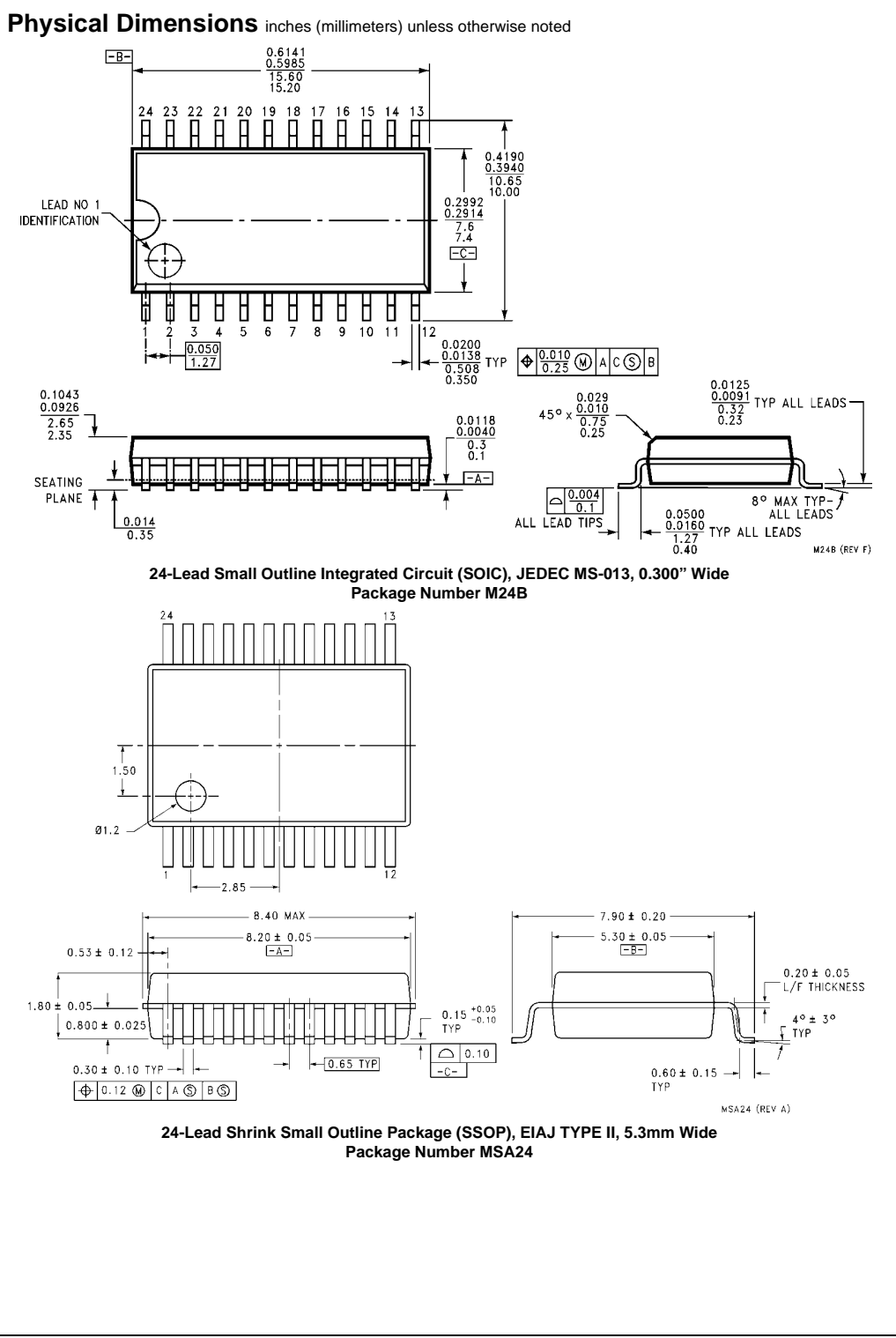

3-STATE Output Low Enable and Disable Times for Logic

t_{rise} and t_{fall}

FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, $t_R = t_F$ = 3ns)

Symbol	V_{CC}		
	3.3V $\pm$ 0.3V	2.7V	2.5V $\pm$ 0.2V
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram Generic for LCX Family

Physical Dimensions inches (millimeters) unless otherwise noted

24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M24B

24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

LAND PATTERN RECOMMENDATION

7.72

4.16

(1.78 TYP)

0.42 TYP

0.65 TYP

7.8 ± 0.1

−A−

24   13

6.4

3.2

4.4 ± 0.1

−B−

1   12

0.2 | C | B | A
ALL LEAD TIPS

0.1 | C
ALL LEAD TIPS

−C−

0.65 TYP

0.19 − 0.30 TYP

0.13 (M) | A | B (S) | C (S)

(0.90)

1.1 MAX

0.10 ± 0.05 TYP

GAGE PLANE

0.25

SEATING PLANE

0°−8°

0.6 ± 0.1

DETAIL A
TYPICAL

SEE DETAIL D

0.09−0.20 TYP

MTC24 (REV B)

24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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