FAIRCHILD

SEMICONDUCTOR ™

74LCX652
Low Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

The LCX652 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX652 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

■ 5V tolerant inputs and outputs

■ 2.3V – 3.6V V_{CC} specifications provided

■ 7.0 ns t_{PD} max (V_{CC} = 3.3V), 10 μA I_{CC} max

■ Power down high impedance inputs and outputs

■ Supports live insertion/withdrawal (Note 1)

■ ±24 mA output drive (V_{CC} = 3.0V)

■ Implements patented noise/EMI reduction circuitry

■ Latch-up performance exceeds 500 mA

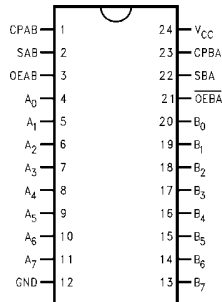■ ESD performance:
  Human body model > 2000V
  Machine model > 200V

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74LCX652WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX652MSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LCX652MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

CPAB	1	24 V_{CC}
SAB	2	23 CPBA
OEAB	3	22 SBA
A_0	4	21 $\overline{OEBA}$
A_1	5	20 B_0
A_2	6	19 B_1
A_3	7	18 B_2
A_4	8	17 B_3
A_5	9	16 B_4
A_6	10	15 B_5
A_7	11	14 B_6
GND	12	13 B_7

Pin Descriptions

Pin Names	Description
A_0–A_7, B_0–B_7	A and B Inputs/3-STATE Outputs
CPAB, CPBA	Clock Inputs
SAB, SBA	Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

74LCX652

Logic Symbols

IEEE/IEC
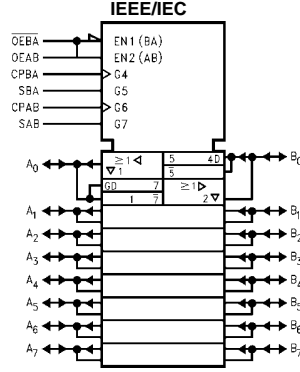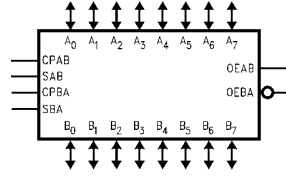
Truth Table

(Note 2)

Inputs						Inputs/Outputs		Operating Mode
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	⌐	⌐	X	X			Store A and B Data
X	H	⌐	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	⌐	⌐	X	X	Input	Output	Store A in Both Registers
L	X	H or L	⌐	X	X	Not Specified	Input	Hold A, Store B
L	L	⌐	⌐	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

Note 2: The data output functions may be enabled or disabled by various signals at OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
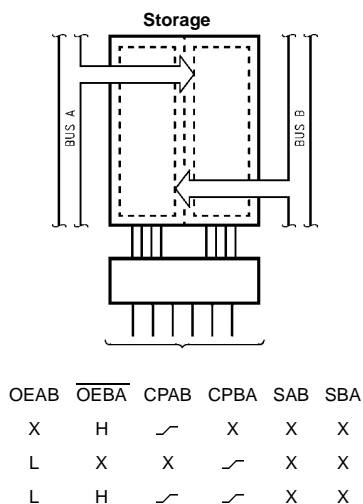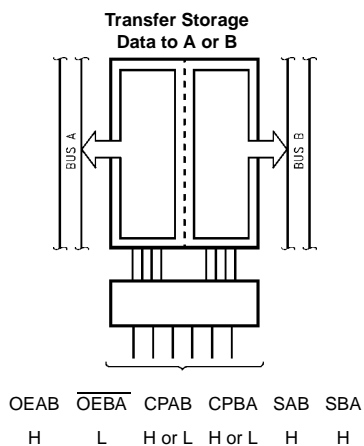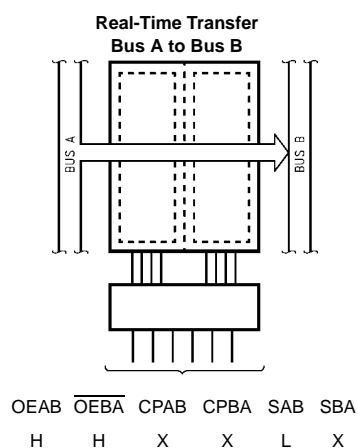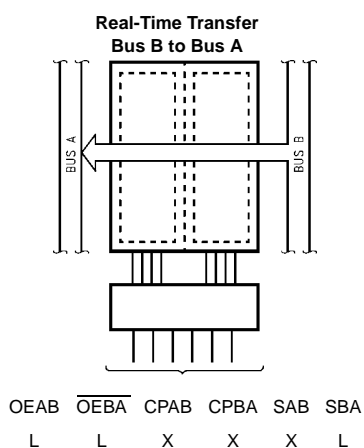
Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.
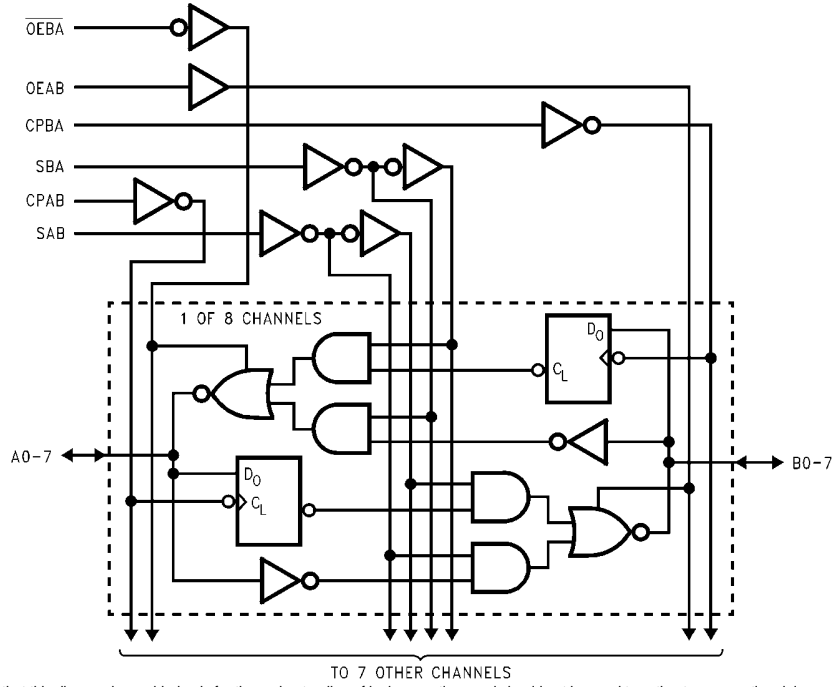
The select (SAB, SBA) controls can multiplex stored and real-time.

The examples below demonstrate the four fundamental bus-management functions that can be performed with the Octal bus transceiver and receiver.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

Real-Time Transfer
Bus B to Bus A

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus A to Bus B

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

Transfer Storage
Data to A or B

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

Storage

OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	⤴	X	X	X
L	X	X	⤴	X	X
L	H	⤴	⤴	X	X

Logic Diagram

74LCX652

OEBA

OEAB

CPBA

SBA

CPAB

SAB

1 OF 8 CHANNELS

A0–7

B0–7

TO 7 OTHER CHANNELS

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 3)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 4)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 5)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V		±24	mA
		V_{CC} = 2.7V − 3.0V		±12	
		V_{CC} = 2.3V − 2.7V		±8	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V − 2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Unused inputs or I/Os must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.3 – 3.6	V_{CC} − 0.2		V
		I_{OH} = −8 mA	2.3	1.8		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.3 – 3.6		0.2	V
		I_{OL} = 8 mA	2.3		0.6	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.3 – 3.6		±5.0	µA
I_{OZ}	3-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V	2.3 – 3.6		±5.0	µA
		V_I = V_{IH} or V_{IL}				
I_{OFF}	Power-Off Leakage Current	V_I or V_O 5.5V	0		10	µA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_CC (V)	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units
I_CC	Quiescent Supply Current	V_I = V_CC or GND	2.3 – 3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V (Note 6)	2.3 – 3.6		±10	
ΔI_CC	Increase in I_CC per Input	V_IH = V_CC −0.6V	2.3 – 3.6		500	μA

Note 6: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	T_A = −40°C to +85°C; R_L = 500Ω V_CC = 3.3V ± 0.3V C_L = 50 pF Min	V_CC = 3.3V ± 0.3V C_L = 50 pF Max	V_CC = 2.7V C_L = 50 pF Min	V_CC = 2.7V C_L = 50 pF Max	V_CC = 2.5V ± 0.2V C_L = 30 pF Min	V_CC = 2.5V ± 0.2V C_L = 30 pF Max	Units
f_MAX	Maximum Clock Frequency	150						MHz
t_PHL	Propagation Delay	1.5	7.0	1.5	8.0	1.5	8.4	ns
t_PLH	Bus to Bus	1.5	7.0	1.5	8.0	1.5	8.4	
t_PHL	Propagation Delay	1.5	8.5	1.5	9.5	1.5	10.5	ns
t_PLH	Clock to Bus	1.5	8.5	1.5	9.5	1.5	10.5	
t_PHL	Propagation Delay	1.5	8.5	1.5	9.5	1.5	10.5	ns
t_PLH	Select to Bus	1.5	8.5	1.5	9.5	1.5	10.5	
t_PZL	Output Enable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns
t_PZH		1.5	8.5	1.5	9.5	1.5	10.5	
t_PLZ	Output Disable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns
t_PHZ		1.5	8.5	1.5	9.5	1.5	10.5	
t_S	Setup Time	2.5		2.5		4.0		ns
t_H	Hold Time	1.5		1.5		2.0		ns
t_W	Pulse Width	3.3		3.3		4.0		ns
t_OSHL	Output to Output Skew (Note 7)		1.0					ns
t_OSLH			1.0					

Note 7: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_OSHL) or LOW-to-HIGH (t_OSLH). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_CC (V)	T_A = 25°C Typical	Units
V_OLP	Quiet Output Dynamic Peak V_OL	C_L = 50 pF, V_IH = 3.3V, V_IL = 0V	3.3	0.8	V
		C_L = 30 pF, V_IH = 2.5V, V_IL = 0V	2.5	0.6	
V_OLV	Quiet Output Dynamic Valley V_OL	C_L = 50 pF, V_IH = 3.3V, V_IL = 0V	3.3	−0.8	V
		C_L = 30 pF, V_IH = 2.5V, V_IL = 0V	2.5	−0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_IN	Input Capacitance	V_CC = Open, V_I = 0V or V_CC	7	pF
C_I/O	Input/Output Capacitance	V_CC = 3.3V, V_I = 0V or V_CC	8	pF
C_PD	Power Dissipation Capacitance	V_CC = 3.3V, V_I = 0V or V_CC, f = 10 MHz	25	pF

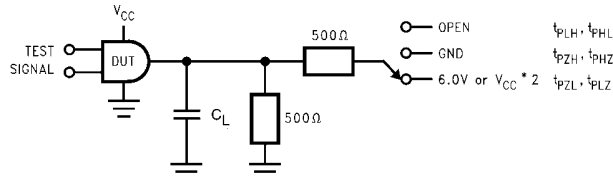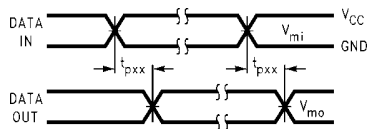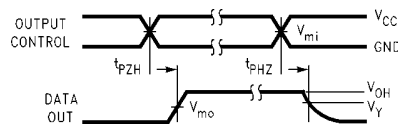# AC LOADING and WAVEFORMS Generic for LCX Family

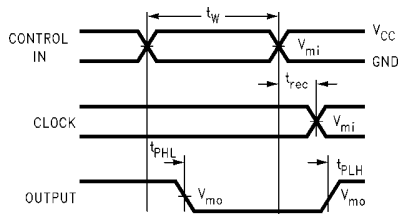**FIGURE 1. AC Test Circuit (C$_L$ includes probe and jig capacitance)**

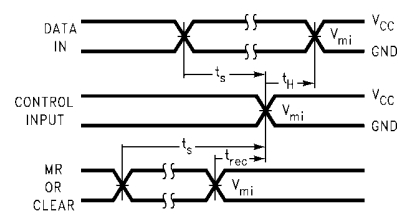| Test	Switch
t$_{PLH}$, t$_{PHL}$	Open
t$_{PZL}$, t$_{PLZ}$	6V at V$_{CC}$ = 3.3 ± 0.3V V$_{CC}$ x 2 at V$_{CC}$ = 2.5 ± 0.2V
t$_{PZH}$, t$_{PHZ}$	GND

Waveform for Inverting and Non-Inverting Functions

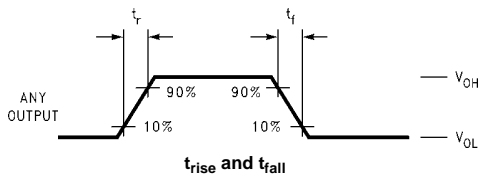**3-STATE Output High Enable and Disable Times for Logic**

Propagation Delay. Pulse Width and t$_{rec}$ Waveforms

Setup Time, Hold Time and Recovery Time for Logic
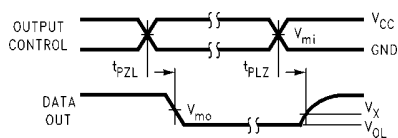
**3-STATE Output Low Enable and Disable Times for Logic**

t$_{rise}$ and t$_{fall}$

FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t$_R$ = t$_F$ = 3ns)

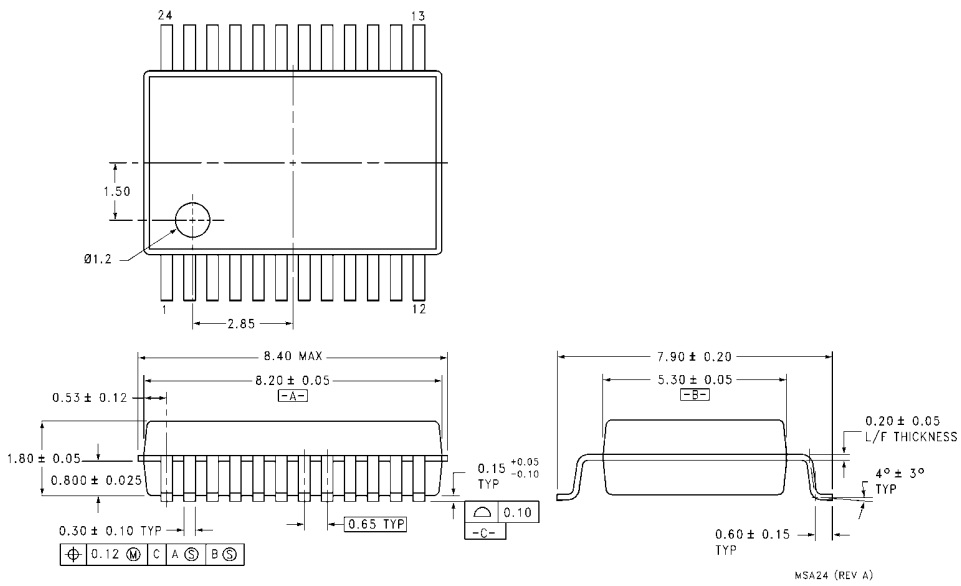| Symbol	V$_{CC}$		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V$_{mi}$	1.5V	1.5V	V$_{CC}$/2
V$_{mo}$	1.5V	1.5V	V$_{CC}$/2
V$_x$	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.15V
V$_y$	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.15V

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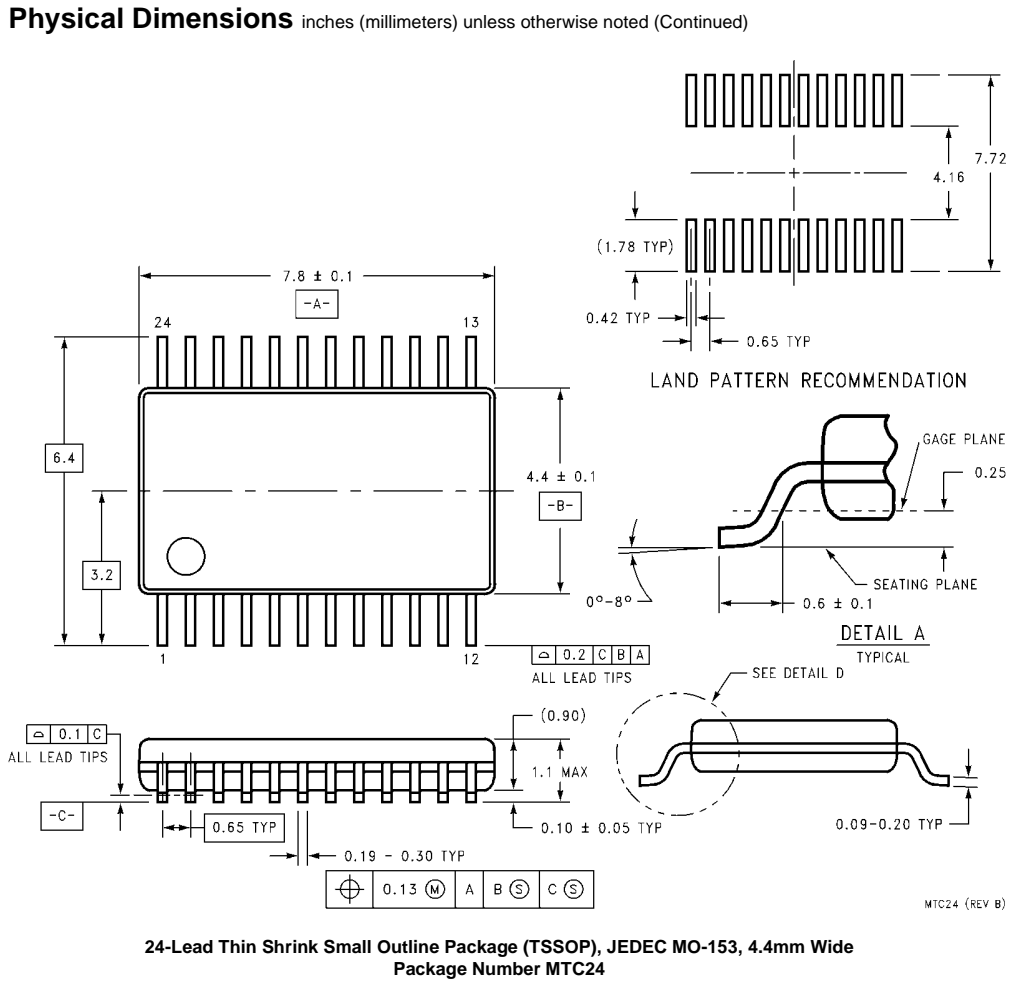**Schematic Diagram** Generic for LCX Family
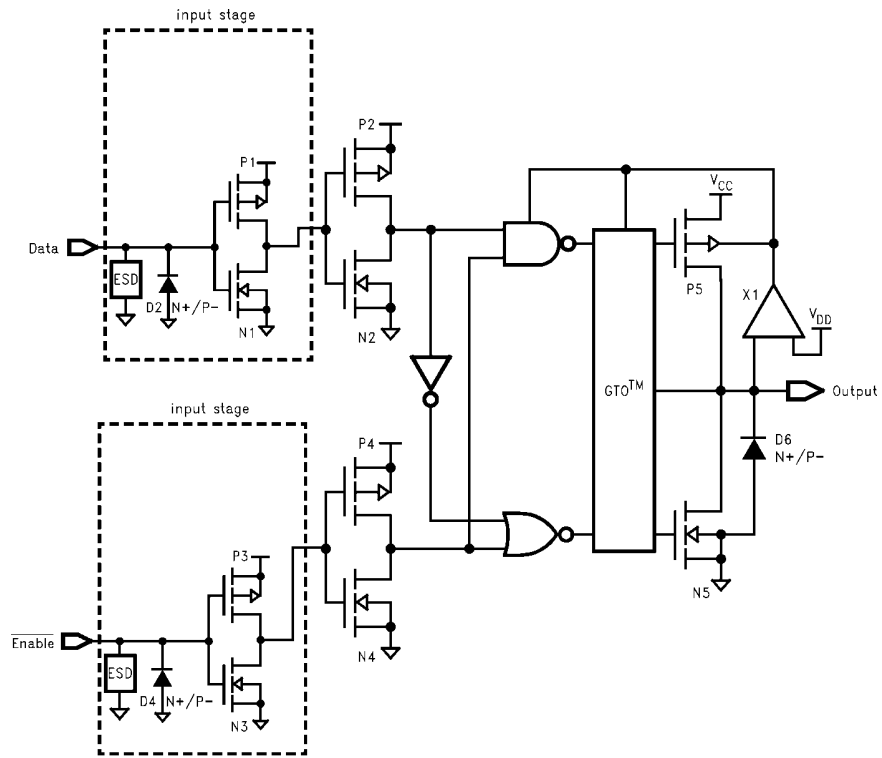
Physical Dimensions inches (millimeters) unless otherwise noted
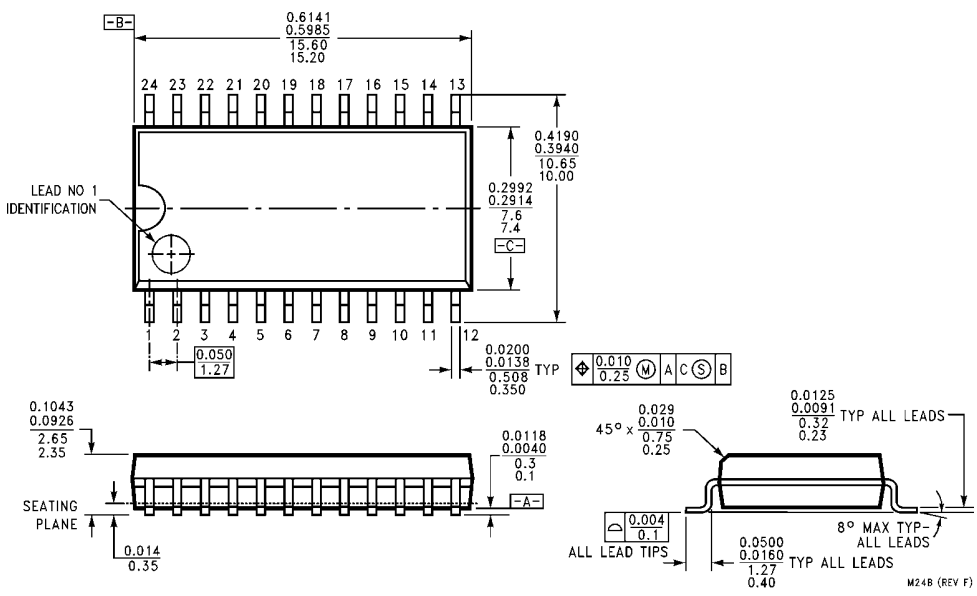
24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M24B

24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA24

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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

7.72

4.16

(1.78 TYP)

0.42 TYP

0.65 TYP

LAND PATTERN RECOMMENDATION

7.8 ± 0.1

−A−

24   13

6.4

4.4 ± 0.1

−B−

3.2

1   12

⌖ 0.2 C B A
ALL LEAD TIPS

GAGE PLANE

0.25

0°−8°

0.6 ± 0.1

SEATING PLANE

DETAIL A
TYPICAL

⌖ 0.1 C
ALL LEAD TIPS

−C−

0.65 TYP

0.19 − 0.30 TYP

(0.90)

1.1 MAX

0.10 ± 0.05 TYP

SEE DETAIL D

0.09−0.20 TYP

⌖ 0.13 Ⓜ A B Ⓢ C Ⓢ

MTC24 (REV B)

24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24