FAIRCHILD SEMICONDUCTOR™

May 2000
Revised May 2000

74LVTH16835
Low Voltage 18-Bit Universal Bus Driver with 3-STATE Outputs (Preliminary)

General Description

The LVTH16835 consists of 18-bit universal bus drivers which combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. This device operates in the transparent mode when the latch-enable (LE) input is HIGH. The A data is latched if the clock (CLK) input is held at a HIGH or LOW logic level. If LE is LOW, the A-bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of the CLK. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state.

The LVTH16835 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

The bus driver is designed for low voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH16835 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

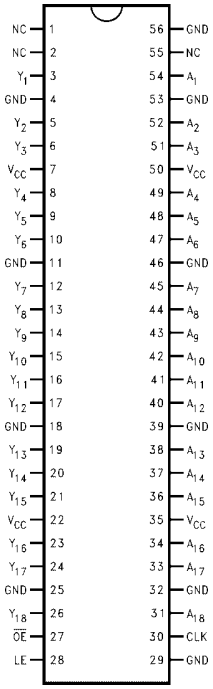
- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink –32 mA/+64 mA
- Latch-up performance exceeds 500 mA

Ordering Code:

Order Number	Package Number	Package Description
74LVTH16835MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
74LVTH16835MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
A_1–A_{18}	Data Register Inputs
Y_1–Y_{18}	3-STATE Outputs
CLK	Clock Pulse Input
$\overline{OE}$	Output Enable Input
LE	Latch Enable Input

Truth Table

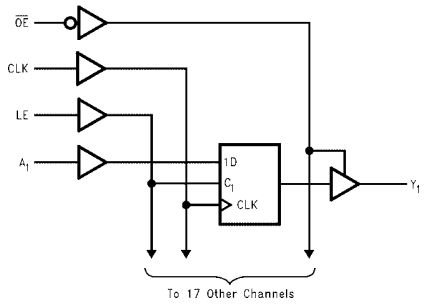
Inputs				Output Y
$\overline{OE}$	LE	CLK	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y_0 (Note 1)
L	L	L	X	Y_0 (Note 2)

H = HIGH Voltage Level L = LOW Voltage Level
X = Immaterial Z = High Impedance
↑ = HIGH-to-LOW Clock Transition

Note 1: Output level before the indicated steady-state input conditions were established, provided that CLK was HIGH before LE went LOW.

Note 2: Output level before the indicated steady-state input conditions were established.

Logic Diagram



Absolute Maximum Ratings(Note 3)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to +7.0	Output in HIGH or LOW State (Note 4)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current		−32	mA
I_{OL}	LOW-Level Output Current		64	mA
T_A	Free-Air Operating Temperature	−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note 3: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 4: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units	Conditions
				Min	Max		
V_{IK}	Input Clamp Diode Voltage		2.7		−1.2	V	$I_I = -18$ mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0		V	$V_O \le 0.1V$ or
V_{IL}	Input LOW Voltage		2.7–3.6		0.8		$V_O \ge V_{CC} - 0.1V$
V_{OH}	Output HIGH Voltage		2.7–3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100$ µA
			2.7	2.4		V	$I_{OH} = -8$ mA
			3.0	2.0		V	$I_{OH} = -32$ mA
V_{OL}	Output LOW Voltage		2.7		0.2	V	$I_{OL} = 100$ µA
			2.7		0.5	V	$I_{OL} = 24$ mA
			3.0		0.4	V	$I_{OL} = 16$ mA
			3.0		0.5	V	$I_{OL} = 32$ mA
			3.0		0.55	V	$I_{OL} = 64$ mA
$I_{I(HOLD)}$	Bushold Input Minimum Drive		3.0	75		µA	$V_I = 0.8V$
				−75		µA	$V_I = 2.0V$
$I_{I(OD)}$	Bushold Input Over-Drive Current to Change State		3.0	500		µA	(Note 5)
				−500		µA	(Note 6)
I_I	Input Current		3.6		10	µA	$V_I = 5.5V$
		Control Pins	3.6		±1	µA	$V_I = 0V$ or V_{CC}
		Data Pins	3.6		−5	µA	$V_I = 0V$
					1	µA	$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current		0		±100	µA	$0V \le V_I$ or $V_O \le 5.5V$
$I_{PU/PD}$	Power up/down 3-STATE Output Current		0–1.5V		±100	µA	$V_O = 0.5V$ to $3.0V$ $V_I = GND$ or V_{CC}
I_{OZL}	3-STATE Output Leakage Current		3.6		−5	µA	$V_O = 0.5V$
I_{OZH}	3-STATE Output Leakage Current		3.6		5	µA	$V_O = 3.0V$
$I_{OZH}+$	3-STATE Output Leakage Current		3.6		10	µA	$V_{CC} < V_O \le 5.5V$
I_{CCH}	Power Supply Current		3.6		0.19	mA	Outputs HIGH
I_{CCL}	Power Supply Current		3.6		5	mA	Outputs LOW
I_{CCZ}	Power Supply Current		3.6		0.19	mA	Outputs Disabled
$I_{CCZ}+$	Power Supply Current		3.6		0.19	mA	$V_{CC} \le V_O \le 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 7)		3.6		0.2	mA	One Input at $V_{CC} - 0.6V$ Other Inputs at V_{CC} or GND

Note 5: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 6: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 8)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			Units	Conditions
			Min	Typ	Max		$C_L = 50$ pF, $R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 9)

Note 8: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\ \Omega$				Units
			$V_{CC} = 3.3 \pm 0.3V$		$V_{CC} = 2.7V$		
			Min	Max	Min	Max	
f_{MAX}			150		150		MHz
t_{PLH}	Propagation Delay		1.3	3.7	1.3	4.0	ns
t_{PHL}	A to Y		1.3	3.7	1.3	4.0	
t_{PLH}	Propagation Delay		1.5	5.1	1.5	5.7	ns
t_{PHL}	LE to Y		1.5	5.1	1.5	5.7	
t_{PLH}	Propagation Delay		1.5	5.1	1.5	5.7	ns
t_{PHL}	CLK to Y		1.5	5.1	1.5	5.7	
t_{PZH}	Output Enable Time		1.3	4.6	1.3	5.5	ns
t_{PZL}			1.3	4.6	1.3	5.5	
t_{PHZ}	Output Disable Time		1.7	5.8	1.7	6.3	ns
t_{PLZ}			1.7	5.8	1.7	6.3	
t_S	Setup Time	A before CLK	2.1		2.4		ns
		A before LE, CLK HIGH	2.3		1.5		
		A before LE, CLK LOW	1.5		0.5		
t_H	Hold Time	A after CLK	1.0		0.0		ns
		A after LE	0.8		0.8		
t_W	Pulse Duration	LE HIGH	3.3		3.3		ns
		CLK HIGH or LOW	3.3		3.3		
t_{OSLH}	Output to Output Skew			1.0		1.0	ns
t_{OSHL}	(Note 10)			1.0		1.0	

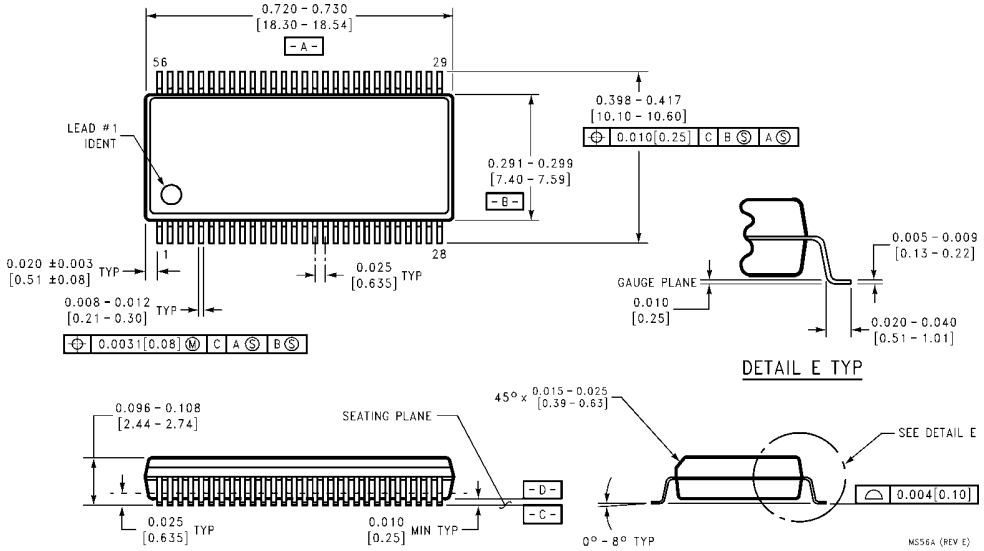
Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 11)

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}	4	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}	8	pF

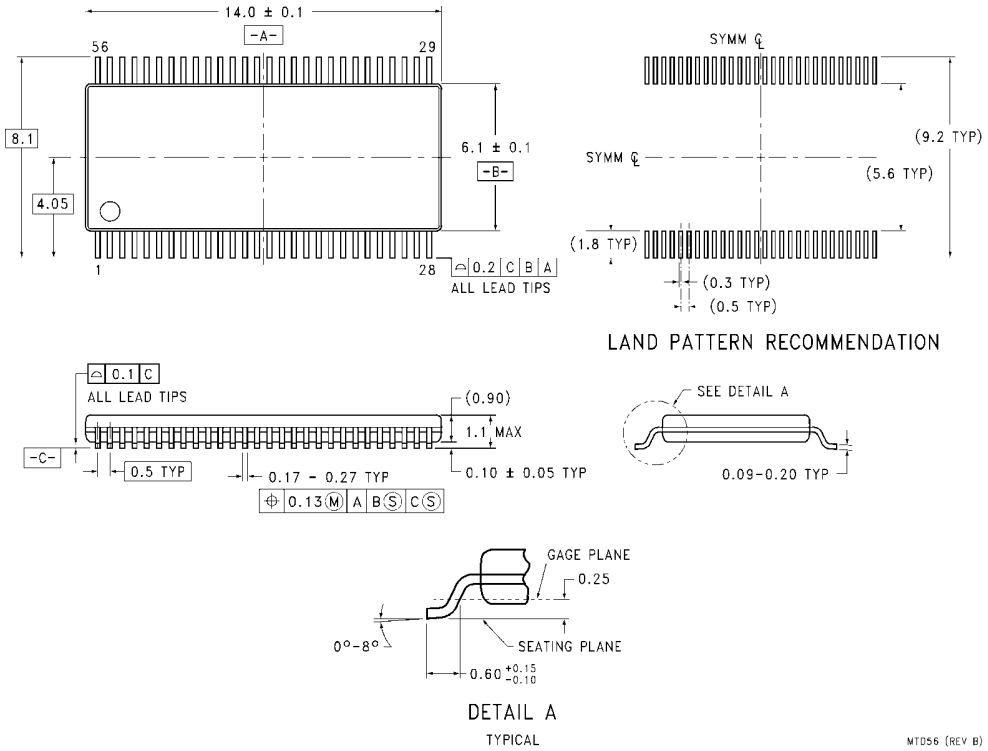
Note 11: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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