

## 74VCX162373

### Low Voltage 16-Bit Transparent Latch with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in Outputs

#### General Description

The VCX162373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear to be transparent to the data when the Latch enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH, the outputs are in a high impedance state.

The VCX162373 is also designed with 26Ω resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers and bus transceivers/transmitters.

The 74VCX162373 is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with I/O compatibility up to 3.6V.

The 74VCX162373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### Features

- 1.65V–3.6V  $V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in outputs
- $t_{PD}$  ( $I_n$  to  $O_n$ )
  - 3.3 ns max for 3.0V to 3.6V  $V_{CC}$
  - 4.5 ns max for 2.3V to 2.7V  $V_{CC}$
  - 9.0 ns max for 1.65V to 1.95V  $V_{CC}$
- Power-off high impedance inputs and outputs
- Support live insertion and withdrawal (Note 1)
- Static Drive ( $I_{OH}/I_{OL}$ )
  - ±12 mA @ 3.0V  $V_{CC}$
  - ±8 mA @ 2.3V  $V_{CC}$
  - ±3 mA @ 1.65V  $V_{CC}$
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

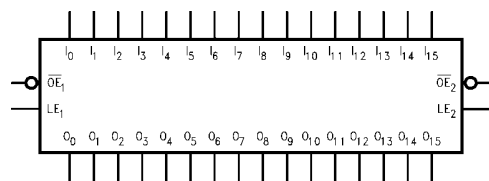
**Note 1:** To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

#### Ordering Code:

Ordering Number	Package Number	Package Description
74VCX162373MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

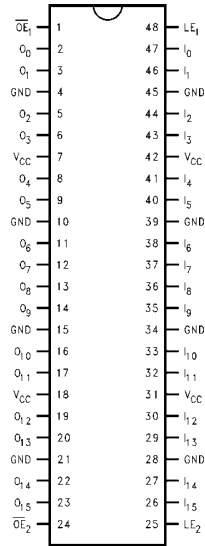
#### Logic Symbol



#### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$LE_n$	Latch Enable Input
$I_0$ – $I_{15}$	Inputs
$O_0$ – $O_{15}$	Outputs

**Connection Diagram**



**Truth Tables**

Inputs			Outputs
LE <sub>1</sub>	$\overline{OE}_1$	I <sub>0</sub> -I <sub>7</sub>	O <sub>0</sub> -O <sub>7</sub>
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O <sub>0</sub>

Inputs			Outputs
LE <sub>2</sub>	$\overline{OE}_2$	I <sub>8</sub> -I <sub>15</sub>	O <sub>8</sub> -O <sub>15</sub>
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O <sub>0</sub>

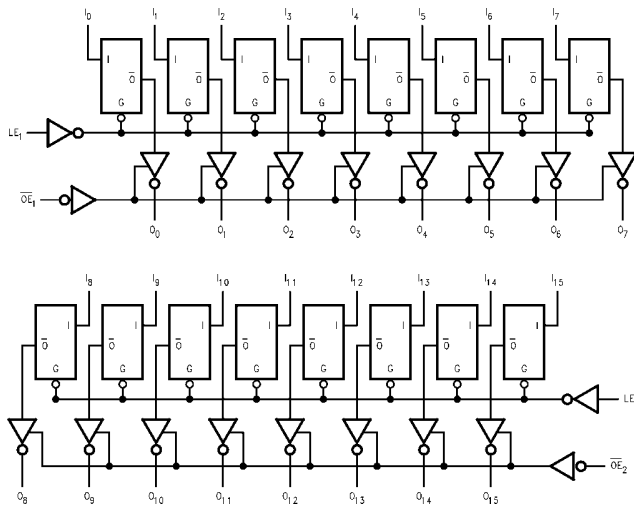
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial (HIGH or LOW, inputs may not float)  
 Z = High Impedance  
 O<sub>0</sub> = Previous O<sub>0</sub> before HIGH-to-LOW of Latch Enable

**Functional Description**

The 74VCX162373 contains sixteen edge D-type latches with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE<sub>n</sub>) input is HIGH, data on the I<sub>n</sub> enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time

its I input changes. When LE<sub>n</sub> is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition on LE<sub>n</sub>. The 3-STATE outputs are controlled by the Output Enable ( $\overline{OE}_n$ ) input. When  $\overline{OE}_n$  is LOW the standard outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

**Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)		Recommended Operating Conditions (Note 4)	
Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V	Power Supply	
DC Input Voltage ( $V_I$ )	-0.5V to +4.6V	Operating	1.65V to 3.6V
Output Voltage ( $V_O$ )		Data Retention Only	1.2V to 3.6V
Outputs 3-STATED	-0.5V to +4.6V	Input Voltage	-0.3V to +3.6V
Outputs Active (Note 3)	-0.5V to $V_{CC} + 0.5V$	Output Voltage ( $V_O$ )	
DC Input Diode Current ( $I_{IK}$ )		Output in Active States	0V to $V_{CC}$
$V_I < 0V$	-50 mA	Output in "OFF" State	0.0V to 3.6V
DC Output Diode Current ( $I_{OK}$ )		Output Current in $I_{OH}/I_{OL}$	
$V_O < 0V$	-50 mA	$V_{CC} = 3.0V$ to 3.6V	$\pm 12$ mA
$V_O > V_{CC}$	+50 mA	$V_{CC} = 2.3V$ to 2.7V	$\pm 8$ mA
DC Output Source/Sink Current		$V_{CC} = 1.65V$ to 2.3V	$\pm 3$ mA
( $I_{OH}/I_{OL}$ )	$\pm 50$ mA	Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
DC $V_{CC}$ or GND Current per		Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
Supply Pin ( $I_{CC}$ or GND)	$\pm 100$ mA	$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C		

**Note 2:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 4:** Floating or unused inputs must be held HIGH or LOW.

### DC Electrical Characteristics (2.7V < $V_{CC}$ ≤ 3.6V)

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		2.7-3.6	2.0		V
$V_{IL}$	LOW Level Input Voltage		2.7-3.6		0.8	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7-3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -6$ mA	2.7	2.2		V
		$I_{OH} = -8$ mA	3.0	2.4		V
		$I_{OH} = -12$ mA	3.0	2.2		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.7-3.6		0.2	V
		$I_{OL} = 6$ mA	2.7		0.4	V
		$I_{OL} = 8$ mA	3.0		0.55	V
		$I_{OL} = 12$ mA	3.0		0.8	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	2.7-3.6		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or $V_{IL}$	2.7-3.6		$\pm 10$	$\mu A$
$I_{OFF}$	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7-3.6		20	$\mu A$
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 5)	2.7-3.6		$\pm 20$	$\mu A$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	2.7-3.6		750	$\mu A$

**Note 5:** Outputs disabled or 3-STATE only.

DC Electrical Characteristics ( $2.3V \leq V_{CC} \leq 2.7V$ )						
Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		2.3 - 2.7	1.6		V
$V_{IL}$	LOW Level Input Voltage		2.3 - 2.7		0.7	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.3 - 2.7	$V_{CC} - 0.2$		V
		$I_{OH} = -4 \text{ mA}$	2.3	2.0		V
		$I_{OH} = -6 \text{ mA}$	2.3	1.8		V
		$I_{OH} = -8 \text{ mA}$	2.3	1.7		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 - 2.7		0.2	V
		$I_{OL} = 6 \text{ mA}$	2.3		0.4	V
		$I_{OL} = 8 \text{ mA}$	2.3		0.6	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	2.3 - 2.7		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or $V_{IL}$	2.3 - 2.7		$\pm 10$	$\mu A$
$I_{OFF}$	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 - 2.7		20	$\mu A$
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 6)	2.3 - 2.7		$\pm 20$	$\mu A$
<b>Note 6:</b> Outputs disabled or 3-STATE only.						
DC Electrical Characteristics ( $1.65V \leq V_{CC} < 2.3V$ )						
Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		1.65 - 2.3	$0.65 \times V_{CC}$		V
$V_{IL}$	LOW Level Input Voltage		1.65 - 2.3		$0.35 \times V_{CC}$	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.65 - 2.3	$V_{CC} - 0.2$		V
		$I_{OH} = -3 \text{ mA}$	1.65	1.25		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	1.65 - 2.3		0.2	V
		$I_{OL} = 3 \text{ mA}$	1.65		0.3	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	1.65 - 2.3		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or $V_{IL}$	1.65 - 2.3		$\pm 10$	$\mu A$
$I_{OFF}$	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND	1.65 - 2.3		20	$\mu A$
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 7)	1.65 - 2.3		$\pm 20$	$\mu A$
<b>Note 7:</b> Outputs disabled or 3-STATE only.						

AC Electrical Characteristics (Note 8)								
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, C_L = 30\text{ pF}, R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	
$t_{PHL}, t_{PLH}$	Prop Delay $I_n$ to $O_n$	0.8	3.3	1.0	4.5	1.5	9.0	ns
$t_{PHL}, t_{PLH}$	Prop Delay LE to $O_n$	0.8	3.6	1.0	4.9	1.5	9.8	ns
$t_{PZL}, t_{PZH}$	Output Enable Time	0.8	3.9	1.0	5.4	1.5	9.8	ns
$t_{PLZ}, t_{PHZ}$	Output Disable Time	0.8	4.0	1.0	4.4	1.5	7.9	ns
$t_S$	Setup Time	1.5		1.5		2.5		ns
$t_H$	Hold Time	1.0		1.0		1.0		ns
$t_W$	Pulse Width	1.5		1.5		4.0		ns
$t_{OSHL}$ $t_{OSLH}$	Output to Output Skew (Note 9)		0.5		0.5		0.75	ns

**Note 8:** For  $C_L = 50\text{ pF}$ , add approximately 300 ps to the AC maximum specification.

**Note 9:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ).

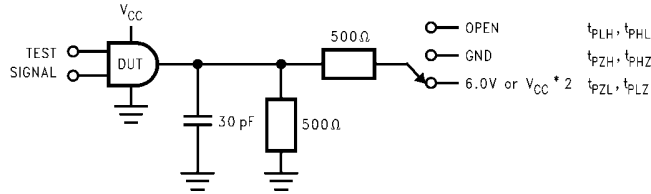
### Dynamic Switching Characteristics

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$	Units
				Typical	
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8	0.15	V
			2.5	0.25	
			3.3	0.35	
$V_{OLV}$	Quiet Output Dynamic Valley $V_{OL}$	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8	-0.15	V
			2.5	-0.25	
			3.3	-0.35	
$V_{OHV}$	Quiet Output Dynamic Valley $V_{OH}$	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8	1.55	V
			2.5	2.05	
			3.3	2.65	

### Capacitance

Symbol	Parameter	Conditions	$T_A = +25^\circ\text{C}$	Units
			Typical	
$C_{IN}$	Input Capacitance	$V_{CC} = 1.8V, 2.5V$ or $3.3V, V_I = 0V$ or $V_{CC}$	6	pF
$C_{OUT}$	Output Capacitance	$V_I = 0V$ or $V_{CC}, V_{CC} = 1.8V, 2.5V$ or $3.3V$	7	pF
$C_{PD}$	Power Dissipation Capacitance	$V_I = 0V$ or $V_{CC}, f = 10\text{ MHz}, V_{CC} = 1.8V, 2.5V$ or $3.3V$	20	pF

### AC Loading and Waveforms



TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ ; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V; 1.8V \pm 0.15V$
$t_{PZH}, t_{PHZ}$	GND

FIGURE 1. AC Test Circuit

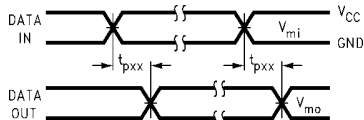


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

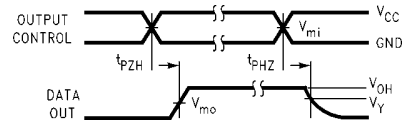


FIGURE 3. 3-STATE Output HIGH Enable and Disable Times for Low Voltage Logic

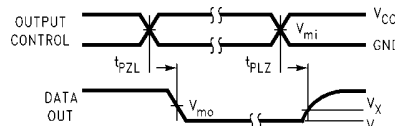


FIGURE 4. 3-STATE Output LOW Enable and Disable Times for Low Voltage Logic

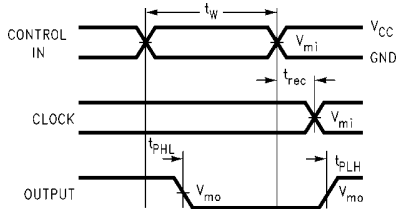


FIGURE 5. Propagation Delay, Pulse Width and  $t_{REC}$  Waveforms

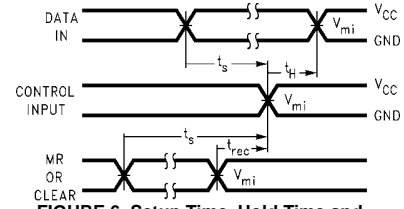


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$
$V_{mi}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
$V_Y$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

