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74VCX16839

Low Voltage 20-Bit Selectable Register/Buffer with 3.6V Tolerant Inputs and Outputs

General Description

The VCX16839 contains twenty non-inverting selectable buffered or registered paths. The device can be configured to operate in a registered, or flow through buffer mode by utilizing the register enable (REGE) and Clock (CP) signals. The device operates in a 20-bit word wide mode. All outputs can be placed into 3-STATE through use of the $\overline{\text{OE}}$ pin. These devices are ideally suited for buffered or registered 168 pin and 200 pin SDRAM DIMM memory modules.

The 74VCX16839 is designed for low voltage (1.65V to 3.6V) $\rm V_{CC}$ applications with I/O compatibility up to 3.6V.

The 74VCX16839 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- Compatible with PC100 and PC133 DIMM module specifications
- 1.65V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD} (CP to O_n)
 - 3.2 ns max for 3.0V to 3.6V V_{CC}
 - 4.4 ns max for 2.3V to 2.7V V_{CC}
 - 8.8 ns max for 1.65V to 1.95V $V_{\rm CC}$
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
 - ±24 mA @ 3.0V V_{CC}
 - \pm 18 mA @ 2.3V V_{CC}
 - ±6 mA @ 1.65V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:

Human body model > 2000V

Machine model > 200V

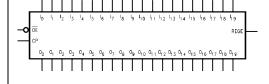
Note 1: To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the distinct

Ordering Code:

Order Number	Package Number	Package Descriptions
74VCX16839MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Pin Descriptions

Pin Names	Description
ŌE	Output Enable Input (Active LOW)
I ₀ -I ₁₉	Inputs
O ₀ -O ₁₉	Outputs
CP	Clock Pulse Input
REGE	Register Enable Input

Connection Diagram



Truth Table

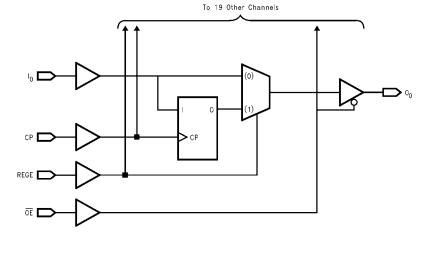
	Inputs				
СР	REGE	I _n	OE	On	
1	Н	Н	L	Н	
1	Н	L	L	L	
Х	L	Н	L	Н	
Х	L	L	L	L	
Х	Х	Х	Н	Z	

- H = HIGH Voltage Level
- L = LOW Voltage Level
 X = Immaterial (HIGH or LOW, inputs may not float)
- Z = High Impedance

Functional Description

The 74VCX16839 consists of twenty selectable non-inverting buffers or registers with word wide controls. Mode functionality is selected through operation of the $\ensuremath{\mathsf{CP}}$ and $\ensuremath{\mathsf{REGE}}$ pin as shown by the truth table. When REGE is held at a logic "1" the device operates as a 20-bit register. Data is transferred from I_n to O_n on the rising edge of the CP pin. When the REGE pin is held at a logic "0" the device operates in a flow through mode and data propagates directly from the In to the On outputs. All outputs can be 3-stated by holding the $\overline{\rm OE}$ pin at a logic "1."

Logic Diagram



Absolute Maximum Ratings(Note 2)

 $\label{eq:continuity} \begin{array}{lll} \mbox{Supply Voltage (V$_{CC}$)} & -0.5\mbox{V to } +4.6\mbox{V} \\ \mbox{DC Input Voltage (V$_{I}$)} & -0.5\mbox{V to } +4.6\mbox{V} \\ \end{array}$

Output Voltage (V_O)

Outputs 3-STATE -0.5 V to +4.6 V Outputs Active (Note 3) $-0.5 \text{V to } V_{\text{CC}} +0.5 \text{V}$ DC Input Diode Current (I_{IK}) $V_{\text{I}} < 0 \text{V}$ -50 mA

DC Output Diode Current (I_{OK})

 $V_{O} < 0V$ -50 mA +50 mA

DC Output Source/Sink Current

 (I_{OH}/I_{OL}) ±50 mA

DC V_{CC} or GND Current per

Supply Pin (I_{CC} or GND) ± 100 mA

Storage Temperature Range (T_{STG}) $-65^{\circ}C$ to $+150^{\circ}C$

Recommended Operating Conditions (Note 4)

Power Supply

 Operating
 1.65V to 3.6V

 Data Retention Only
 1.2V to 3.6V

 Input Voltage
 -0.3V to +3.6V

Output Voltage (V_O)

Output in Active States $0V \text{ to } V_{CC}$ Output in "OFF" State 0.0V to 3.6V

Output Current in I_{OH}/I_{OL}

 $V_{CC} = 3.0 \text{V to } 3.6 \text{V}$ $\pm 24 \text{ mA}$ $V_{CC} = 2.3 \text{V to } 2.7 \text{V}$ $\pm 18 \text{ mA}$

 $V_{CC} = 1.65V \text{ to } 2.3V$ $\pm 6 \text{ mA}$

Free Air Operating Temperature (T_A) -40°C to +85°C

Minimum Input Edge Rate ($\Delta t/\Delta V$)

 $V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$ 10 ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics (2.7V < $V_{CC} \le 3.6V)$

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 – 3.6	2.0		V
V _{IL}	LOW Level Input Voltage		2.7 – 3.6		0.8	V
V _{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu\text{A}$	2.7 – 3.6	V _{CC} - 0.2		V
		I _{OH} = -12 mA	2.7	2.2		V
		I _{OH} = -18 mA	3.0	2.4		V
		I _{OH} = -24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.7 – 3.6		0.2	V
		I _{OL} = 12 mA	2.7		0.4	V
		I _{OL} = 18 mA	3.0		0.4	V
		I _{OL} = 24 mA	3.0		0.55	V
I _I	Input Leakage Current	$0 \le V_I \le 3.6V$	2.7 – 3.6		±5.0	μΑ
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V	2.7 – 3.6		±10	μА
		$V_I = V_{IH}$ or V_{IL}	2.7 - 3.0		±10	μΑ
I _{OFF}	Power-OFF Leakage Current	$0 \le (V_1, V_0) \le 3.6V$	0		10	μΑ
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.7 – 3.6		20	μΑ
		$V_{CC} \le (V_I, V_O) \le 3.6V \text{ (Note 5)}$	2.7 – 3.6		±20	μΑ
ΔI_{CC}	Increase in I _{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7 - 3.6		750	μΑ

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Note 5: Outputs disabled or 3-STATE only.

DC Electrical Characteristics (2.3V \leq $V_{CC} \leq$ 2.7V)

Symbol	Parameter	Conditions	V _{CC}	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.6		V
V _{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
V _{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu\text{A}$	2.3 – 2.7	V _{CC} - 0.2		V
		I _{OH} = -6 mA	2.3	2.0		V
		I _{OH} = -12 mA	2.3	1.8		V
		I _{OH} = -18 mA	2.3	1.7		V
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3 – 2.7		0.2	V
		I _{OL} = 12 mA	2.3		0.4	V
		I _{OL} = 18 mA	2.3		0.6	٧
I	Input Leakage Current	$0 \le V_I \le 3.6V$	2.3 – 2.7		±5.0	μΑ
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V	2.3 – 2.7		±10	μА
		$V_I = V_{IH}$ or V_{IL}	2.3 - 2.1		±10	μΑ
I _{OFF}	Power-OFF Leakage Current	$0 \le (V_I, V_O) \le 3.6V$	0		10	μΑ
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3 – 2.7		20	μΑ
		$V_{CC} \le (V_I, V_O) \le 3.6V \text{ (Note 6)}$	2.3 – 2.7		±20	μΑ

Note 6: Outputs disabled or 3-STATE only.

DC Electrical Characteristics (1.65V \leq $V_{\mbox{\footnotesize CC}} < 2.3\mbox{\footnotesize V})$

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		1.65 - 2.3	$0.65 \times V_{CC}$		V
V _{IL}	LOW Level Input Voltage		1.65 - 2.3		$0.35 \times V_{CC}$	V
V _{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu\text{A}$	1.65 - 2.3	V _{CC} - 0.2		V
		$I_{OH} = -6 \text{ mA}$	1.65	1.4		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu\text{A}$	1.65 - 2.3		0.2	V
		I _{OL} = 6 mA	1.65		0.3	V
I _I	Input Leakage Current	$0 \le V_I \le 3.6V$	1.65 - 2.3		±5.0	μΑ
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V	1.65 - 2.3		±10	μА
		$V_I = V_{IH}$ or V_{IL}	1.00 - 2.3		±10	μΑ
I _{OFF}	Power-OFF Leakage Current	$0 \le (V_I, V_O) \le 3.6V$	0		10	μΑ
Icc	Quiescent Supply Current	V _I = V _{CC} or GND	1.65 - 2.3		20	μΑ
		$V_{CC} \le (V_I, V_O) \le 3.6V \text{ (Note 7)}$	1.65 - 2.3		±20	μΑ

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics VCX16839 (Note 8)

		$T_A = -40^{\circ}$ C to $+85^{\circ}$ C, $C_L = 30$ pF, $R_L = 500\Omega$						
Symbol	Parameter	$V_{CC} = 3.3V \pm 0.3V$		$V_{CC}=2.5V\pm0.2V$		$V_{CC} = 1.8V \pm 0.15V$		Units
		Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	250		200		100		MHz
t _{PHL}	Prop Delay I _n to O _n	0.8	2.5	1.0	3.5	1.5	7.0	ns
t _{PLH}	(REGE = 0)							
t _{PHL}	Prop Delay CP to O _n	0.8	3.2	1.0	4.4	1.5	8.8	ns
t _{PLH}	(REGE = 1)							
t _{PHL} , t _{PLH}	Prop Delay REGE to O _n	0.8	4.0	1.0	5.0	1.5	9.8	ns
t _{PZL} , t _{PZH}	Output Enable Time	0.8	3.8	1.0	4.9	1.5	9.8	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	0.8	3.7	1.0	4.2	1.5	7.6	ns
t _S	Setup Time	1.0		1.0		2.5		ns
t _H	Hold Time	0.7		0.7		1.0		ns
t _W	Pulse Width	1.5		1.5		4.0		ns
t _{OSHL}	Output to Output Skew		0.5		0.5		0.75	ns
t _{OSLH}	(Note 9)							

Note 8: For $C_L = 50 \, \mathrm{pF}$, add approximately 300 ps to the AC maximum specification.

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (toshL) or LOW-to-HIGH (toshL).

Extended AC Electrical Characteristics (Note 10)

Symbol	Parameter	$T_A = -0^{\circ}\text{C to } +85^{\circ}\text{C}, R_L = C_1 = 0$	Units	
Syllibol	Farameter	Min	Max	Units
t _{PHL} , t _{PLH}	Prop Delay I _n to O _n (REGE = 0)	1.0	2.8	ns
t _{PHL} , t _{PLH}	Prop Delay CP to O _n (REGE = 1)	1.4	3.5	ns
t _{PHL} , t _{PLH}	Prop Delay REGE to On	1.0	4.3	ns
t _{PZL} , t _{PZH}	Output Enable Time	1.0	4.1	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	1.0	4.0	ns
t _S	Setup Time	1.0		ns
t _H	Hold Time	0.7		ns

Note 10: This parameter is guaranteed by characterization but not tested.

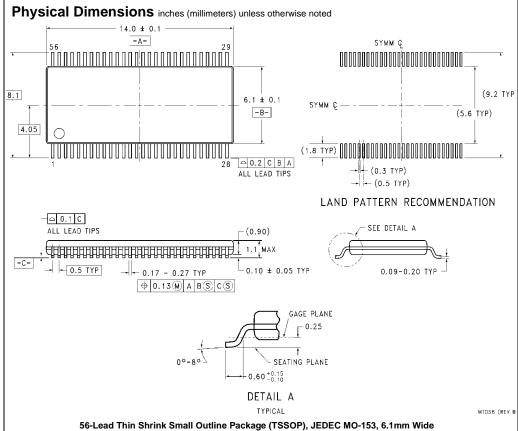
Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C	Units
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8	0.25	
			2.5	0.6	V
			3.3	0.8	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	$C_L = 30 \text{ pF, } V_{IH} = V_{CC}, V_{IL} = 0V$	1.8	-0.25	
			2.5	-0.6	V
			3.3	-0.8	
V _{OHV}	Quiet Output Dynamic Valley V _{OH}	$C_L = 30 \text{ pF, } V_{IH} = V_{CC}, V_{IL} = 0V$	1.8	1.5	
			2.5	1.9	V
			3.3	2.2	

Capacitance

Symbol	Parameter	Conditions	$T_A = +25^{\circ}C$	Units
			Typical	
C _{IN}	Input Capacitance	$V_{CC} = 1.8V$, 2.5V or 3.3V, $V_I = 0V$ or V_{CC}	6	pF
C _{OUT}	Output Capacitance	$V_I = 0V \text{ or } V_{CC}, V_{CC} = 1.8V, 2.5V \text{ or } 3.3V$	7	pF
C _{PD}	Power Dissipation Capacitance	$V_I = 0V \text{ or } V_{CC}, f = 10 \text{ MHz},$	20	pF
		V _{CC} = 1.8V, 2.5V or 3.3V		

AC Loading and Waveforms t_{PLH} , t_{PHL} 500Ω TEST C $t_{\rm PZH},\,t_{\rm PHZ}$ t_{PZL} , t_{PLZ} 500Ω SWITCH Open t_{PLH}, t_{PHL} 6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$; $1.8V \pm 0.15V$ $t_{PZL},\,t_{PLZ}$ GND $t_{PZH},\,t_{PHZ}$ FIGURE 1. AC Test Circuit $v_{\rm cc}$ v_{cc} CONTROL OUT FIGURE 3. 3-STATE Output High Enable and FIGURE 2. Waveform for Inverting and Disable Times for Low Voltage Logic **Non-Inverting Functions** $v_{\rm cc}$ OUTPUT CONTROL t_{PZL} DATA FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic CONTROL IN CONTROL CLOCK MR OR CLEAR STUDY Time, Hold Time and OUTPUT FIGURE 5. Propagation Delay, Pulse Width and $\rm t_{\rm rec}$ Waveforms Recovery Time for Low Voltage Logic v_{cc} Symbol $3.3V \pm 0.3V$ $2.5V \pm 0.2V$ $\textbf{1.8V} \pm \textbf{0.15V}$ 1.5V V_{CC}/2 V_{CC}/2 1.5V V_{CC}/2 V_{CC}/2 V_{OL} +0.3V V_{OL} +0.15V V_{OL} +0.15V V_{OH} -0.3V V_{OH} -0.15V V_{OH} –0.15V



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