FAIRCHILD SEMICONDUCTOR™

June 1999
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74VCX2245
Low Voltage Bidirectional Transceiver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in B Outputs

General Description

The VCX2245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The T/$\overline{R}$ input determines the direction of data flow. The $\overline{OE}$ input disables both the A and B ports by placing them in a high impedance state.

The 74VCX2245 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V. The VCX2245 is also designed with 26Ω series resistance in the B Port outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers transmitters

The 74VCX2245 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V - 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in B Port outputs
- Power-off high impedance inputs and outputs
- Supports Live Insertion and Withdrawal (Note 1)
- t_{PD} (A to B)
  - 4.4 ns max for 3.0V to 3.6V V_{CC}
  - 5.6 ns max for 2.3V to 2.7V V_{CC}
  - 9.8 ns max for 1.65V to 1.95V V_{CC}
- Static Drive (I_{OH}/I_{OL} B outputs):
  - ±12 mA @ 3.0V V_{CC}
  - ±8 mA @ 2.3V V_{CC}
  - ±3 mA @ 1.65V V_{CC}
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

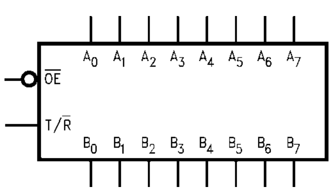
Note 1: To ensure the high impedance state during power up and power down, $\overline{OE}_n$ should be tied to V_{CC} through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74VCX2245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VCX2245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-STATE Outputs
B_0–B_7	Side B Inputs or 3-STATE Outputs

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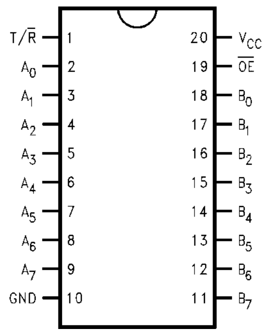
Connection Diagram



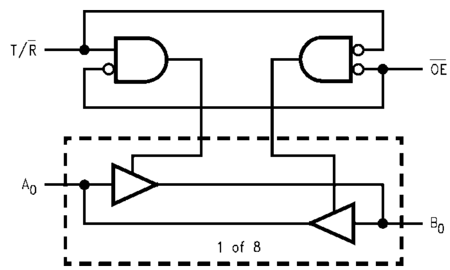
Truth Table

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7 (Note 2)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Note 2: Unused bus terminals during HIGH Z State must be held HIGH or LOW.

Logic Diagram



Absolute Maximum Ratings (Note 3)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
DC Output Voltage (V_O)	
Outputs 3-STATE	−0.5V to +4.6V
Outputs Active (Note 4)	−0.5V to V_{CC} + 0.5V
DC Input Diode Current (I_{IK}) $V_I < 0V$	−50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	−50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA
DC V_{CC} or Ground Current	±100 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 5)

Power Supply Voltage (V_{CC})	
Operating	1.65V to 3.6V
Data Retention Only	1.2V to 3.6V
Input Voltage	−0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0V to 3.6V
Output Current in I_{OH}/I_{OL} - A Outputs	
V_{CC} = 3.0V to 3.6V	±24 mA
V_{CC} = 2.3V to 2.7V	±18 mA
V_{CC} = 1.65V to 2.3V	±6 mA
Output Current in I_{OH}/I_{OL} - B Outputs	
V_{CC} = 3.0V to 3.6V	± 12 mA
V_{CC} = 2.3V to 2.7V	± 8 mA
V_{CC} = 1.65V to 2.3V	± 3 mA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics (2.7V < V_{CC} ≤ 3.6V)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage A Outputs	I_{OH} = −100 µA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
	HIGH Level Output Voltage B Outputs	I_{OH} = −100 µA	2.7–3.6	V_{CC}–0.2		V
		I_{OH} = −6 mA	2.7	2.2		
		I_{OH} = −8 mA	3.0	2.4		
		I_{OH} = −12 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage A Outputs	I_{OL} = 100 µA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 18 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
	LOW Level Output Voltage B Outputs	I_{OL} = 100 µA	2.7–3.6		0.2	V
		I_{OL} = 6 mA	2.7		0.4	
		I_{OL} = 8 mA	3.0		0.55	
		I_{OL} = 12 mA	3.0		0.8	
I_I	Input Leakage Current	0 ≤ V_I ≤ 3.6V	2.7–3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 3.6V V_I = V_{IH} or V_{IL}	2.7–3.6		±10	µA
I_{OFF}	Power Off Leakage Current	0 ≤ (V_I, V_O) ≤ 5.5V	0		10	µA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.7–3.6		20	µA
		V_{CC} ≤ (V_I, V_O) ≤ 3.6V (Note 6)	2.7–3.6		±20	
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7–3.6		750	µA

Note 6: Outputs disabled or 3-STATE only.

DC Electrical Characteristics (2.3V ≤ V_{CC} ≤ 2.7V)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.3–2.7	1.6		V
V_{IL}	LOW Level Input Voltage		2.3–2.7		0.7	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100 μA	2.3–2.7	V_{CC} – 0.2		V
	A Outputs	I_{OH} = –6 mA	2.3	2.0		
		I_{OH} = –12 mA	2.3	1.8		
		I_{OH} = –18 mA	2.3	1.7		
	HIGH Level Output Voltage	I_{OH} = –100 μA	2.3–2.7	V_{CC}–2		V
	B Outputs	I_{OH} = –4 mA	2.3	2.0		
		I_{OH} = –6 mA	2.3	1.8		
		I_{OH} = –8mA	2.3	1.7		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.3–2.7		0.2	V
	A Outputs	I_{OL} = 12 mA	2.3		0.4	
		I_{OL} = 18 mA	2.3		0.6	
	LOW Level Output Voltage	I_{OL} = 100 μA	2.3–2.7		0.2	V
	B Outputs	I_{OL} = 6 mA	2.3		0.4	
		I_{OL} = 8 mA	2.3		0.6	
I_I	Input Leakage Current	0 ≤ V_I ≤ 3.6V	2.3–2.7		±5.0	μA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 3.6V	2.3–2.7		±10	μA
		V_I = V_{IH} or V_{IL}				
I_{OFF}	Power Off Leakage Current	0 ≤ (V_I, V_O) ≤ 3.6V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.3–2.7		20	μA
		V_{CC} ≤ (V_I, V_O) ≤ 3.6V (Note 7)	2.3–2.7		±20	

Note 7: Outputs disabled or 3-STATE only.

DC Electrical Characteristics (1.65V ≤ V_{CC} < 2.3V)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65–2.3	0.65 x V_{CC}		V
V_{IL}	LOW Level Input Voltage		1.65–2.3		0.35 x V_{CC}	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100 μA	1.65–2.3	V_{CC} – 0.2		V
	A Outputs	I_{OH} = –6 mA	1.65	1.25		
	HIGH Level Output Voltage	I_{OH} = -100 μA	1.65–2.3	V_{CC}–0.2		V
	B Outputs	I_{OH} = -3 mA	1.65	1.25		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	1.65–2.3		0.2	V
	A Outputs	I_{OL} = 6 mA	1.65		0.3	
	LOW Level Output Voltage	I_{OL} = 100μA	1.65–2.3		0.2	V
	B Outputs	I_{OL} = 3 mA	1.65		0.3	
I_I	Input Leakage Current	0 ≤ V_I ≤ 3.6V	1.65–2.3		±5.0	μA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 3.6V	1.65-2.3		±10	μA
		V_I = V_{IH} or V_{IL}				
I_{OFF}	Power Off Leakage Current	0 ≤ (V_I, V_O) ≤ 3.6V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	1.65–2.3		20	μA
		V_{CC} ≤ (V_I, V_O) ≤ 3.6V (Note 8)	1.65–2.3		±20	

Note 8: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 9)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 30$ pF, $R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay, A to B	0.6	4.4	0.8	5.6	1.5	9.8	ns
t_{PHL} t_{PLH}	Propagation Delay, B to A	0.6	3.5	0.8	4.2	1.5	8.4	ns
t_{PZL} t_{PZH}	Output Enable Time, A to B	0.6	5.0	0.8	6.6	1.5	9.8	ns
t_{PZL} t_{PZH}	Output Enable Time, B to A	0.6	4.5	0.8	5.6	1.5	9.8	ns
t_{PLZ} t_{PHZ}	Output Disable Time, A to B	0.6	4.2	0.8	4.7	1.5	8.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time, B to A	0.6	3.6	0.8	4.0	1.5	7.2	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 10)		0.5		0.5		0.75	ns

Note 9: For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}, B to A	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8 2.5 3.3	0.3 0.7 1.0	V
	Quiet Output Dynamic Peak V_{OL}, A to B	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8 2.5 3.3	0.2 0.45 0.65	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}, B to A	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8 2.5 3.3	−0.3 −0.7 −1.0	V
	Quiet Output Dynamic Valley, V_{OL}, A to B	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8 2.5 3.3	−0.2 −0.45 −0.65	V
V_{OHV}	Quiet Output Dynamic Valley V_{OH}, B to A	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8 2.5 3.3	1.3 1.7 2.0	V
	Quiet Output Dynamic Valley V_{OH}, A to B	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8 2.5 3.3	1.5 2.0 2.5	V

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$ Typical	Units
C_{IN}	Input Capacitance	$V_I = 0V$ or V_{CC}, $V_{CC} = 1.8V$, 2.5V or 3.3V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_I = 0V$ or V_{CC}, $V_{CC} = 1.8V$, 2.5V or 3.3V	7	pF
C_{PD}	Power Dissipation Capacitance	$V_I = 0V$ or V_{CC}, f = 10 MHz, $V_{CC} = 1.8V$, 2.5V or 3.3V	20	pF

AC Loading and Waveforms

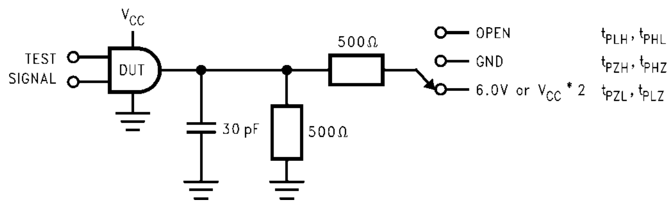


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V; V_{CC} x 2 at V_{CC} = 2.5V ± 0.2V; 1.8V ± 0.15V
t_{PZH}, t_{PHZ}	GND

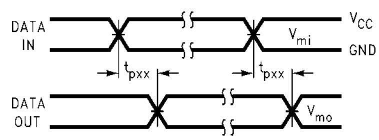


FIGURE 2. Waveform for Inverting and Non-inverting Functions

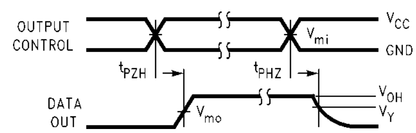


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

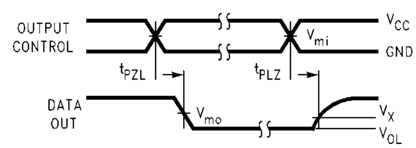
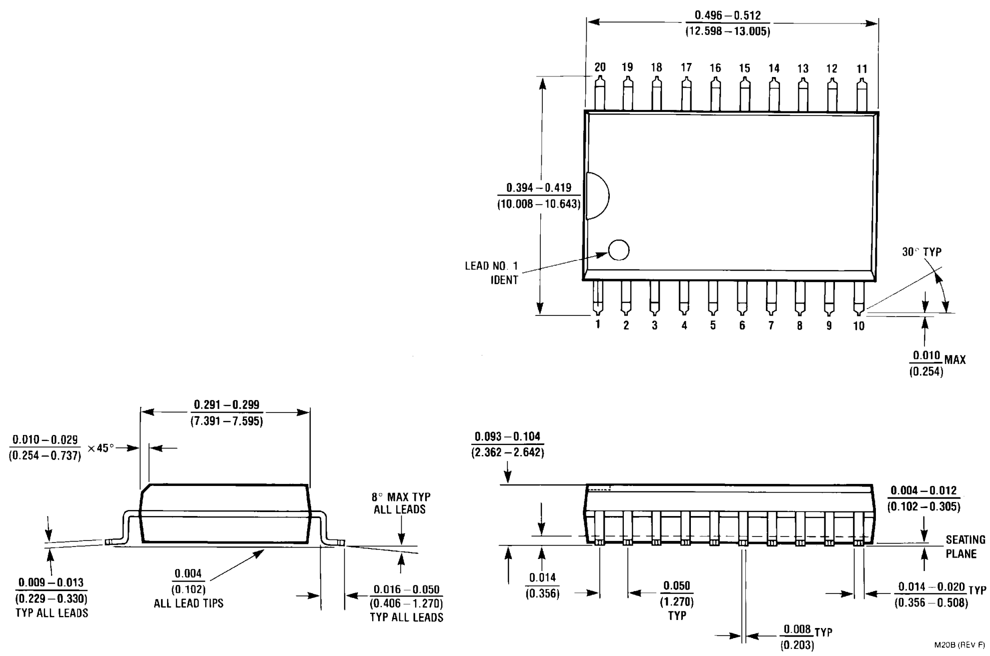


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

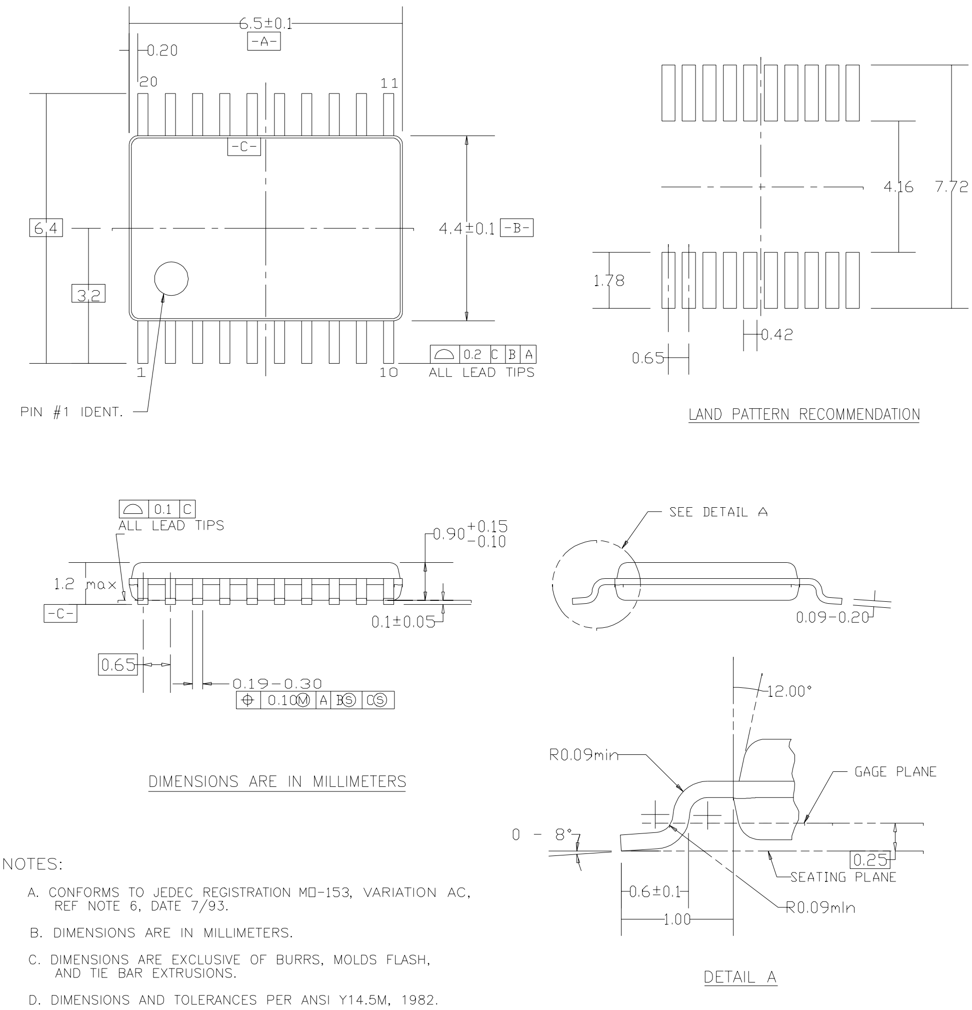
Symbol	V_{CC}		
	3.3V ± 0.3V	**2.5V ± 0.2V**	**1.8V ± 0.15V**
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_x	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_y	V_{OH} – 0.3V	V_{OH} – 0.15V	V_{OH} – 0.15V

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20