FAIRCHILD SEMICONDUCTOR™

September 1995
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74VHC132
Quad 2-Input NAND Schmitt Trigger

General Description

The VHC132 is an advanced high speed CMOS 2-input NAND Schmitt Trigger Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to Bipolar Schottky TTL while maintaining the CMOS low power dissipation. Pin configuration and function are the same as the VHC00 but the inputs have hysteresis between the positive-going and negative-going input thresholds, which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Thus greater noise margin then conventional gates is provided. An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

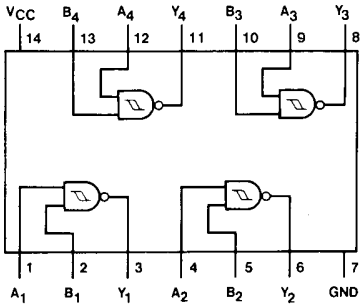
- High Speed: t_{PD} = 3.9 ns (typ) at V_{CC} = 5 V
- Power down protection is provided on all inputs
- Low power dissipation: I_{CC} = 2 μA (max) at T_A = 25°C
- Low noise: V_{OLP} = 0.8 V (max)
- Pin and function compatible with 74HC132

Ordering Code:

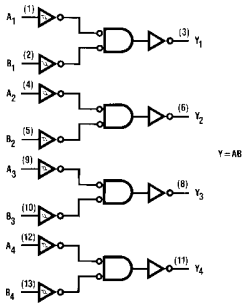
Order Number	Package Number	Package Description
74VHC132M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74VHC132SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC132MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC132N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Logic Diagram



Pin Descriptions

Pin Names	Description
A_n, B_n	Inputs
Y_n	Outputs

Truth Table

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Input Voltage (V_{IN})	–0.5V to +7.0V
DC Output Voltage (V_{OUT})	–0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	–20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	–65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	–40°C to +85°C

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = –40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_P	Positive	3.0			2.20		2.20			
	Threshold Voltage	4.5			3.15		3.15	V		
		5.5			3.85		3.85			
V_N	Negative	3.0	0.90			0.90				
	Threshold Voltage	4.5	1.35			1.35		V		
		5.5	1.65			1.65				
V_H	Hysteresis	3.0	0.30		1.20	0.30	1.20			
	Output Voltage	4.5	0.40		1.40	0.40	1.40	V		
		5.5	0.50		1.60	0.50	1.60			
V_{OH}	HIGH Level	2.0	1.9	2.0		1.9			V_{IN} = V_{IH}	I_{OH} = –50 µA
	Output Voltage	3.0	2.9	3.0		2.9		V	or V_{IL}	
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = –4 mA
		4.5	3.94			3.80				I_{OH} = –8 mA
V_{OL}	LOW Level	2.0		0.0	0.1		0.1		V_{IN} = V_{IH}	I_{OL} = 50 µA
	Output Voltage	3.0		0.0	0.1		0.1	V	or V_{IL}	
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	µA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0		20.0	µA	V_{IN} = V_{CC} or GND	

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$		Units	Conditions
			Typ	Limit		
V_{OLP} (Note 3)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.3	0.8	V	$C_L = 50$ pF
V_{OLV} (Note 3)	Quiet Output Maximum Dynamic V_{OL}	5.0	−0.3	−0.8	V	$C_L = 50$ pF
V_{IHD} (Note 3)	Maximum HIGH Level Dynamic Input Voltage	5.0		3.5	V	$C_L = 50$ pF
V_{ILD} (Note 3)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	$C_L = 50$ pF

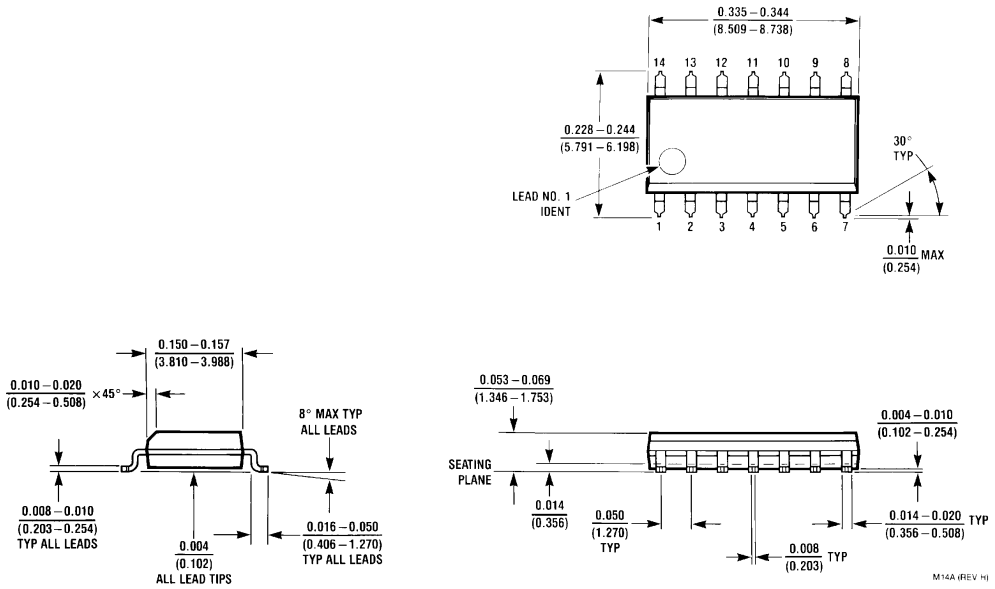
Note 3: Parameter guaranteed by design

AC Electrical Characteristics

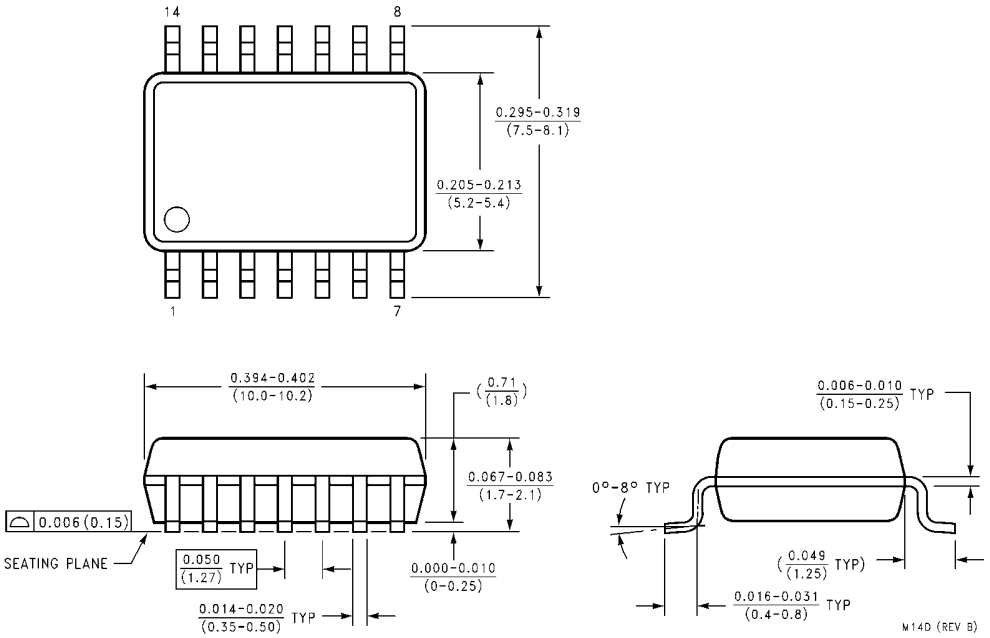
Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PHL} t_{PLH}	Propagation Delay	3.3 ± 0.3		6.1	11.9	1.0	14.0	ns	$C_L = 15$ pF
				8.0	15.4	1.0	17.5		$C_L = 50$ pF
		5.0 ± 0.5		3.9	7.7	1.0	9.0	ns	$C_L = 15$ pF
				5.9	9.7	1.0	11.0		$C_L = 50$ pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			16				pF	(Note 4)

Note 4: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = $C_{PD} * V_{CC} * I_{IN} + I_{CC}/4$ (per gate)

Physical Dimensions inches (millimeters) unless otherwise noted

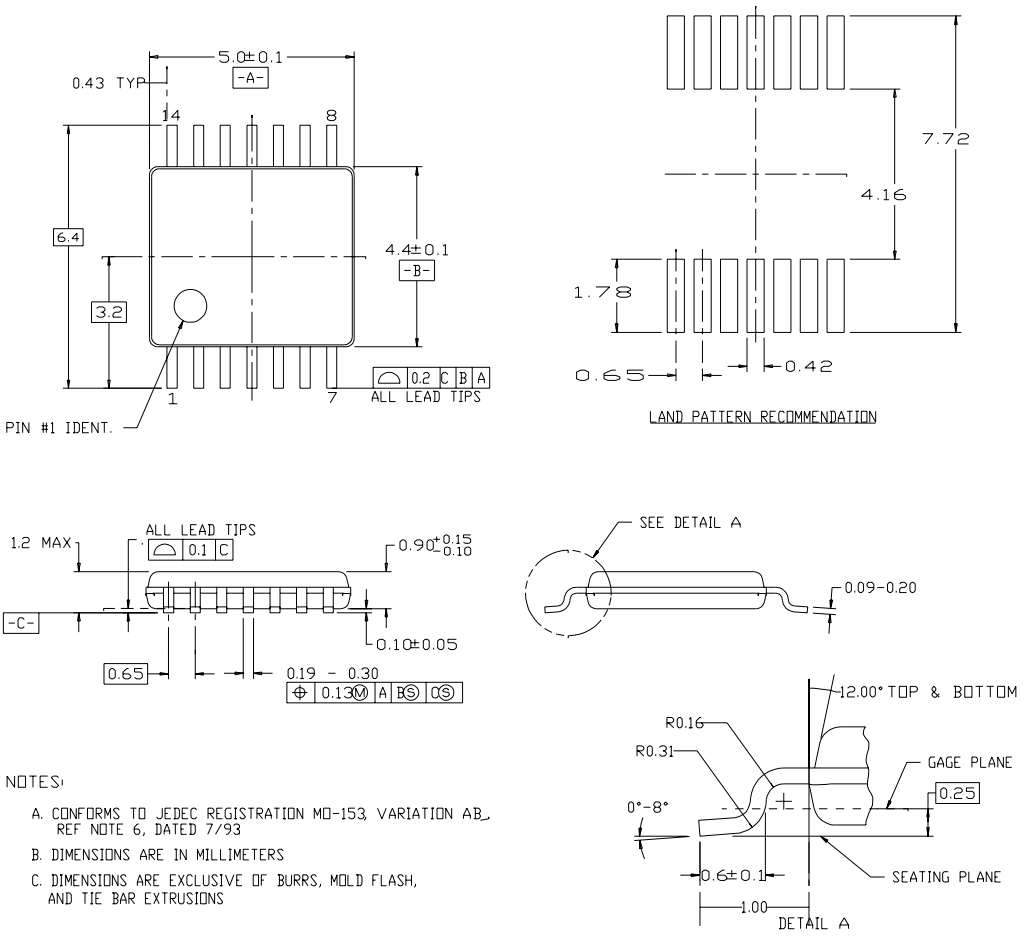


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A



14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

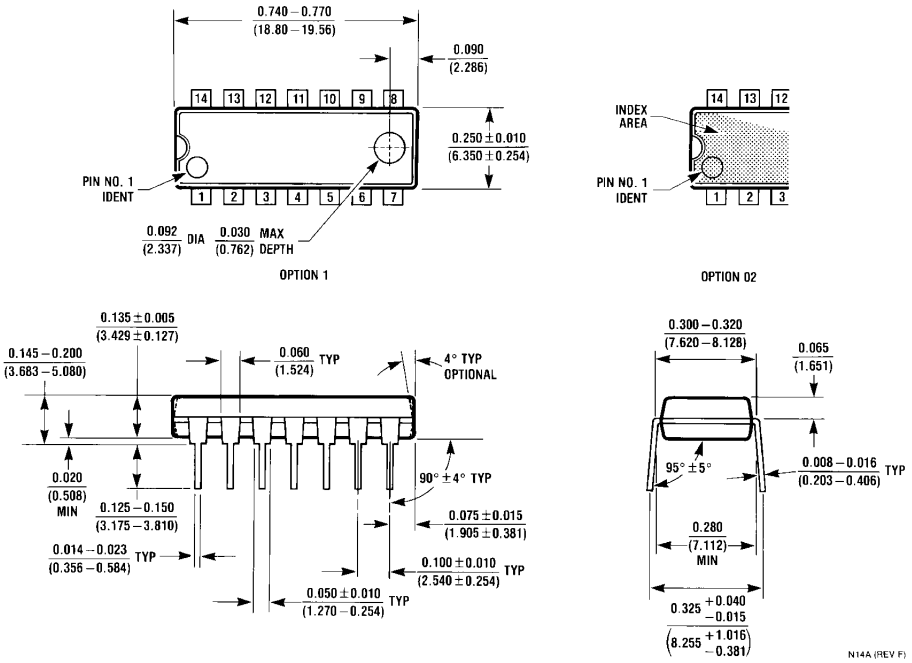
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A