

74VHC163 4-Bit Binary Counter with Synchronous Clear

General Description

The VHC163 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC163 is a high-speed synchronous modulo-16 binary counter. This device is synchronously presettable for application in programmable dividers and has two types of Count Enable inputs plus a Terminal Count output for versatility in forming multistage counters. The CLK input is active on the rising edge. Both \overline{PE} and \overline{MR} inputs are active on low logic level. Presetting is synchronous to rising edge of CLK and the Clear function of the VHC163 is synchronous to CLK. Two enable inputs (ENP and ENT) and Carry Output are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

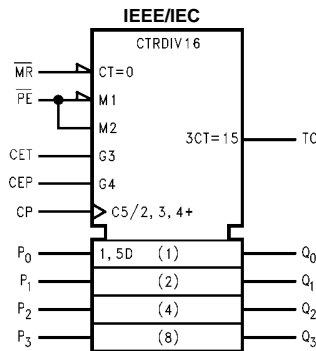
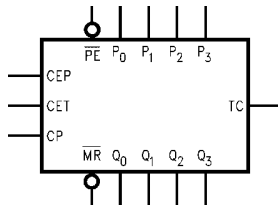
- High speed: $f_{MAX} = 185$ MHz (typ) at $V_{CC} = 5V$
- Low power dissipation: $I_{CC} = 4$ μA (max) at $T_A = 25^\circ C$
- Synchronous counting and loading
- High-speed synchronous expansion
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Power down protection is provided on all inputs.
- Low noise: $V_{OLP} = 0.8V$ (max)
- Pin and function compatible with 74HC163

Ordering Code:

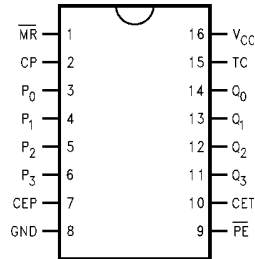
| Order Number | Package Number | Package Description |
|--------------|----------------|-----------------------------------------------------------------------------|
| 74VHC163M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| 74VHC163SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74VHC163MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74VHC163N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

| Pin Names | Description |
|-----------------|--------------------------------|
| CEP | Count Enable Parallel Input |
| CET | Count Enable Trickle Input |
| CP | Clock Pulse Input |
| \overline{MR} | Synchronous Master Reset Input |
| P_0 – P_3 | Parallel Data Inputs |
| \overline{PE} | Parallel Enable Inputs |
| Q_0 – Q_3 | Flip-Flop Outputs |
| TC | Terminal Count Output |

Functional Description

The VHC163 counts in modulo-16 binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: synchronous reset, parallel load, count-up and hold. Four control inputs—Synchronous Reset (\overline{MR}), Parallel Enable (\overline{PE}), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on \overline{MR} overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on \overline{PE} overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With \overline{PE} and \overline{MR} HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The VHC163 uses D-type edge-triggered flip-flops and changing the \overline{MR} , \overline{PE} , CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchro-

nous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to TC delay of the first stage, plus the cumulative CET to TC delays of the intermediate stages, plus the CET to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to TC delay of the first stage plus the CEP to CP setup time of the last stage. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters.

Logic Equations: Count Enable = $CEP \cdot CET \cdot \overline{PE}$
 $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$

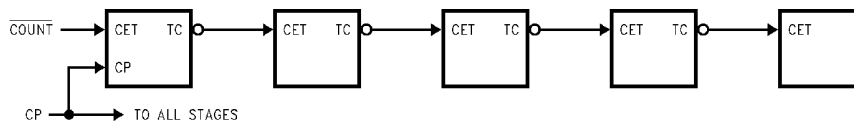


FIGURE 1.

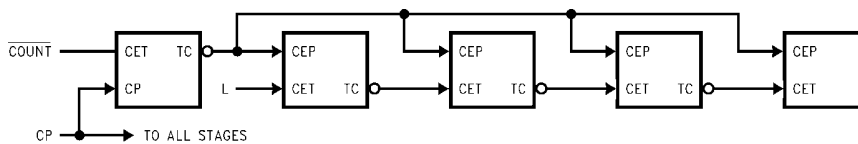


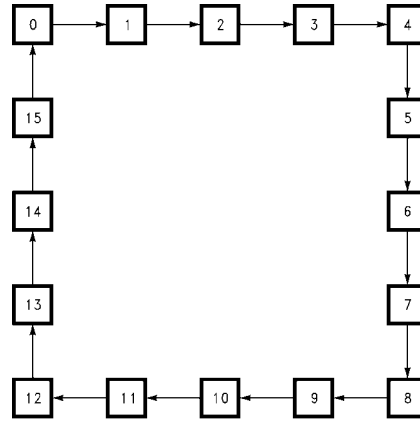
FIGURE 2.

Mode Select Table

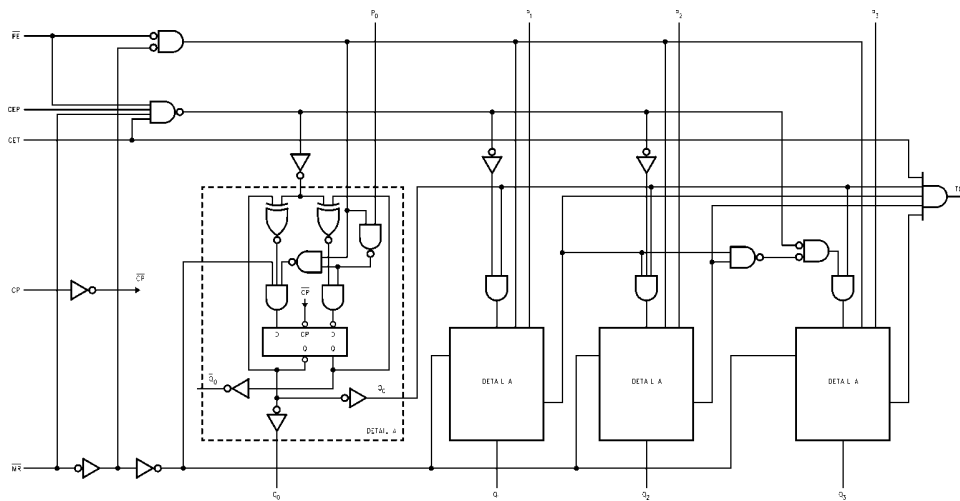
| \overline{MR} | \overline{PE} | CET | CEP | Action on the Rising Clock Edge (↗) |
|-----------------|-----------------|-----|-----|-------------------------------------|
| L | X | X | X | Reset (Clear) |
| H | L | X | X | Load ($P_n \rightarrow Q_n$) |
| H | H | H | H | Count (Increment) |
| H | H | L | X | No Change (Hold) |
| H | H | X | L | No Change (Hold) |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

State Diagram



Block Diagram



Absolute Maximum Ratings (Note 1)

| | |
|-------------------------------------------------------|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Voltage (V_{IN}) | -0.5V to +7.0V |
| DC Output Voltage (V_{OUT}) | -0.5V to $V_{CC} + 0.5V$ |
| Input Diode Current (I_{IK}) | -20 mA |
| Output Diode Current (I_{OK}) | ± 20 mA |
| DC Output Current (I_{OUT}) | ± 25 mA |
| DC V_{CC}/GND Current (I_{CC}) | ± 50 mA |
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Lead Temperature (T_L) (Soldering, 10 seconds) | 260°C |

Recommended Operating**Conditions** (Note 2)

| | |
|-----------------------------------------|---------------------------------------|
| Supply Voltage (V_{CC}) | 2.0V to +5.5V |
| Input Voltage (V_{IN}) | 0V to +5.5V |
| Output Voltage (V_{OUT}) | 0V to V_{CC} |
| Operating Temperature (T_{OPR}) | -40°C to +85°C |
| Input Rise and Fall Time (t_r, t_f) | |
| | $V_{CC} = 3.3V \pm 0.3V$ 0 ~ 100 ns/V |
| | $V_{CC} = 5.0V \pm 0.5V$ 0 ~ 20 ns/V |

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = 25^\circ\text{C}$ | | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | Units | Conditions | |
|----------|--------------------------|-----------------|--------------------------|--------------|-----------|-------------------------------------------------|-----------|---------------|----------------------------------|------------------------------------------------------|
| | | | Min | Typ | Max | Min | Max | | | |
| V_{IH} | HIGH Level | 2.0 | 1.50 | | | 1.50 | | V | | |
| | Input Voltage | 3.0 – 5.5 | 0.7 V_{CC} | | | 0.7 V_{CC} | | | | |
| V_{IL} | LOW Level | 2.0 | | 0.50 | | 0.50 | | V | | |
| | Input Voltage | 3.0 – 5.5 | | 0.3 V_{CC} | | 0.3 V_{CC} | | | | |
| V_{OH} | HIGH Level | 2.0 | 1.9 | 2.0 | | 1.9 | | V | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OH} = -50 \mu\text{A}$ |
| | | 3.0 | 2.9 | 3.0 | | 2.9 | | | | |
| | Output Voltage | 4.5 | 4.4 | 4.5 | | 4.4 | | | | $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$ |
| | | 3.0 | 2.58 | | | 2.48 | | | | |
| V_{OL} | LOW Level | 2.0 | | 0.0 | 0.1 | | 0.1 | V | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OL} = 50 \mu\text{A}$ |
| | | 3.0 | | 0.0 | 0.1 | | 0.1 | | | |
| | Output Voltage | 4.5 | | 0.0 | 0.1 | | 0.1 | | | $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$ |
| | | 3.0 | | | 0.36 | | 0.44 | | | |
| | | 4.5 | | | 0.36 | | 0.44 | | | |
| I_{IN} | Input Leakage Current | 0 – 5.5 | | | ± 0.1 | | ± 1.0 | μA | $V_{IN} = 5.5V$ or GND | |
| I_{CC} | Quiescent Supply Current | 5.5 | | | 4.0 | | 40.0 | μA | $V_{IN} = V_{CC}$ or GND | |

Noise Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = 25^\circ\text{C}$ | | Units | Conditions |
|-----------------------|-----------------------|-----------------|--------------------------|--------|-------|-----------------------|
| | | | Typ | Limits | | |
| V_{OLP} (Note 3) | Quiet Output Maximum | 5.0 | 0.4 | 0.8 | V | $C_L = 50 \text{ pF}$ |
| | Dynamic V_{OL} | | | | | |
| V_{OLV} (Note 3) | Quiet Output Minimum | 5.0 | -0.4 | -0.8 | V | $C_L = 50 \text{ pF}$ |
| | Dynamic V_{OL} | | | | | |
| V_{IHD} (Note 3) | Minimum HIGH Level | 5.0 | | 3.5 | V | $C_L = 50 \text{ pF}$ |
| | Dynamic Input Voltage | | | | | |
| V_{ILD} (Note 3) | Maximum LOW Level | 5.0 | | 1.5 | V | $C_L = 50 \text{ pF}$ |
| | Dynamic Input Voltage | | | | | |

Note 3: Parameter guaranteed by design.

| AC Electrical Characteristics | | | | | | | | | |
|-------------------------------|------------------------------------------------|------------------------|-----------------------|------|-----|--------------------------------|-----|------------------------|------------|
| Symbol | Parameter | V _{CC} (V) | T _A = 25°C | | | T _A = -40° to +85°C | | Units | Conditions |
| | | | Min | Typ | Max | Min | Max | | |
| t _{PLH} | Propagation Delay Time (CP-Q _n) | 3.3 ± 0.3 | 8.3 | 12.8 | 1.0 | 15.0 | ns | C _L = 15 pF | |
| t _{PHL} | | | 10.8 | 16.3 | 1.0 | 18.5 | | C _L = 50 pF | |
| | | 5.0 ± 0.5 | 4.9 | 8.1 | 1.0 | 9.5 | ns | C _L = 15 pF | |
| | | | 6.4 | 10.1 | 1.0 | 11.5 | | C _L = 50 pF | |
| t _{PLH} | Propagation Delay Time (CP-TC, Count) | 3.3 ± 0.3 | 8.7 | 13.6 | 1.0 | 16.0 | ns | C _L = 15 pF | |
| t _{PHL} | | | 11.2 | 17.1 | 1.0 | 19.5 | | C _L = 50 pF | |
| | | 5.0 ± 0.5 | 4.9 | 8.1 | 1.0 | 9.5 | ns | C _L = 15 pF | |
| | | | 6.4 | 10.1 | 1.0 | 11.5 | | C _L = 50 pF | |
| t _{PLH} | Propagation Delay Time (CP-TC, Load) | 3.3 ± 0.3 | 11.0 | 17.2 | 1.0 | 20.0 | ns | C _L = 15 pF | |
| t _{PHL} | | | 13.5 | 20.7 | 1.0 | 23.5 | | C _L = 50 pF | |
| | | 5.0 ± 0.5 | 6.2 | 10.3 | 1.0 | 12.0 | ns | C _L = 15 pF | |
| | | | 7.7 | 12.3 | 1.0 | 14.0 | | C _L = 50 pF | |
| t _{PLH} | Propagation Delay Time (CET-TC) | 3.3 ± 0.3 | 7.5 | 12.3 | 1.0 | 14.5 | ns | C _L = 15 pF | |
| t _{PHL} | | | 10.5 | 15.8 | 1.0 | 18.0 | | C _L = 50 pF | |
| | | 5.0 ± 0.5 | 4.9 | 8.1 | 1.0 | 9.5 | ns | C _L = 15 pF | |
| | | | 6.4 | 10.1 | 1.0 | 11.5 | | C _L = 50 pF | |
| f _{MAX} | Maximum Clock Frequency | 3.3 ± 0.3 | 80 | 130 | 70 | | MHz | C _L = 15 pF | |
| | | | 55 | 85 | 50 | | | C _L = 50 pF | |
| | | 5.0 ± 0.5 | 135 | 185 | 115 | | MHz | C _L = 15 pF | |
| | | | 95 | 125 | 85 | | | C _L = 50 pF | |
| C _{IN} | Input Capacitance | | 4 | 10 | 10 | | pF | V _{CC} = Open | |
| C _{PD} | Power Dissipation Capacitance | | 23 | | | | pF | (Note 4) | |

Note 4: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr) = C_{PD} * V_{CC} * f_{IN} + I_{CC}.

When the outputs drive a capacitive load, total current consumption is the sum of C_{PD}, and ΔI_{CC} which is obtained from the following formula:

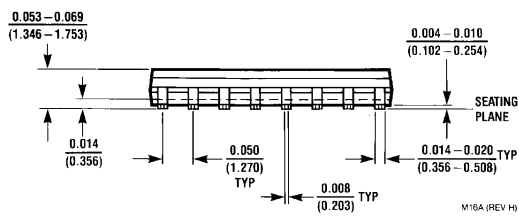
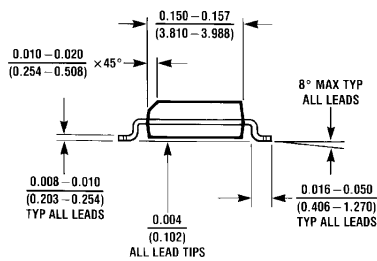
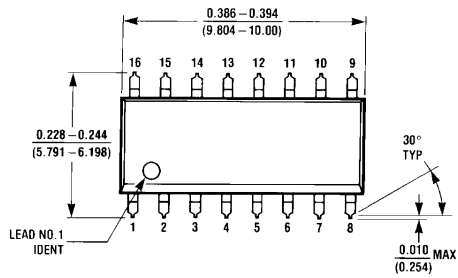
$$\Delta I_{CC} = F_{CP} \cdot V_{CC} \left(\frac{C_{Q0}}{2} + \frac{C_{Q1}}{4} + \frac{C_{Q2}}{8} + \frac{C_{Q3}}{16} + \frac{C_{TC}}{16} \right)$$

C_{Q0}-C_{Q3} and C_{TC} are the capacitances at Q0-Q3 and TC, respectively. F_{CP} is the input frequency of the CP.

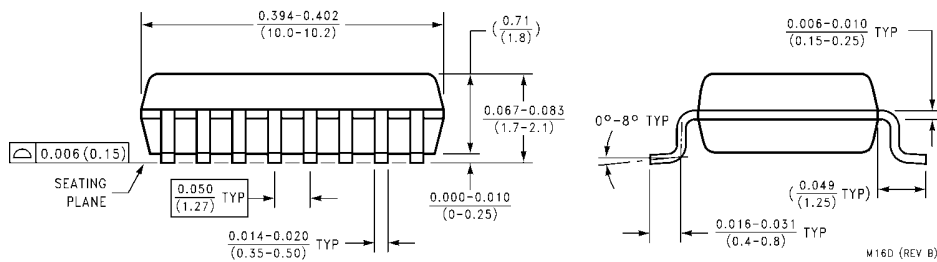
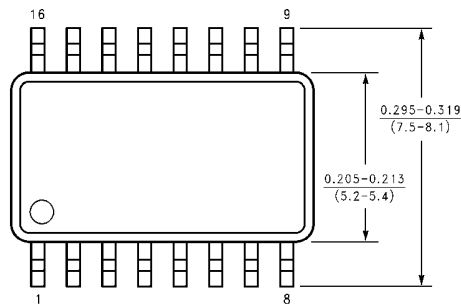
| AC Operating Requirements | | | | | | |
|---------------------------|-----------------------------------------------------|------------------------------------|-----------------------|--------------------|------------------------|-------|
| Symbol | Parameter | V _{CC} (Note 5) (V) | T _A = 25°C | | T _A = -40°C | Units |
| | | | Typ | Guaranteed Minimum | | |
| t _S | Minimum Setup Time (P _n -CP) | 3.3 | | 5.5 | 6.5 | ns |
| | | 5.0 | | 4.5 | 4.5 | |
| t _S | Minimum Setup Time ($\overline{\text{PE}}$ -CP) | 3.3 | | 8.0 | 9.5 | ns |
| | | 5.0 | | 5.0 | 6.0 | |
| t _S | Minimum Setup Time (CEP or CET-CP) | 3.3 | | 7.5 | 9.0 | ns |
| | | 5.0 | | 5.0 | 6.0 | |
| t _S | Minimum Setup Time ($\overline{\text{MR}}$ -CP) | 3.3 | | 4.0 | 4.0 | ns |
| | | 5.0 | | 3.5 | 3.5 | |
| t _H | Minimum Hold Time (P _n -CP) | 3.3 | | 1.0 | 1.0 | ns |
| | | 5.0 | | 1.0 | 1.0 | |
| t _H | Minimum Hold Time ($\overline{\text{PE}}$ -CP) | 3.3 | | 1.0 | 1.0 | ns |
| | | 5.0 | | 1.0 | 1.0 | |
| t _H | Minimum Hold Time (CEP or CET-CP) | 3.3 | | 1.0 | 1.0 | ns |
| | | 5.0 | | 1.0 | 1.0 | |
| t _H | Minimum Hold Time ($\overline{\text{MR}}$ -CP) | 3.3 | | 1.0 | 1.0 | ns |
| | | 5.0 | | 1.5 | 1.5 | |
| t _{W(L)} | Minimum Pulse Width | 3.3 | | 5.0 | 5.0 | ns |
| t _{W(H)} | CP (Count) | 5.0 | | 5.0 | 5.0 | |

Note 5: V_{CC} is 3.3 ± 0.3V or 5.0 ± 0.5V

Physical Dimensions inches (millimeters) unless otherwise noted

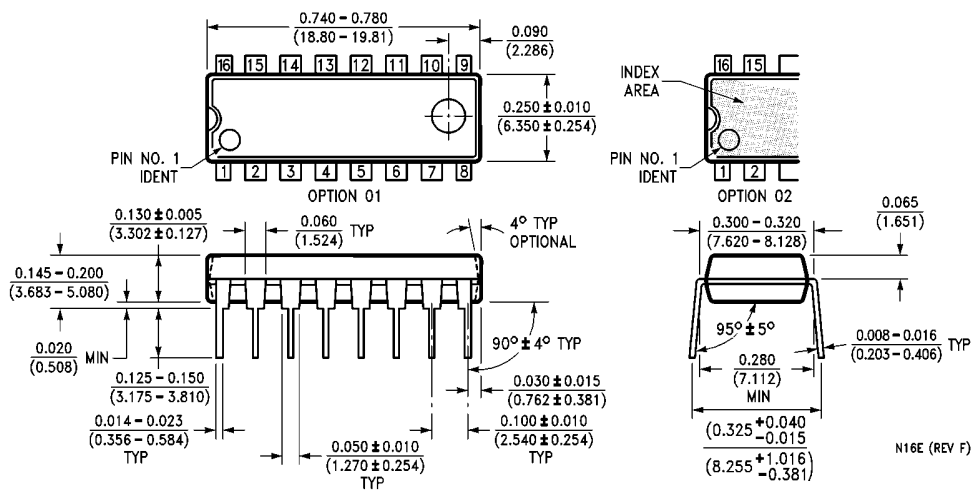


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

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