FAIRCHILD

SEMICONDUCTOR™

74VHC541
Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The VHC541 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC541 is an octal buffer/line driver designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers.

This device is similar in function to the VHC244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

■ High Speed: t_{PD} = 3.5 ns (typ) at V_{CC} = 5V

■ Low power dissipation: I_{CC} = 4 μA (max) at T_A = 25°C

■ High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)

■ Power down protection is provided on all inputs

■ Low noise: V_{OLP} = 0.9V (typ)

■ Pin and function compatible with 74HC541

Ordering Code:

Order Number	Package Number	Package Description
74VHC541M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74VHC541SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC541N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Logic Symbol

IEEE/IEC
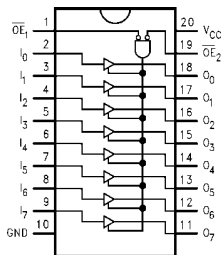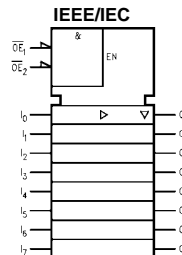
Pin Descriptions

Pin Names	Descriptions
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I_0 - I_7	Inputs
O_0 - O_7	3-STATE Outputs

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level   X = Immaterial
L = LOW Voltage Level   Z = High Impedance

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ~ 20 ns/V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	2.0	1.50			1.50		V		
		3.0 – 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Input Voltage	2.0			0.50		0.50	V		
		3.0 – 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50$ μA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		$I_{OH} = -4$ mA
		4.5	3.94			3.80				$I_{OH} = -8$ mA
V_{OL}	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50$ μA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		$I_{OL} = 4$ mA
		4.5			0.36		0.44			$I_{OL} = 8$ mA
I_{OZ}	3-STATE Output Off-State Current	5.5			±0.25		±2.5	μA	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	
I_{IN}	Input Leakage Current	0 – 5.5			±0.1		±1.0	μA	$V_{IN} = 5.5$V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	$V_{IN} = V_{CC}$ or GND	

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$		Units	Conditions
			Typ	Limits		
V_{OLP} (Note 3)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.9	1.2	V	$C_L = 50$ pF
V_{OLV} (Note 3)	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.8	−1.0	V	$C_L = 50$ pF
V_{IHD} (Note 3)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	$C_L = 50$ pF
V_{ILD} (Note 3)	Maximum HIGH Level Dynamic Input Voltage	5.0		1.5	V	$C_L = 50$ pF

Note 3: Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
t_{PLH}	Propagation Delay	3.3 ± 0.3		5.0	7.0	1.0	8.5	ns		C_L = 15 pF
t_{PHL}	Time			7.5	10.5	1.0	12.0			C_L = 50 pF
		5.0 ± 0.5		3.5	5.0	1.0	6.0	ns		C_L = 15 pF
				5.0	7.0	1.0	8.0			C_L = 50 pF
t_{PZL}	3-STATE Output	3.3 ± 0.3		6.8	10.5	1.0	12.5	ns	R_L = 1 kΩ	C_L = 15 pF
t_{PZH}	Enable Time			9.3	14.0	1.0	16.0			C_L = 50 pF
		5.0 ± 0.5		4.7	7.2	1.0	8.5	ns		C_L = 15 pF
				6.2	9.2	1.0	10.5			C_L = 50 pF
t_{PLZ}	3-STATE	3.3 ± 0.3		11.2	15.4	1.0	17.5		R_L = 1 kΩ	C_L = 50 pF
t_{PHZ}	Output	5.0 ± 0.5		6.0	8.8	1.0	10.0	ns		C_L = 50 pF
	Disable Time									
t_{OSLH}	Output to Output Skew	3.3 ± 0.3			1.5		1.5	ns	(Note 4)	C_L = 50 pF
t_{OSHL}		5.0 ± 0.5			1.0		1.0			C_L = 50 pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open	
C_{OUT}	Output Capacitance			6				pF	V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance			18				pF	(Note 5)	

Note 4: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|$; $t_{OSHL} = |t_{PHLmax} - t_{PHLmin}|$.
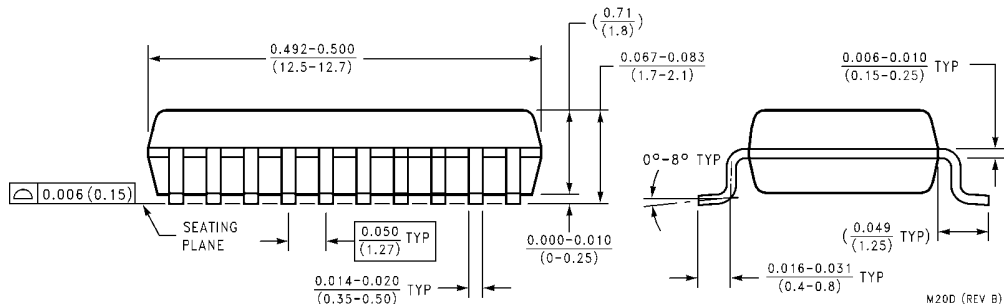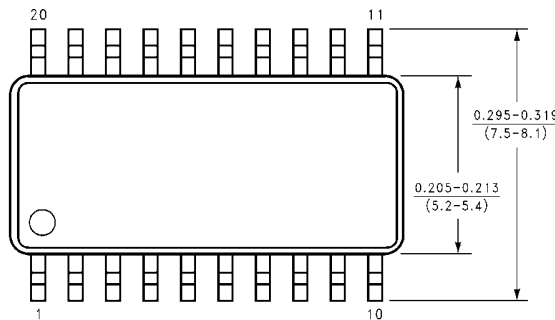
Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (OPR.) $= C_{PD} * V_{CC} * f_{IN} + I_{CC}/8$ (per bit).

Physical Dimensions inches (millimeters) unless otherwise noted

0.496 − 0.512
(12.598 − 13.005)

20 19 18 17 16 15 14 13 12 11

0.394 − 0.419
(10.008 − 10.643)

LEAD NO. 1
IDENT

1 2 3 4 5 6 7 8 9 10

30° TYP

0.010 MAX
(0.254)

0.291 − 0.299
(7.391 − 7.595)

0.010 − 0.029
(0.254 − 0.737) × 45°

8° MAX TYP
ALL LEADS

0.009 − 0.013
(0.229 − 0.330)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.093 − 0.104
(2.362 − 2.642)

0.004 − 0.012
(0.102 − 0.305)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
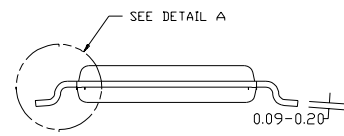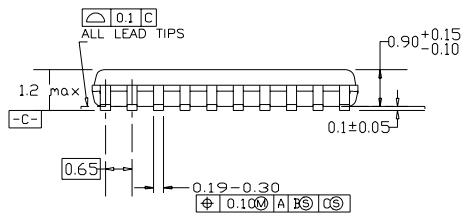(0.203)

0.014 − 0.020 TYP
(0.356 − 0.508)
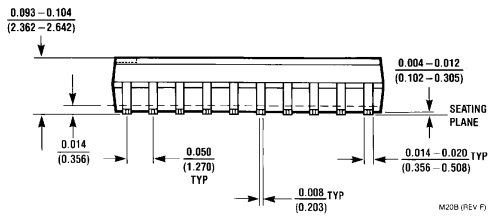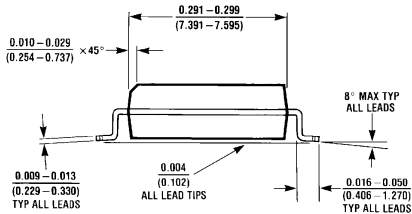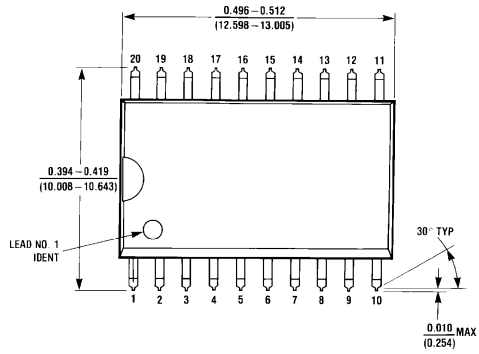
M20B (REV F)

20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

20   11

0.295−0.319
(7.5−8.1)

0.205−0.213
(5.2−5.4)

1   10

(0.71)
(1.8)

0.492−0.500
(12.5−12.7)

0.067−0.083
(1.7−2.1)

0.006−0.010 TYP
(0.15−0.25)

△ 0.006 (0.15)

SEATING
PLANE

0.050 TYP
(1.27)

0.014−0.020 TYP
(0.35−0.50)

0.000−0.010
(0−0.25)

0°−8° TYP

(0.049 TYP)
(1.25)

0.016−0.031 TYP
(0.4−0.8)

M20D (REV B)

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

6.5±0.1
-A-

0.20

20   11
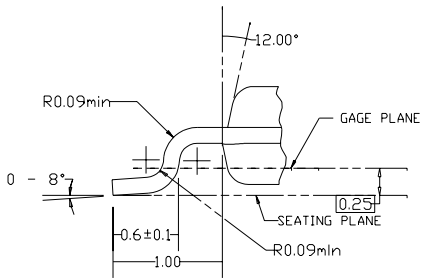
-C-

6.4   4.4±0.1 -B-

3.2

1   10

PIN #1 IDENT.

⌒ 0.2 C B A
ALL LEAD TIPS

LAND PATTERN RECOMMENDATION

4.16   7.72

1.78

0.42

0.65

⌒ 0.1 C
ALL LEAD TIPS

0.90 +0.15 −0.10

1.2 max

-C-

0.1±0.05

0.65

0.19−0.30
⊕ 0.10 M A B S C S

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.09−0.20

12.00°

R0.09min

GAGE PLANE
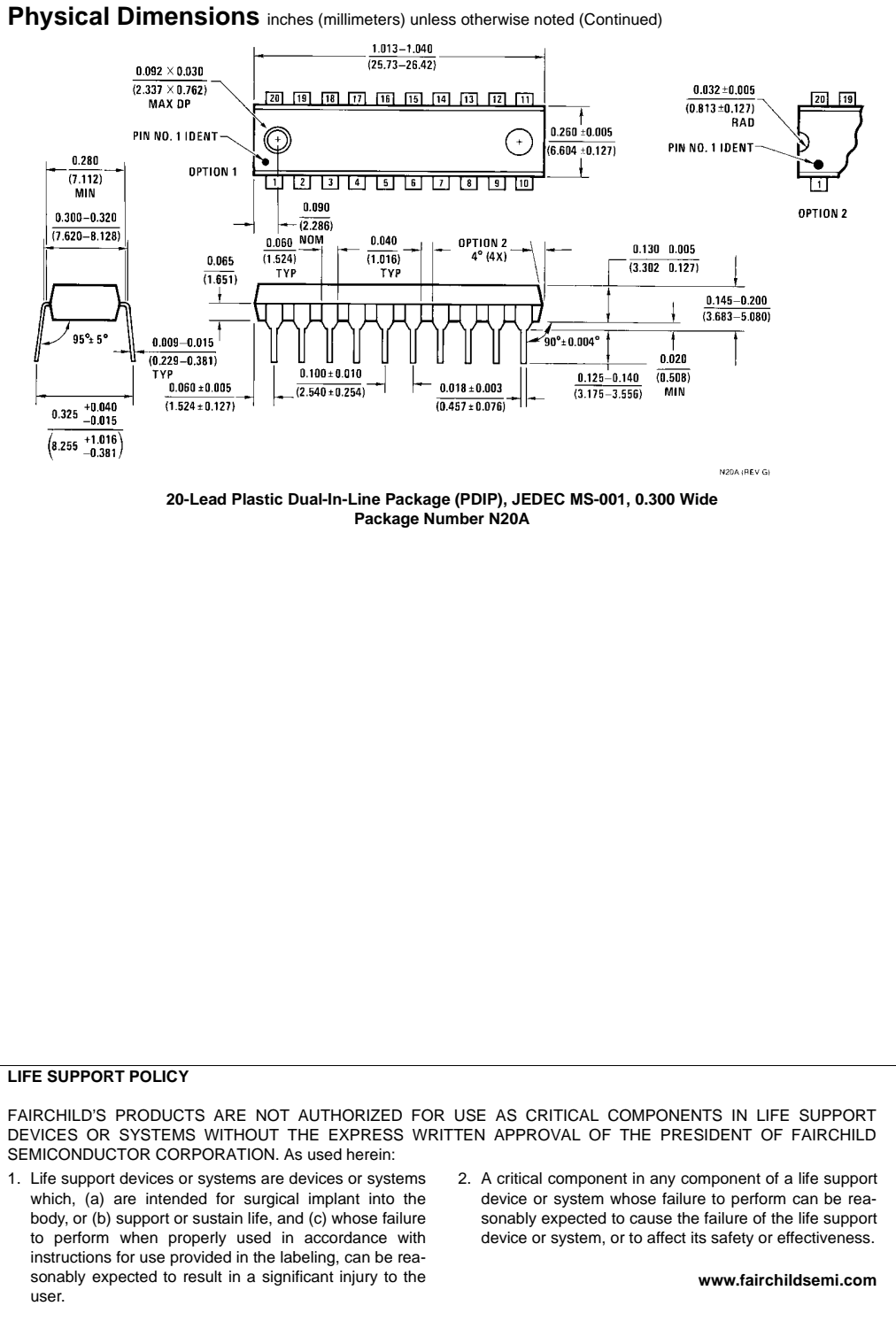
0 - 8°

0.25

SEATING PLANE

0.6±0.1

R0.09min

1.00
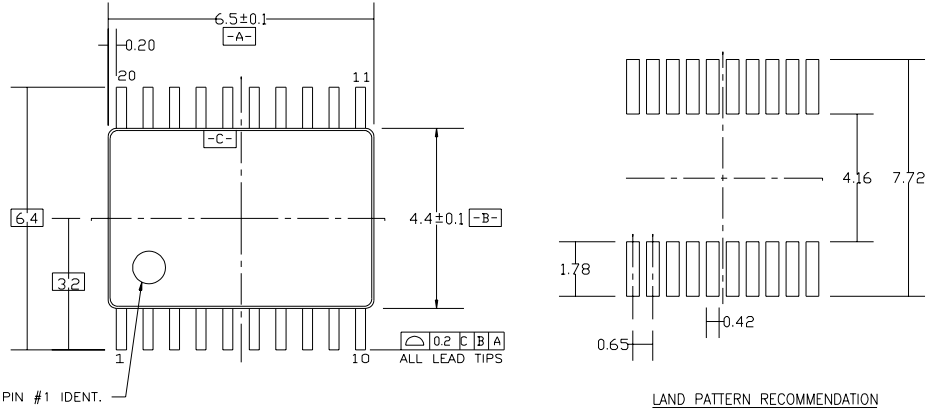
DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC,
   REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH,
   AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.092 × 0.030
(2.337 × 0.762)
MAX DP

PIN NO. 1 IDENT

OPTION 1

1.013−1.040
(25.73−26.42)

0.260 ±0.005
(6.604 ±0.127)

0.032 ±0.005
(0.813 ±0.127)
RAD

PIN NO. 1 IDENT

OPTION 2

0.280
(7.112)
MIN

0.300−0.320
(7.620−8.128)

0.065
(1.651)

95° ± 5°

0.009−0.015
(0.229−0.381)
TYP

0.060 ±0.005
(1.524 ±0.127)

0.325 +0.040 −0.015
(8.255 +1.016 −0.381)

0.090
(2.286)

0.060 NOM
(1.524)
TYP

0.040
(1.016)
TYP

OPTION 2
4° (4X)

0.100 ±0.010
(2.540 ±0.254)

0.018 ±0.003
(0.457 ±0.076)

90° ±0.004°

0.125−0.140
(3.175−3.556)

0.130 0.005
(3.302 0.127)

0.145−0.200
(3.683−5.080)

0.020
(0.508)
MIN

N20A (REV G)

20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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