

## 74VHCT74A Dual D-Type Flip-Flop with Preset and Clear

### General Description

The VHCT74A is an advanced high speed CMOS Dual D-Type Flip-Flop fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The signal level applied to the D INPUT is transferred to the Q OUTPUT during the positive going transition of the CK pulse. CLR and PR are independent of the CK and are accomplished by setting the appropriate input LOW.

Protection circuits ensure that 0V to 7V can be applied to the input pins without regard to the supply voltage and to the output pins with  $V_{CC} = 0V$ . These circuits prevent device destruction due to mismatched supply and input/

output voltages. This device can be used to interface 3V to 5V systems and two supply systems such as battery backup.

### Features

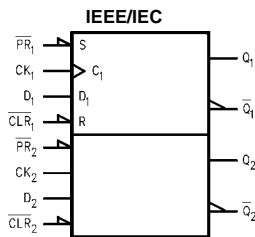
- High speed:  $f_{MAX} = 160$  MHz (typ) at  $T_A = 25^\circ C$
- High noise immunity:  $V_{IH} = 2.0V$ ,  $V_{IL} = 0.8V$
- Power down protection is provided on all inputs and outputs
- Low power dissipation:  
 $I_{CC} = 2 \mu A$  (max) at  $T_A = 25^\circ C$
- Pin and function compatible with 74HCT74

### Ordering Code:

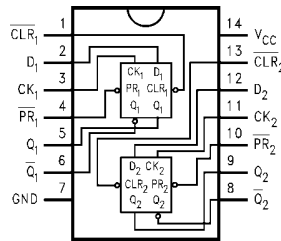
Order Number	Package Number	Package Description
74VHCT74AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74VHCT74ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHCT74AMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHCT74AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



### Pin Descriptions

Pin Names	Description
$D_1, D_2$	Data Inputs
$CK_1, CK_2$	Clock Pulse Inputs
$\overline{CLR}_1, \overline{CLR}_2$	Direct Clear Inputs
$\overline{PR}_1, \overline{PR}_2$	Direct Preset Inputs
$Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$	Outputs

### Truth Table

Inputs				Outputs		Function
CLR	PR	D	CK	Q	Q	
L	H	X	X	L	H	Clear Preset
H	L	X	X	H	L	
L	L	X	X	H	H	
H	H	L	~	L	H	No Change
H	H	H	~	H	L	
H	H	X	~	$Q_n$	$Q_n$	
H	H	X	~	$Q_n$	$Q_n$	

**Absolute Maximum Ratings** (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-0.5V to +7.0V
DC Output Voltage ( $V_{OUT}$ )	
(Note 2)	-0.5V to $V_{CC} + 0.5V$
(Note 3)	-0.5V to 7.0V
Input Diode Current ( $I_{IK}$ )	-20 mA
Output Diode Current ( $I_{OK}$ )	
(Note 4)	$\pm 20$ mA
DC Output Current ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ /GND Current ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Lead Temperature ( $T_L$ )	
Soldering (10 seconds)	260°C

**Recommended Operating****Conditions** (Note 5)

Supply Voltage ( $V_{CC}$ )	4.5V to 5.5V
Input Voltage ( $V_{IN}$ )	0V to +5.5V
Output Voltage ( $V_{OUT}$ )	
(Note 2)	0V to $V_{CC}$
(Note 3)	0V to 5.5V
Operating Temperature ( $T_{OPR}$ )	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ )	
$V_{CC} = 5.0V \pm 0.5V$	0 ns/V ~ 20 ns/V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

**Note 2:** HIGH or LOW state.  $I_{OUT}$  absolute maximum rating must be observed.

**Note 3:**  $V_{CC} = 0V$ .

**Note 4:**  $V_{OUT} < GND, V_{OUT} > V_{CC}$  (Outputs Active)

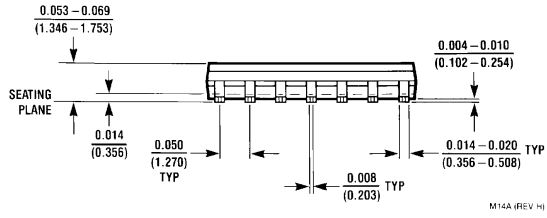
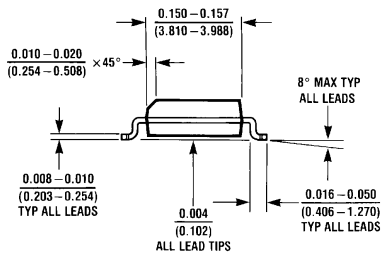
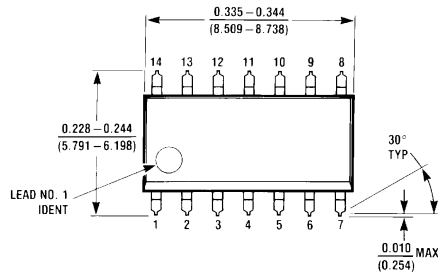
**Note 5:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Typ	Max	Min	Max		
$V_{IH}$	HIGH Level	4.5	2.0			2.0	V		
	Input Voltage	5.5	2.0			2.0			
$V_{IL}$	LOW Level	4.5		0.8		0.8	V		
	Input Voltage	5.5		0.8		0.8			
$V_{OH}$	HIGH Level	4.5	4.40	4.50		4.40	V	$V_{IN} = V_{IH}$ or $V_{IL}$	
	Output Voltage	4.5	3.94			3.80			
$V_{OL}$	LOW Level	4.5		0.0	0.1	0.1	V	$V_{IN} = V_{IH}$ or $V_{IL}$	
	Output Voltage	4.5		0.36		0.44			
$I_{IN}$	Input Leakage Current	0-5.5		$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$	$V_{IN} = 5.5V$ or GND	
$I_{CC}$	Quiescent Supply Current	5.5		2.0		20.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND	
$I_{CCT}$	Maximum $I_{CC}$ /Input	5.5		1.35		1.50	mA	$V_{IN} = 3.4V$ Other Inputs = $V_{CC}$ or GND	
$I_{OFF}$	Output Leakage Current (Power Down State)	0.0		+0.5		+5.0	$\mu\text{A}$	$V_{OUT} = 5.5V$	

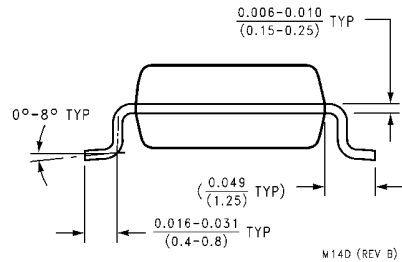
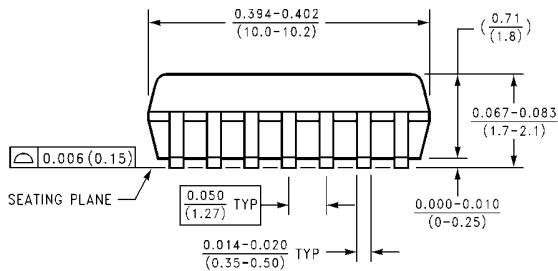
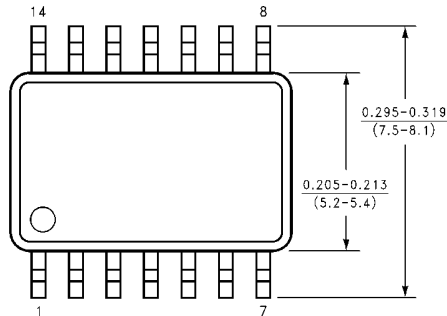
AC Electrical Characteristics									
Symbol	Parameter	V <sub>CC</sub> (V) (Note 6)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	5.0	100	160		80		MHz	C <sub>L</sub> = 15 pF
		5.0	80	140		65			C <sub>L</sub> = 50 pF
t <sub>PLH</sub>	Propagation Delay Time	5.0		5.8	7.8	1.0	9.0	ns	C <sub>L</sub> = 15 pF
t <sub>PHL</sub>	(CK-Q, $\bar{Q}$ )	5.0		6.3	8.8	1.0	10.0		C <sub>L</sub> = 50 pF
t <sub>PLH</sub>	Propagation Delay time	5.0		7.6	10.4	1.0	12.0	ns	C <sub>L</sub> = 15 pF
t <sub>PHL</sub>	(CLR, $\overline{PR}$ -Q, $\bar{Q}$ )	5.0		8.1	11.4	1.0	13.0		C <sub>L</sub> = 50 pF
C <sub>IN</sub>	Input Capacitance			4	10		10	pF	V <sub>CC</sub> = Open
C <sub>PD</sub>	Power Dissipation Capacitance			24				pF	(Note 7)
<p><b>Note 6:</b> V<sub>CC</sub> is 5.0 ± 0.5V</p> <p><b>Note 7:</b> C<sub>PD</sub> is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC</sub> (opr) = C<sub>PD</sub> × V<sub>CC</sub> × f<sub>IN</sub> + I<sub>CC</sub>/2 (per flip-flop).</p>									
AC Operating Requirements									
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40°C to +85°C		Units		
			Typ	Guaranteed Minimum					
t <sub>W(L)</sub> t <sub>W(H)</sub>	Minimum Pulse Width (CK)	5.0 ± 0.5			5.0	5.0	ns		
t <sub>W(L)</sub>	Minimum Pulse Width (CLR, $\overline{PR}$ )	5.0 ± 0.5			5.0	5.0	ns		
t <sub>S</sub>	Minimum Setup Time	5.0 ± 0.5			5.0	5.0	ns		
t <sub>H</sub>	Minimum Hold Time	5.0 ± 0.5			0	0	ns		
t <sub>REM</sub>	Minimum Removal Time (CLR, $\overline{PR}$ )	5.0 ± 0.5			3.5	3.5	ns		

**Physical Dimensions** inches (millimeters) unless otherwise noted



M14A (REV H)

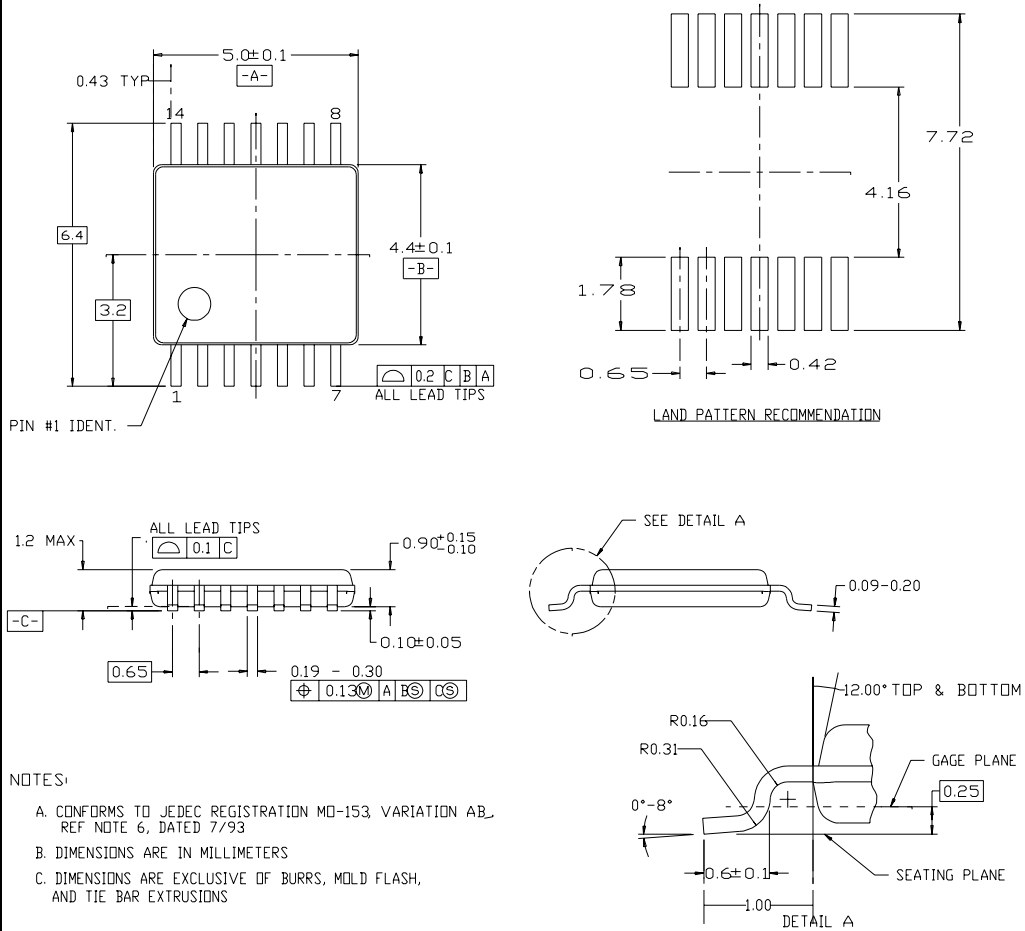
**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A**



M14D (REV B)

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

**OPTION 1**

**OPTION 2**

**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A**

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