

October 1987 Revised January 1999

CD4030C Quad EXCLUSIVE-OR Gate

General Description

The CD4030C EXCLUSIVE-OR gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to $\rm V_{DD}$ and $\rm V_{SS}$.

Features

■ Wide supply voltage range: 3.0V to 15V

■ Low power: 100 nW (typ.)■ Medium speed operation:

 $t_{\mbox{\footnotesize PHL}} = t_{\mbox{\footnotesize PLH}} = 40$ ns (typ.) at $C_L = 15$ pF, 10V supply

■ High noise immunity 0.45 V_{CC} (typ.)

Applications

- Automotive
- · Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- · Remote metering
- Computers

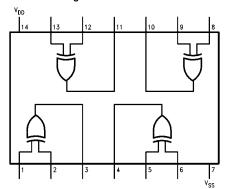
Ordering Code:

Order Number	Package Number	Package Description
CD4030CSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4030CN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP) JEDEC MS-001_0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP and SOP



Truth Table

Α	В	J
0	0	0
1	0	1
0	1	1
1	1	0

1 = HIGH Level 0 = LOW Level

Absolute Maximum Ratings(Note 1)

Power Dissipation (P_D)

 Dual-In-Line
 700 mW

 Small Outline
 500 mW

 Operating V_{DD} Range
 V_{SS} +3.0V to V_{SS} +15V

Lead Temperature

(Soldering, 10 seconds)

260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics tables provide conditions for actual device operation.

Note 2: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

DC Electrical Characteristics

	Parameter	Conditions	Limits									
Symbol			-40°C		+25°C			+85°C			Units	
			Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
IL	Quiescent Device	$V_{DD} = 5.0V$			5.0		0.05	5.0			70	μΑ
	Current	V _{DD} = 10V			10		0.1	10			140	μΑ
P _D	Quiescent Device	$V_{DD} = 5.0V$			25		0.25	25			350	μW
	Dissipation Package	V _{DD} = 10V			100		1.0	100			1,400	μW
V _{OL}	Output Voltage	V _{DD} = 5.0V			0.05		0	0.05			0.05	V
	LOW Level	V _{DD} = 10V			0.05		0	0.05			0.05	V
V _{OH}	Output Voltage	V _{DD} = 5.0V	4.95			4.95	5.0		4.95			V
	HIGH Level	V _{DD} = 10V	9.95			9.95	10		9.95			V
V _{NL}	Noise Immunity	$V_{DD} = 5.0V$	1.5			1.5	2.25		1.4			V
	(All Inputs)	$V_{DD} = 10V$	3.0			3.0	4.5		2.9			V
V _{NH}	Noise Immunity	$V_{DD} = 5.0V$	1.4			1.5	2.25		1.5			V
	(All Inputs)	V _{DD} = 10V	2.9			3.0	4.5		3.0			V
I _D N	Output Drive Current	$V_{DD} = 5.0V$	0.35			0.3	1.2		0.25			mA
	N-Channel (Note 3)	V _{DD} = 10V	0.7			0.6	2.4		0.5			mA
I _D P	Output Drive Current	$V_{DD} = 5.0V$	-0.21			-0.15	-0.6		-0.12			mA
	P-Channel (Note 3)	V _{DD} = 10 V	-0.45			-0.32	-1.3		-0.25			mA
I	Input Current	$V_I = 0V \text{ or } V_I = V_{DD}$					10					pA

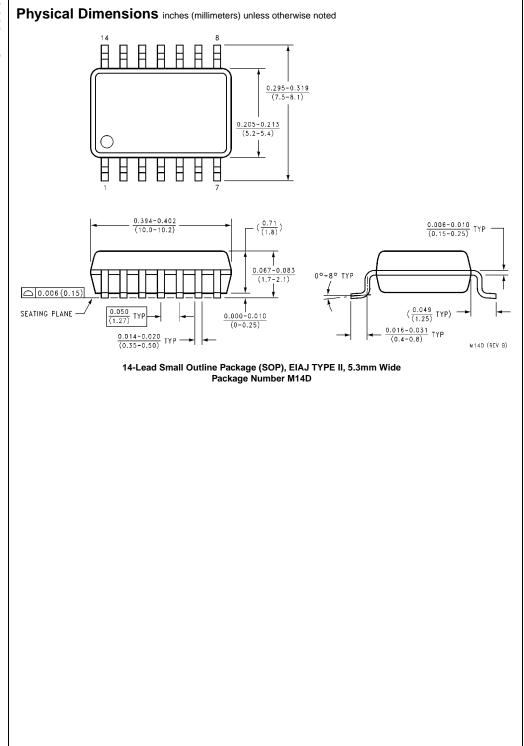
Note 3: I_DN and I_DP are tested one output at a time.

AC Electrical Characteristics (Note 4)

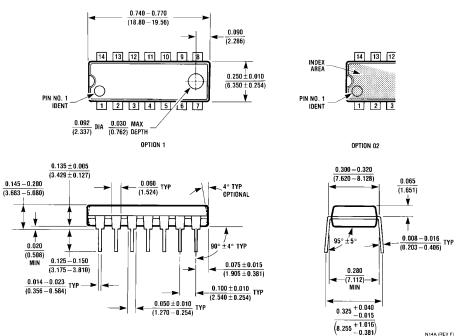
Symbol	Parameter	Conditions		Limits			
		Conditions	Min	Тур	Max	Units	
t _{PHL}	Propagation Delay Time	V _{DD} = 5.0V		100	300	ns	
		V _{DD} = 10V		40	150	ns	
t _{PLH}	Propagation Delay Time	V _{DD} = 5.0V		100	300	ns	
		V _{DD} = 10V		40	150	ns	
t _{THL}	Transition Time	V _{DD} = 5.0V		70	300	ns	
	HIGH-to-LOW Level	$V_{DD} = 10V$		25	150	ns	
t _{TLH}	Transition Time	V _{DD} = 5.0V		80	300	ns	
	LOW-to-HIGH Level	V _{DD} = 10V		30	150	ns	
C _I	Input Capacitance	$V_I = 0V \text{ or } V_I = V_{DD}$		5.0		pF	

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Note 4: AC Parameters are guaranteed by DC correlated testing.



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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