

CD4043BC • CD4044BC

Quad 3-STATE NOR R/S Latches • Quad 3-STATE NAND R/S Latches

General Description

The CD4043BC are quad cross-couple 3-STATE CMOS NOR latches, and the CD4044BC are quad cross-couple 3-STATE CMOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. There is a common 3-STATE ENABLE input for all four latches. A logic "1" on the ENABLE input connects the latch states to the Q outputs. A logic "0" on the ENABLE input disconnects the latch states from the Q outputs resulting in an open circuit condition on the Q output. The 3-STATE feature allows common bussing of the outputs.

Features

- Wide supply voltage range: 3V to 15V
- Low power: 100 nW (typ.)
- High noise immunity: $0.45 V_{DD}$ (typ.)
- Separate SET and RESET inputs for each latch
- NOR and NAND configuration
- 3-STATE output with common output enable

Applications

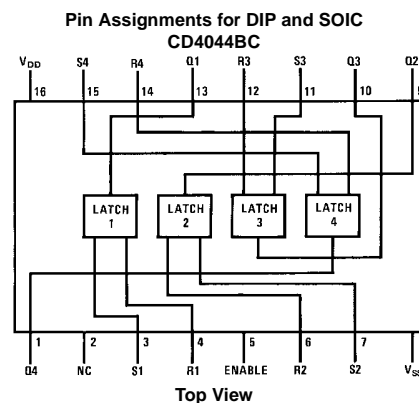
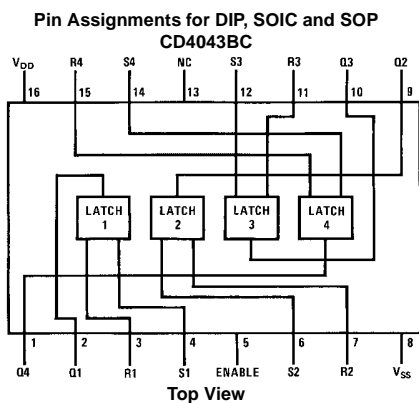
- Multiple bus storage
- Strobed register
- Four bits of independent storage with output enable
- General digital logic

Ordering Code:

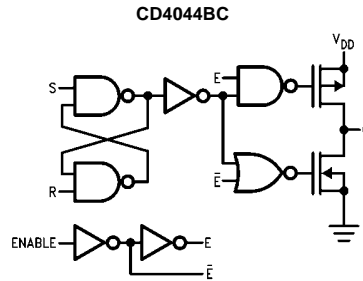
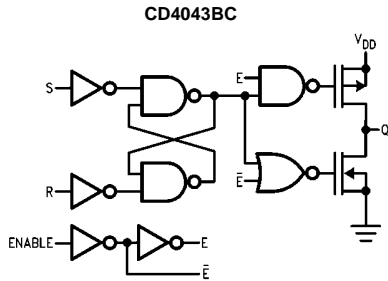
Order Number	Package Number	Package Description
CD4043BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD4043BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4044BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD4044BCSJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4044BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams



Block Diagrams



Truth Tables

CD4043BC

S	R	E	Q
X	X	0	OC
0	0	1	NC
1	0	1	1
0	1	1	0
1	1	1	Δ

CD4044BC

S	R	E	Q
X	X	0	OC
1	1	1	NC
0	1	1	1
1	0	1	0
0	0	1	$\Delta\Delta$

OC = 3-STATE
 NC = No change
 X = Don't care
 Δ = Dominated by S = 1 input
 $\Delta\Delta$ = Dominated by R = 0 input

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions	
(Note 2)		(Note 2)	
Supply Voltage (V_{DD})	-0.5V to +18V	Supply Voltage (V_{DD})	3.0V to 15V
Input Voltage (V_{IN})	-0.5V to V_{DD} +0.5V	Input Voltage (V_{IN})	0 to V_{DD} V
Storage Temperature Range (T_S)	-65°C to +150°C	Operating Temperature Range (T_A)	-40°C to +85°C
Power Dissipation (P_D)		CD4043BC, CD4044BC	-40°C to +85°C
Dual-In-Line	700 mW	Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation. Note 2: $V_{SS} = 0V$ unless otherwise specified.	
Small Outline	500 mW		
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C		

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		20		0.01	20		150	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		40		0.01	40		300	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		80		0.02	80		600	μA
V_{OL}	LOW Level Output Voltage	$ I_O \leq 1 \mu A, V_{IL} = 0V, V_{IH} = V_{DD}$		0.05		0	0.05		0.05	V
		$V_{DD} = 5.0V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	$ I_O \leq 1 \mu A, V_{IL} = 0V, V_{IH} = V_{DD}$								V
		$V_{DD} = 5.0V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
V_{IL}	LOW Level Input Voltage	$ I_O \leq 1 \mu A$								V
		$V_{DD} = 5.0V, V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0		4.5	3.0		3.0	V
V_{IH}	HIGH Level Input Voltage	$ I_O \leq 1 \mu A$								V
		$V_{DD} = 5.0V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 5.0V, V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
I_{OL}	LOW Level Output Current (Note 3)	$V_{IL} = 0V, V_{IH} = V_{DD}$								mA
		$V_{DD} = 5.0V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.2		0.9		mA
I_{OH}	HIGH Level Output Current (Note 3)	$V_{IL} = 0V, V_{IH} = V_{DD}$								mA
		$V_{DD} = 5.0V, V_O = 4.6V$	-0.52		-0.44	-0.32		-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.3		-1.1	-0.8		-0.9		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$	-0.3			-0.3			-1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$	0.3			0.3			1.0	μA

Note 3: I_{OH} and I_{OL} are tested one output at a time.

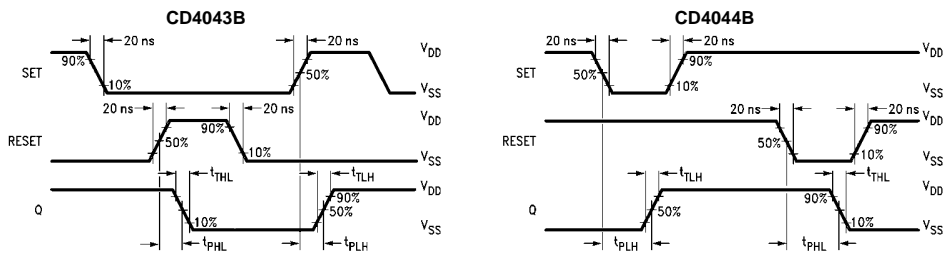
AC Electrical Characteristics (Note 4)

$T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}$, input $t_r = t_f = 20\text{ ns}$, unless otherwise noted

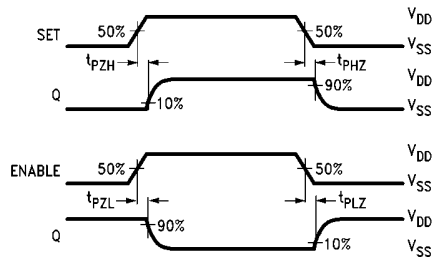
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH} , t_{PHL}	Propagation Delay S or R to Q	$V_{DD} = 5.0\text{V}$		175	350	ns
		$V_{DD} = 10\text{V}$		75	175	ns
		$V_{DD} = 15\text{V}$		60	120	ns
t_{PZH} , t_{PHZ}	Propagation Delay Enable to Q (HIGH)	$V_{DD} = 5.0\text{V}$		115	230	ns
		$V_{DD} = 10\text{V}$		55	110	ns
		$V_{DD} = 15\text{V}$		40	80	ns
t_{PZL} , t_{PLZ}	Propagation Delay Enable to Q (LOW)	$V_{DD} = 5.0\text{V}$		100	200	ns
		$V_{DD} = 10\text{V}$		50	100	ns
		$V_{DD} = 15\text{V}$		40	80	ns
t_{THL} , t_{TLH}	Transition Time	$V_{DD} = 5.0\text{V}$		100	200	ns
		$V_{DD} = 10\text{V}$		50	100	ns
		$V_{DD} = 15\text{V}$		40	80	ns
t_{WO}	Minimum SET or RESET Pulse Width	$V_{DD} = 5.0\text{V}$		80	160	ns
		$V_{DD} = 10\text{V}$		40	80	ns
		$V_{DD} = 15\text{V}$		20	40	ns
C_{IN}	Input Capacitance			5.0	7.5	pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

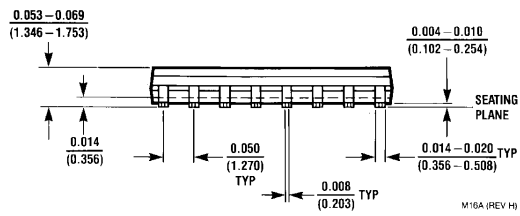
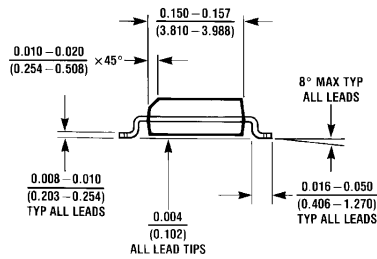
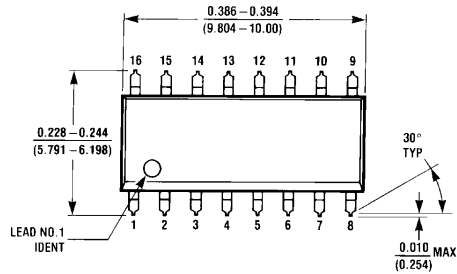
Timing Waveforms



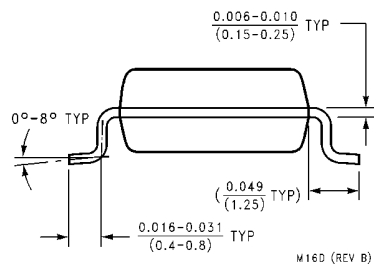
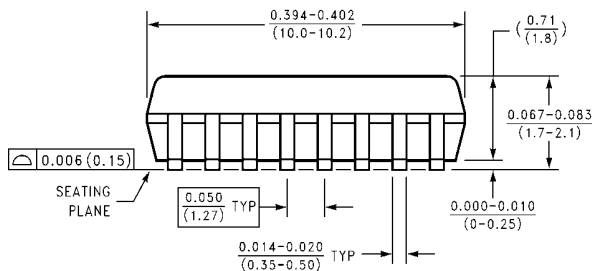
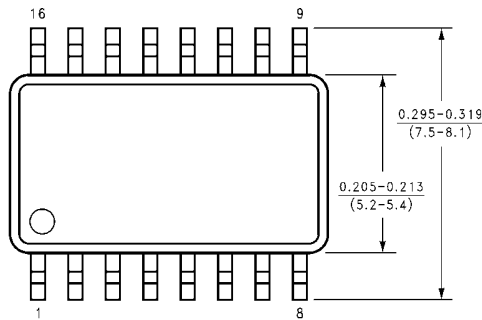
Enable Timing



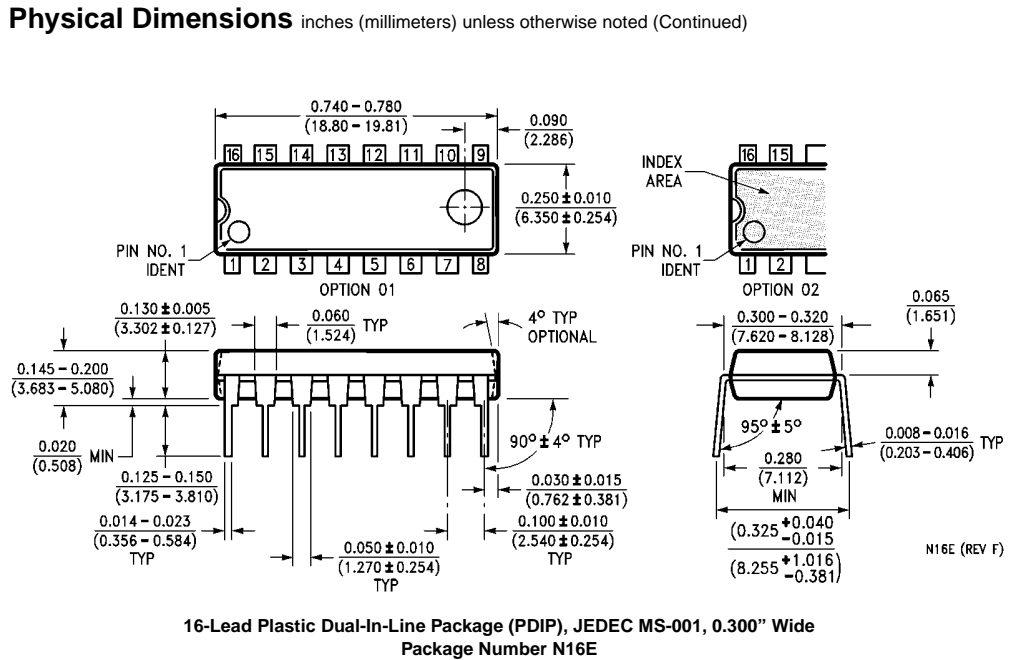
Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
Package Number M16A**



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**



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