FAIRCHILD SEMICONDUCTOR™

April 1984
Revised February 2000

DM74ALS273
Octal D-Type Edge-Triggered Flip-Flop with Clear

General Description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or LOW level, the D input signal has no effect at the output.

Features

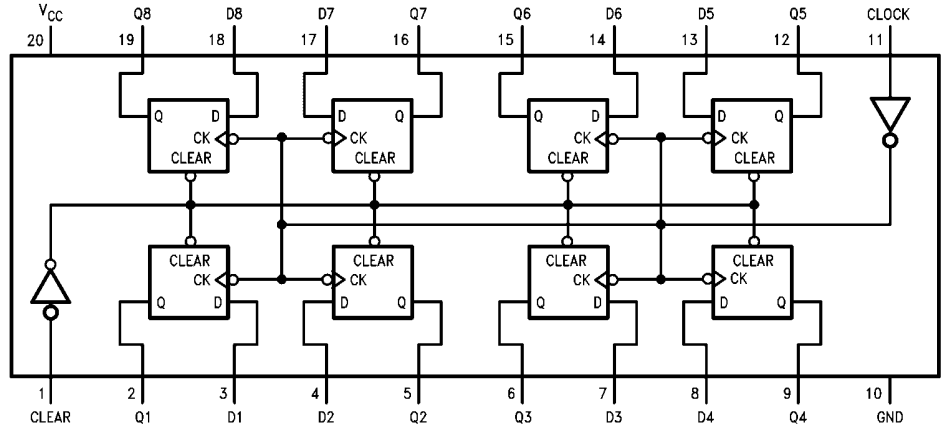
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Buffer-type outputs and improved AC offer significant advantage over DM74LS273.
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with DM74LS273.

Ordering Code:

Order Number	Package Number	Package Description
DM74ALS273WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74ALS273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74ALS273MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
DM74ALS273N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



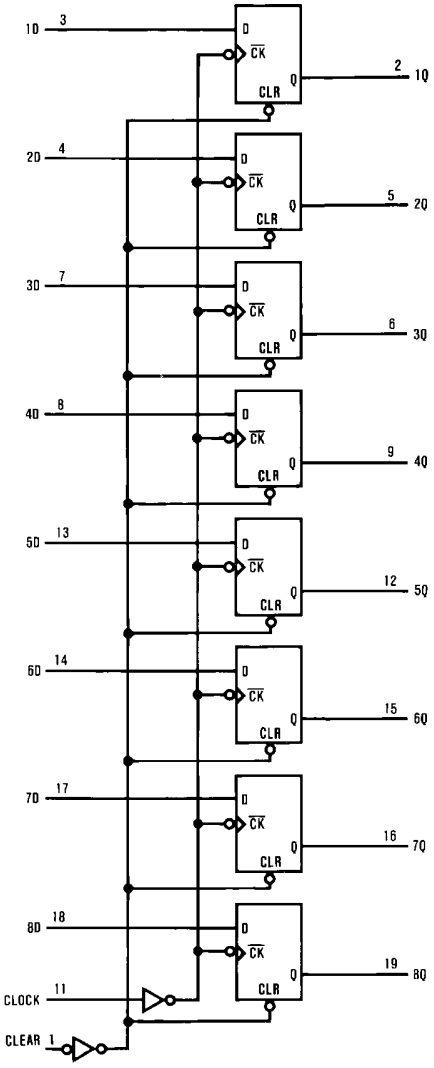
Function Table

(Each Flip-Flop)

Inputs			Output
Clear	**Clock**	**D**	**Q**
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

L = LOW State
H = HIGH State
X = Don't Care
↑ = Positive Edge Transition
Q_0 = Previous Condition of Q

Logic Diagram



Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	60.0°C/W
M Package	79.0°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−2.6	mA
I_{OL}	LOW Level Output Current				24	mA
f_{CLK}	Clock Frequency		0		35	MHz
$t_{W(CLK)}$	Width of Clock Pulse	HIGH	14			ns
		LOW	14			ns
t_W	Width of Clear Pulse	LOW	10			ns
t_{SU}	Data Setup Time (Note 2)		10↑			ns
		Clear Inactive	15↑			
t_H	Data Hold Time		0↑			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 2: The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

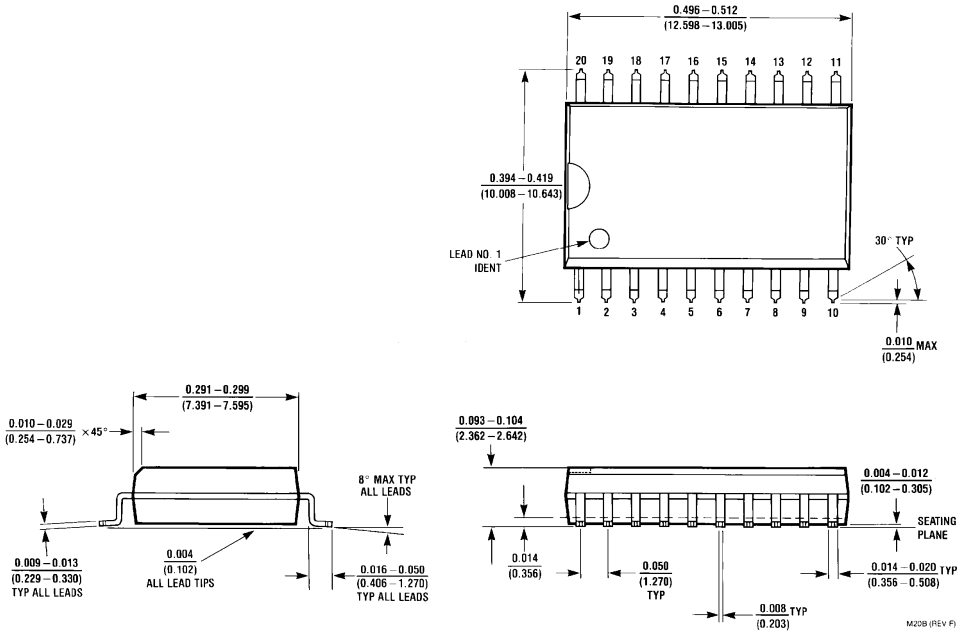
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	HIGH Level	V_{CC} = 4.5V	I_{OH} = −2.6 mA	2.4	3.3		V
	Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −400 µA	V_{CC} − 2			V
V_{OL}	LOW Level	V_{CC} = 4.5V	I_{OL} = 12 mA		0.25	0.4	V
	Output Voltage		I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Maximum Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	µA
I_{IL}	LOW Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs HIGH		11	20	mA
		Outputs OPEN	Outputs LOW		19	29	mA

Switching Characteristics

over recommended operating free air temperature range.

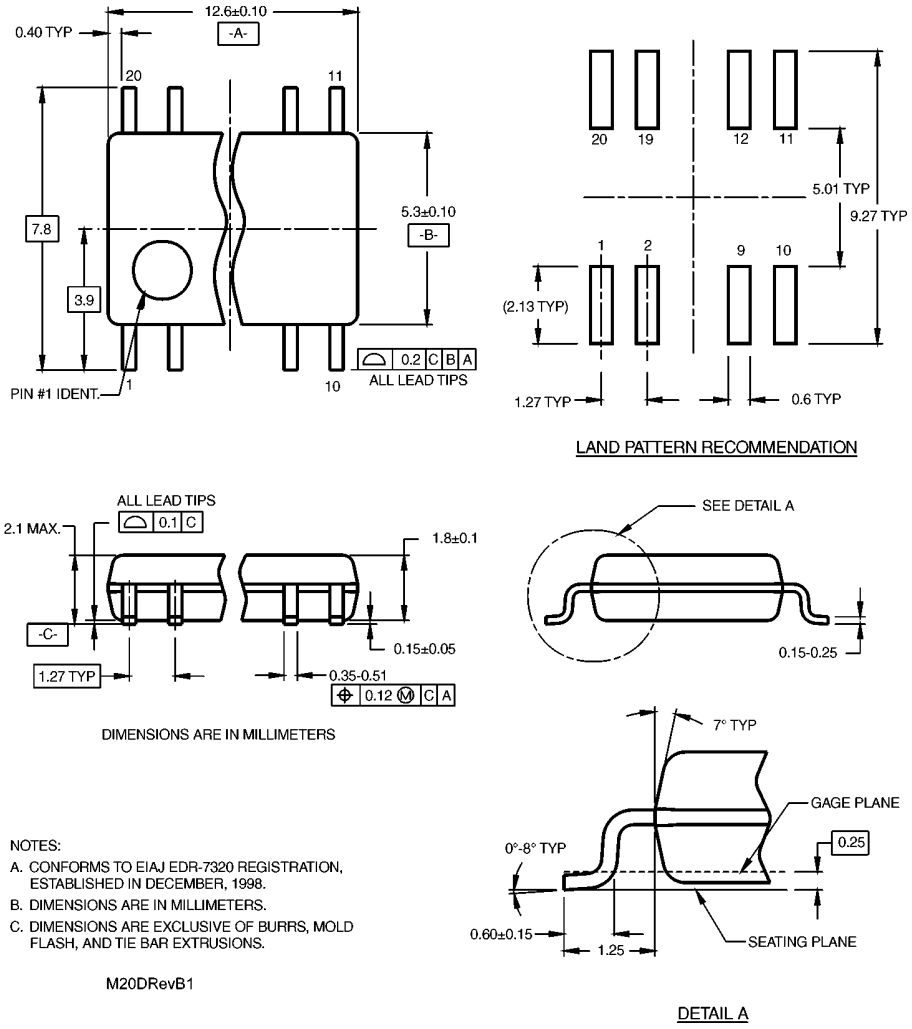
Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V			35		MHz
t_{PHL}	Propagation Delay Time	R_L = 500Ω	Clear	Any Q	4	18	ns
	HIGH-to-LOW Level Output	C_L = 50 pF					
t_{PLH}	Propagation Delay Time		Clock	Any Q	2	12	ns
	LOW-to-HIGH Level Output						
t_{PHL}	Propagation Delay Time		Clock	Any Q	3	15	ns
	HIGH-to-LOW Level Output						

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

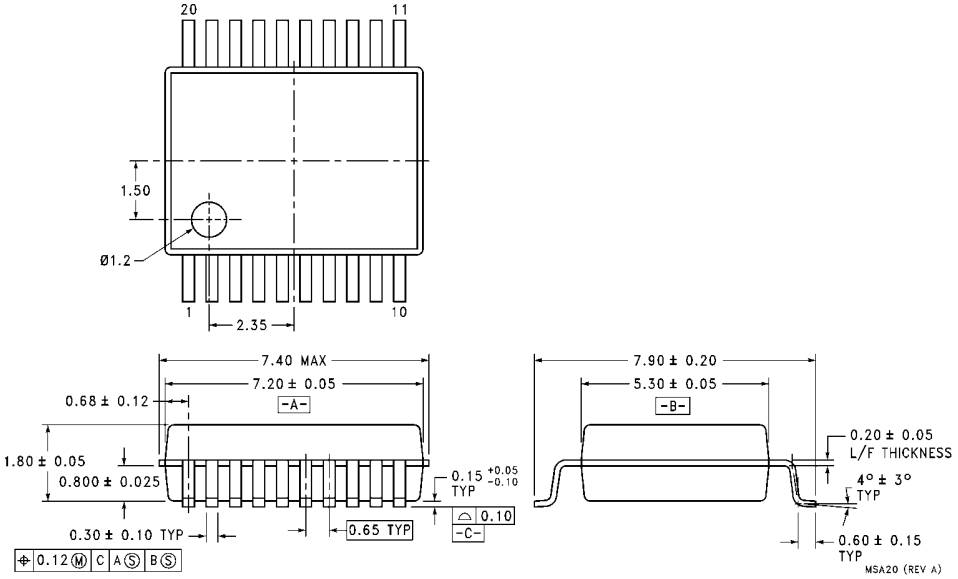
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

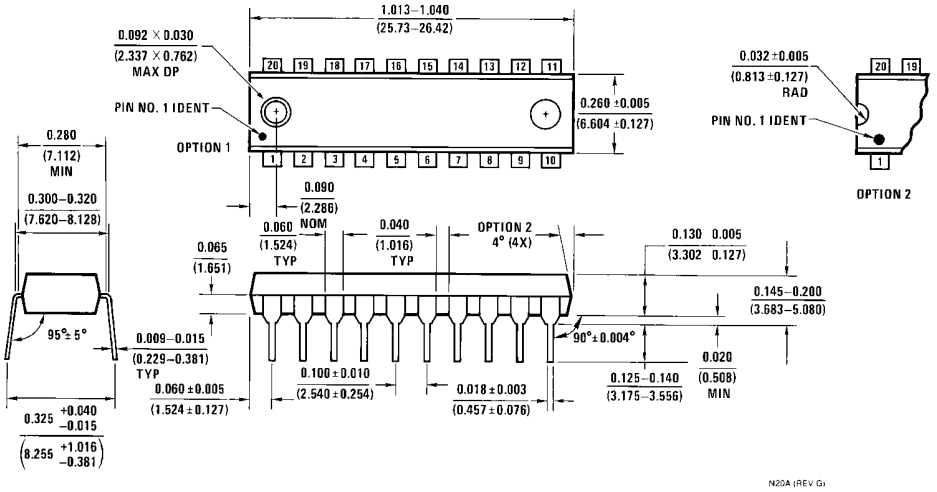
20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A