FAIRCHILD

SEMICONDUCTOR

DM74ALS520 • DM74ALS521 8-Bit Comparator

General Description

These comparators perform an "equal to" comparison of two 8-bit words with provision for expansion or external enabling. The matching of the two 8-bit input plus a logic LOW on the $\overline{\text{EN}}$ input produces the output $\overline{A}=\overline{B}$ on the DM74ALS520 and DM74ALS521. The DM74ALS520 and DM74ALS521 have totem pole outputs for wire AND cascading. Additionally, the DM74ALS520 is provided with B input pull up termination resistors for analog or switch data.

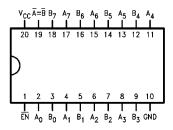
September 1986 Revised April 2000

DM74ALS520 • DM74ALS521 8-Bit Comparator

Ordering Code:

Ordering Code	Package Number	Package Description
DM74ALS520WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74ALS520N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74ALS521WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
SM74ALS521N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Devices also available	in Tape and Reel. Specify	by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Features

process

counterpart

Switching specifications at 50 pF

ture and $V_{\mbox{CC}}$ range

Switching specifications guaranteed over full tempera-

Advanced oxide-isolated, ion-implanted Schottky TTL

■ Functionally and pin for pin compatible with LS family

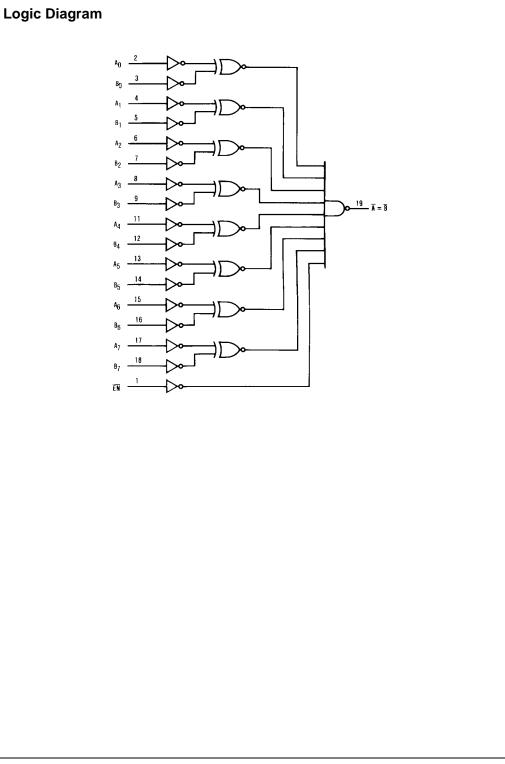
Improved output transient handling capability

Inp	Inputs	
EN	Data	$\overline{\mathbf{A}} = \overline{\mathbf{B}}$
L	A = B	L
L	A ≠ B	н
н	х	н

H = HIGH Logic Level L = LOW Logic Level X = Don't Care

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Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Typical θ _{JA}	
N Package	62.0°C/W
M Package	82.0°C/W
-	

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation. DM74ALS520 • DM74ALS521

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	
′cc	Supply Voltage	4.5	5	5.5	V	
ін	HIGH Level Input Voltage	2			V	
IL	LOW Level Input Voltage			0.8	V	
ЭН	HIGH Level Output Current			-2.6	mA	
DL	LOW Level Output Current			24	mA	
A	Free Air Operating Temperature	0		70	°C	

Electrical Characteristics

	nperature range. All typical values are measured at V	$_{\rm CC}$ = 5V, $T_{\rm A}$	= 25°C.

Symbol	Parameter	Conditi	ons	Min	Тур	Max	Units
V _{IK}	Input Clamp Voltage	$V_{CC} = 4.5V, I_I = -18 \text{ mA}$				-1.5	V
V _{OH}	HIGH Level Output Voltage	$V_{CC} = 4.5V$ to 5.5V $I_{OH} = -400 \ \mu A$		$V_{CC}-2$			V
		V _{CC} = 4.5V I _{OH} = Max		2.4	3.2		V
V _{OL}	LOW Level Output Voltage	$V_{CC} = 4.5V$	I _{OL} = 24 mA		0.35	0.5	V
I _I	Max HIGH Input Current	$V_{CC} = 5.5V$	$V_{IH} = 5.5V$ B Input DM74ALS520 $V_{IH} = 7V$, All Others			0.1	mA
IIH	HIGH Level Input Current	V _{CC} = 5.5V, V _{IH} = 2.7V	All Others B Input DM74ALS520			20 200	μΑ
IL	Low Level Input	$V_{CC} = 5.5V,$	B Input DM74ALS520			-0.6	mA
	Current	$V_{IL} = 0.4V$	All Others			-0.1	mA
I _O	Output Drive Current	$V_{CC} = 5.5V$	V _O = 2.25V	-30		-112	mA
I _{CC}	Supply Current	V _{CC} = 5.5V (Note 2)			12	19	mA

Note 2: I_{CC} is measured with EN grounded, A and B inputs at 4.5V and outputs OPEN.

Switching Characteristics

Symbol	Parameter	Conditions	From Input	To Output	Min	Max	Units
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$V_{CC} = 4.5V$ to 5.5V $C_L = 50 \text{ pF}$	A or B Data	$\overline{A} = \overline{B}$	3	12	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	$R_L = 500\Omega$	A or B Data	$\overline{A} = \overline{B}$	5	20	ns
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		EN	$\overline{A} = \overline{B}$	2	12	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		EN	$\overline{A} = \overline{B}$	5	22	ns

