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DM74LS181 4-Bit Arithmetic Logic Unit

General Description

The DM74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations.

October 1988 Revised April 2000

Provides 16 arithmetic operations: add, subtract, com-

■ Full lookahead for high speed arithmetic operation on

pare, double, plus twelve other arithmetic operations

Provides all 16 logic operations of two variables: exclusive-OR, compare, AND, NAND, OR, NOR, plus

DM74LS181 4-Bit Arithmetic Logic Unit

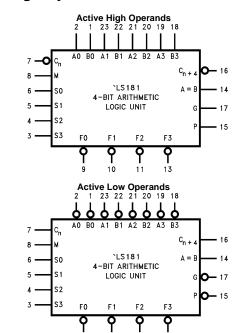
Ordering Code:

Order Number	Package Number	Package Description
DM74LS181N	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600 Wide

Features

long words

Logic Symbols



Connection Diagram

ten other logic operations

<u></u> во —		24	L
Ā0 —	2	24	−V _{CC} −Ā1
S3 —	3	23	— B1
s2 —	4	21	— Ā2
s1—	5	20	— Ē2
so —	6	19	— Ā3
c _n —	7	18	— <u>B</u> 3
м —	8	17	— Ē
Ē0 —	9	16	— C _{n+4}
Ē1—	10	15	− P
Ē2 —	11	14	— A=B
GND -	12	13	— F3

Pin Descriptions

Pin Names	Description
A0-A3	Operand Inputs (Active LOW)
B0-B3	Operand Inputs (Active LOW)
S0-S3	Function Select Inputs
М	Mode Control Input
C _n	Carry Input
F0-F3	Function Outputs (Active LOW)
A = B	Comparator Output
G	Carry Generate Output (Active LOW)
P	Carry Propagate Output (Active LOW)
C _{n+4}	Carry Output

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V_{CC} = Pin 24 GND = Pin 12 11

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Functional Description

The DM74LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (SO–S3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the $\ensuremath{C_{n\!+\!4}}$ output, or for carry lookahead between packages using the signals \overline{P} (Carry Propagate) and \overline{G} (Carry Generate). In the ADD mode, \overline{P} indicates that \overline{F} is 15 or more, while \overline{G} indicates that \overline{F} is 16 or more. In the SUBTRACT mode, \overline{P} indicates that \overline{F} is zero or less, while \overline{G} indicates that \overline{F} is less than zero. \overline{P} and \overline{G} are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output $(C_{n\!+\!4})$ signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of four DM74LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four \overline{F} outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

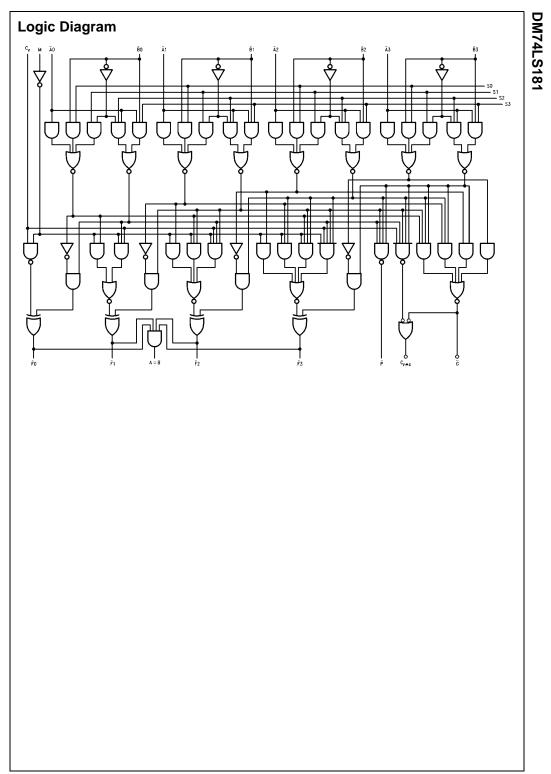
The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

Function Table

	Mode	Select		Acti	ve LOW Operands	Acti	ve HIGH Operands
	Inp	uts			& F _n Outputs		& F _n Outputs
				Logic	Arithmetic (Note 2)	Logic	Arithmetic (Note 2)
S3	S2	S1	S0	(M = H)	$(\mathbf{M}=\mathbf{L})~(\mathbf{C}_{\mathbf{n}}=\mathbf{L})$	(M = H)	$(\mathbf{M}=\mathbf{L})~(\mathbf{C_n}=\mathbf{H})$
L	L	L	L	Ā	A minus 1	Ā	A
L	L	L	н	AB	AB minus 1	$\overline{A} + \overline{B}$	A + B
L	L	н	L	$\overline{A} + \overline{B}$	AB minus 1	Ā B	$A + \overline{B}$
L	L	н	Н	Logic 1	minus 1	Logic 0	minus 1
L	Н	L	L	$\overline{A} + \overline{B}$	A plus (A + B)	AB	A plus AB
L	н	L	Н	В	AB plus (A + B)	В	(A + B) plus AB
L	н	н	L	$\overline{A} \oplus \overline{B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	н	н	н	$A + \overline{B}$	$A + \overline{B}$	AB	AB minus 1
н	L	L	L	Ā B	A plus (A + B)	$\overline{A} + B$	A plus AB
н	L	L	н	A ⊕ B	A plus B	$\overline{A} \oplus \overline{B}$	A plus B
н	L	н	L	В	AB plus (A + B)	В	(A + B) plus AB
н	L	н	Н	A + B	A + B	AB	AB minus 1
н	н	L	L	Logic 0	A plus A (Note 1)	Logic 1	A plus A (Note 1)
н	н	L	н	AB	AB plus A	$A + \overline{B}$	(A + B) plus A
н	н	н	L	AB	AB minus A	A + B	(A + B) plus A
н	н	н	н	A	A	A	A minus 1

Note 1: Each bit is shifted to the next most significant position. Note 2: Arithmetic operations expressed in 2s complement notation.

Note 2. Antimetic operations expressed in 2s complement notati



DM74LS181

Absolute Maximum Ratings(Note 3)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{ОН}	HIGH Level Output Current			-0.4	mA
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

Symbol	Parameter	Conditions	i	Min	Typ (Note 4)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$				-1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max		2.7			V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IH} = Min			0.35	0.5	v
		$I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$			0.25	0.4	ĺ
I	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 7V$	M input Ā _n , Ē _n S _n C _n			0.1 0.3 0.4 0.5	mA
IIH	HIGH Level Input Current	$V_{CC} = Max, V_I = 2.7V$	M input Ā _n , Ē _n S _n C _n			20 60 80 100	μΑ
l _{IL}	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V$	M input Ā _n , Ē _n S _n C _n			-0.4 -1.2 -1.6 -2.0	mA
os	Short Circuit Output Current	V _{CC} = Max (Note 5)		-20		-100	mA
сс	Supply Current	$V_{CC} = Max, \overline{B}_n, C_n = GND$ $S_n, M, \overline{A}_n = 4.5V$				37	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

• • •	$T_A = 25^{\circ}C$.		C _L =	15 pF		
Symbol	Parameter		Conditions		Min Max		Units	
LH	Propagation Delay	M = GI	ND			27	ns	
νHL	C _n to C _{n+4}					20	115	
LH	Propagation Delay	M = GN	ND			26	ns	
ΉL	C _n to F					20	110	
'LH	Propagation Delay		$S_2 = GND;$			29	ns	
ΉL	\overline{A} or \overline{B} to \overline{G} (Sum)	S ₁ , S ₃	= 4.5V			23		
LH	Propagation Delay		S ₃ = GND;			32	ns	
HL	A or B to G (Diff)	S ₁ , S ₂				26	-	
LH	Propagation Delay		$S_2 = GND;$			30	ns	
HL	A or B to P (Sum)	S ₀ , S ₃				30		
LH	Propagation Delay		S ₃ = GND;			30	ns	
ΉL	A or B to P (Diff)	S ₁ , S ₂	= 4.5V			33		
LH	Propagation Delay		$S_2 = GND;$			32	ns	
HL	\overline{A}_i or \overline{B}_i to \overline{F}_i (Sum)	S ₀ , S ₃	= 4.5V			25		
'LH	Propagation Delay	-	S ₃ = GND;			32	ns	
ΉL	A _i or B _i to F _i (Diff)	S ₁ , S ₂				33		
чLН	Propagation Delay	M = 4.5	ov.			33	ns	
ΉL	A or B to F (Logic)		0.000			29		
чLН	Propagation Delay		$S_2 = GND;$			38	ns	
ΉL	\overline{A} or \overline{B} to C_{n+4} (Sum) Propagation Delay	S ₀ , S ₃	= 4.5V S ₃ = GND;			38 41		
чLН							ns	
νHL	A or B to C _{n+4} (Diff)		$S_1, S_2 = 4.5V$ M, $S_0, S_3 = GND;$			41 50		
PLH	Propagation Delay \overline{A} or \overline{B} to $A = B$		33 - GND,			30	ns	
			4 5)/:			60	ns	
	Mode Test Tabl	$R_L = 2$	= 4.5V; kΩ to 5.0V ction Inpu	ts		62	ns	
Sum ^{S0 = S3 =}	Mode Test Tabl 4.5V, S1 = S2 = M = 0V Input	e 1 Fun	kΩ to 5.0V		Data Inpu		Output Under	
Sum	Mode Test Tabl 4.5V, S1 = S2 = M = 0V Input	e 1 Fun	kΩ to 5.0V Ction Inpur				Output	
Sum 50 = 53 =	Mode Test Tabl 4.5V, S1 = S2 = M = 0V Input Junder	e 1 Fun Othe	kû to 5.0V Ction Inpur r Input ne Bit	Other		ts	Output Under	
Sum 50 = 53 = Symt	Mode Test Tabl 4.5V, S1 = S2 = M = 0V Input Junder	R _L =2 e 1 Fun Othe Sam	kΩ to 5.0V ction Inpur r Input ne Bit Apply	Other		ts Apply	Output Under	
Sum <u>S0 = S3 =</u> Symt	Mode Test Tabl	R _L =2 e 1 Fun Othe Sam Apply 4.5V	kΩ to 5.0V ction Input r Input te Bit Apply GND	Other Apply 4.5V		ts Apply GND	Output Under Test	
Sum <u>S0 = S3 =</u> Symt	Mode Test Tabl	R _L =2 e 1 Fun Othe Sam Apply 4.5V	kΩ to 5.0V ction Input r Input te Bit Apply GND	Other Apply 4.5V Remaining		ts Apply GND	Output Under Test	
Sum <u>S0 = S3 =</u> Symt PLH PHL PLH	Mode Test Tabl 4.5V, S1 = S2 = M = 0V Input bol Under Test Ā _i	R _L = 2 e 1 Fun Othe Sam Apply 4.5V B _i	kΩ to 5.0V ction Input r Input te Bit Apply GND None	Apply 4.5V Remaining Ā and B		ts Apply GND C _n	Output Under Test F _i	
Sum S0 = S3 = Symt PLH PHL PLH PHL	Mode Test Tabl 4.5V, S1 = S2 = M = 0V Input bol Under Test Ā _i	R _L = 2 e 1 Fun Othe Sam Apply 4.5V B _i	kΩ to 5.0V ction Input r Input te Bit Apply GND None	Other Apply 4.5V Remaining Ā and B Remaining		ts Apply GND C _n	Output Under Test F _i	
S0 = S3 =	Mode Test Tabl 4.5V, S1 = S2 = M = 0V Input bol Under Test Ā _i B _i	RL = 2 e 1 Fun Othe San Apply 4.5V Bi Apply	kΩ to 5.0V ction Input r Input Bit Apply GND None None	Other Apply 4.5V Remaining Ā and Ē Remaining Ā and Ē	Re	Apply GND C _n C _n	Output Under Test \overline{F}_i \overline{F}_i	
Sum S0 = S3 = Symt PLH PHL PHL PHL PHL	Mode Test Tabl 4.5V, S1 = S2 = M = 0V Input bol Under Test Ā _i B _i	RL = 2 e 1 Fun Othe San Apply 4.5V Bi Apply	kΩ to 5.0V ction Input r Input Bit Apply GND None None	Other Apply 4.5V Remaining Ā and Ē Remaining Ā and Ē	Re	ts Apply GND C _n C _n maining	Output Under Test \overline{F}_i \overline{F}_i	
Sum S0 = S3 = Symt PLH PHL PHL PHL PHL PLH	Mode Test Tabl 4.5V, S1 = S2 = M = 0V Input bol Under Test Ā _i B _i Ā	RL = 2 e 1 Fun Othe San Apply 4.5V Bi Ai B -	kΩ to 5.0V Ction Input Bit Apply GND None None None	Other Apply 4.5V Remaining Ā and B Remaining Ā and B None	Re Ā a	ts Apply GND C _n C _n maining and B, C _n	Output Under Test \overline{F}_i \overline{F}_i \overline{P}	
Sum S0 = S3 = Symt PLH PHL PHL PHL PHL PHL PHL	Mode Test Tabl 4.5V, S1 = S2 = M = 0V Input bol Under Test Ā _i B _i Ā	RL = 2 e 1 Fun Othe San Apply 4.5V Bi Ai B -	kΩ to 5.0V Ction Input Bit Apply GND None None None	Other Apply 4.5V Remaining Ā and B Remaining Ā and B None	Re Āa Rē Āa	ts Apply GND C _n C _n maining and B, C _n maining	Output Under Test \overline{F}_i \overline{F}_i \overline{P}	
Sum S0 = S3 = Symt จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห	Mode Test Tabl 4.5V, S1 = S2 = M = 0V Input bol Under Test Ā _i B _i B	RL = 2 e 1 Fun Othe San Apply 4.5V Bi Ai Appl Ai Appl Ai Appl Ai Ai Ai	kΩ to 5.0V	Other Apply 4.5V Remaining Ā and B Remaining Ā and B None None	Re Āa Re Āa	ts Apply GND C _n maining Ind B, C _n maining Ind B, C _n maining Ind B, C _n	Output Under Test \overline{F}_i \overline{P}	
Sum 50 = S3 = Symt 2LH 2LH 2LH 2LH 2LH 2LH 2LH 2LH	Mode Test Tabl 4.5V, S1 = S2 = M = 0V Input bol Under Test Ā _i B _i B	RL = 2 e 1 Fun Othe San Apply 4.5V Bi Ai Appl Ai Appl Ai Appl Ai Ai Ai	KΩ to 5.0V Ction Input Te Bit Apply GND None None None None B	Other Apply 4.5V Remaining Ā and B Remaining Ā and B None None Remaining B	Re Āa Re Āa	ts Apply GND Cn Cn Cn maining und B, Cn maining und B, Cn	Output Under Test \overline{F}_i \overline{P}	
Sum S0 = S3 = Symt จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห	Ande Test Table 4.5V, S1 = S2 = M = 0V Input bol Under Test Ā; B; Ā B Ā	RL = 2 e 1 Fun Othe San Apply 4.5V B A A None	kΩ to 5.0V	Other Apply 4.5V Remaining Ā and B Remaining Ā and B None None Remaining	Re Ā a Re Ā a Re Re	ts Apply GND Cn Cn maining Ind B, Cn maining Ind B, Cn maining Ind B, Cn maining Ind B, Cn maining maining T, Cn maining T, Cn maining	Output Under Test \overline{F}_i \overline{P} \overline{P} \overline{G}	
Sum S0 = S3 = Symt PLH PLH PLH PLH PLH PLH PLH PLH	Ande Test Table 4.5V, S1 = S2 = M = 0V Input Under Test Ā; B; Ā B; Ā B; Ā B;	RL = 2 e 1 Fun Othe San Apply 4.5V Bi Ai Apply Apply A.5V Apply A.5V Apply A.5V Apply A.5V Apply A.5V Apply A.5V Apply None None	KΩ to 5.0V Ction Input Te Bit Apply GND None None None None Topot Topo	Other Apply 4.5V Remaining Ā and B Remaining Ā and B None None Remaining B Remaining B Remaining B Remaining B	Re A a Re Re Re	ts Apply GND Cn Cn Cn maining und B, Cn maining maining A, Cn maining A, Cn	Output Under Test \overline{F}_i \overline{P} \overline{Q} \overline{Q}	
Sum S0 = S3 = Symt จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห	Ande Test Table 4.5V, S1 = S2 = M = 0V Input bol Under Test Ā; B; Ā B Ā	RL = 2 e 1 Fun Othe San Apply 4.5V B A A None	KΩ to 5.0V Ction Input Te Bit Apply GND None None None None B	Other Apply 4.5V Remaining Ā and B Remaining Ā and B None None Remaining B Remaining Remaining	Re A a Re A a Re Re Re	ts Apply GND Cn Cn Cn maining und B, Cn maining maining maining T, Cn ma	Output Under Test \overline{F}_i \overline{P} \overline{P} \overline{G}	
Sum 50 = S3 = Symt 2LH 2LH 2LH 2LH 2LH 2LH 2LH 2LH	Mode Test Table 4.5V, S1 = S2 = M = 0V Input bol Under Test Ā ₁ B Ā B Ā B Ā B Ā	RL = 2 e 1 Fun Othe San Apply 4.5V Bi Ai None None None None	KΩ to 5.0V	Other Apply 4.5V Remaining Ā and B Remaining Ā and B None None Remaining B	Re A a Re A a Re Re Re	ts Apply GND Cn Cn Cn maining und B, Cn maining maining A, Cn maining T,	Output Under Test \overline{F}_i \overline{P} \overline{P} \overline{G} \overline{G} \overline{G} \overline{C}_{n+4}	
Sum S0 = S3 = Symt จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห จะเห	Ande Test Table 4.5V, S1 = S2 = M = 0V Input Under Test Ā; B; Ā B; Ā B; Ā B;	RL = 2 e 1 Fun Othe San Apply 4.5V Bi Ai Apply Apply A.5V Apply A.5V Apply A.5V Apply A.5V Apply A.5V Apply A.5V Apply None None	KΩ to 5.0V Ction Input Te Bit Apply GND None None None None Rone Rone Rone Rone Rone Rone Rone R	Other Apply 4.5V Remaining Ā and B Remaining Ā and B None None Remaining B Remaining B	Re A a Re A a Re Re Re Re	ts Apply GND C_n C_n maining and \overline{B}, C_n maining \overline{A}, C_n maining maining \overline{A}, C_n maining maining \overline{A}, C_n maining maining \overline{A}, C_n maining \overline{A}, C_n maining	Output Under Test \overline{F}_i \overline{P} \overline{Q} \overline{Q}	
Sum S0 = S3 = Symt PLH PHL PHL PHL PHL PHL PLH	Ande Test Table 4.5V, S1 = S2 = M = 0V Input Jool Under Test Ā; B; Ā B; Ā B; Ā B; Ā B; Ā	RL = 2 e 1 Fun Othe San Apply 4.5V Bi Ai None None None None	KΩ to 5.0V	Other Apply 4.5V Remaining Ā and B Remaining Ā and B None None Remaining B	Re A a Re A a Re Re Re Re	ts Apply GND Cn Cn Cn maining und B, Cn maining maining A, Cn maining T,	Output Under Test \overline{F}_i \overline{P} \overline{P} \overline{G} \overline{G} \overline{G} \overline{C}_{n+4}	

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`	= S3 = M = 0V Input	Other Input		Other Da	Output Under	
Symbol	Under	Under Same Bit				
	Test	Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	Test
t _{PLH} t _{PHL}	Ā	None	B	Remaining Ā	Remaining B, C _n	Fi
t _{PLH} t _{PHL}	B	Ā	None	Remaining Ā	Remaining B, C _n	F _i
t _{PLH} t _{PHL}	Ā	None	B	None	Remaining \overline{A} and \overline{B} , C_n	P
t _{PLH} t _{PHL}	В	Ā	None	None	Remaining A and B, C _n	P
t _{PLH} t _{PHL}	Ā	B	None	None	Remaining A and B, C _n	G
t _{PLH} t _{PHL}	B	None	Ā	None	Remaining \overline{A} and \overline{B} , C_n	G
t _{PLH} t _{PHL}	Ā	None	B	Remaining Ā	Remaining B, C _n	A = B
t _{PLH} t _{PHL}	B	Ā	None	Remaining Ā	Remaining B, C _n	A = B
t _{PLH} t _{PHL}	Ā	B	None	None	Remaining A and B, C _n	C _{n+4}
t _{PLH} t _{PHL}	B	None	Ā	None	Remaining \overline{A} and \overline{B} , C_n	C _{n+4}

Logic Mode Test Table 3 Fu

Function Inputs

Symbol	Input Under	Other Input Same Bit		Other Da	ata Inputs	Output Under
	Test	Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	Test
t _{PLH} t _{PHL}	Ā	B	None	None	Remaining \overline{A} and \overline{B} , C_n	Any F
t _{PLH} t _{PHL}	B	Ā	None	None	Remaining \overline{A} and \overline{B} , C _n	Any F

