FAIRCHILD SEMICONDUCTOR™

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DM74LS299
8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

General Description

The DM74LS299 is an 8-bit universal shift/storage register with 3-STATE outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q0 and Q7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

Features

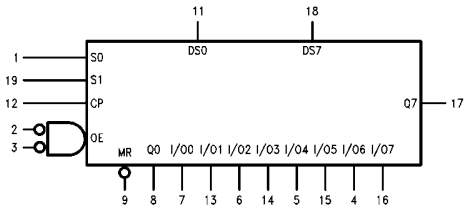
- Common I/O for reduced pin count
- Four operation modes: shift left, shift right, load and store
- Separate shift right serial input and shift left serial input for easy cascading
- 3-STATE outputs for bus oriented applications

Ordering Code:

Order Number	Package Number	Package Description
DM74LS299WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS299N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

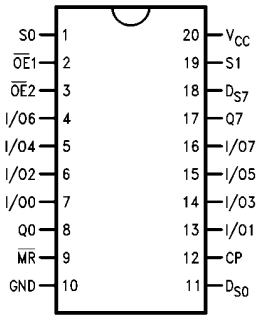
Logic Symbol



V_{CC} = Pin 20

GND = Pin 10

Connection Diagram



Pin Descriptions

Pin Names	Description
CP	Clock Pulse Input (Active Rising Edge)
D_{S0}	Serial Data Input for Right Shift
D_{S7}	Serial Data Input for Left Shift
S0, S1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}1$, $\overline{OE}2$	3-STATE Output Enable Inputs (Active LOW)
I/O0–I/O7	Parallel Data Inputs or 3-STATE Parallel Outputs
Q0–Q7	Serial Outputs

Functional Description

The DM74LS299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by the S0 and S1, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q0 and Q7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

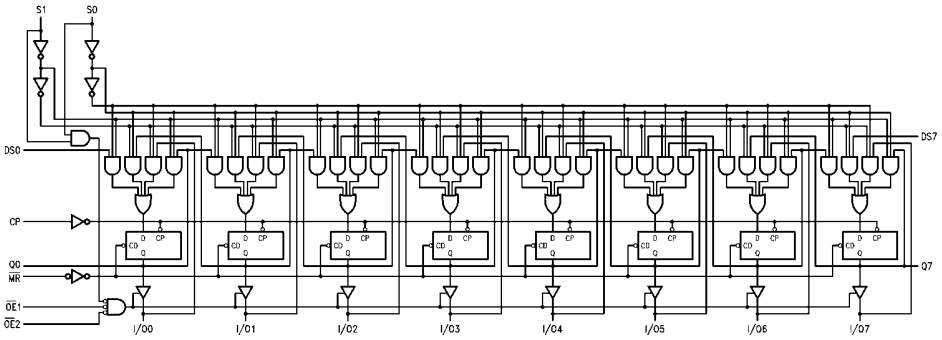
A HIGH signal on either $\overline{OE}1$ or $\overline{OE}2$ disables the 3-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-STATE buffers are also disabled by HIGH signals on both S0 and S1 in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
$\overline{MR}$	S1	S0	CP	
L	X	X	X	Asynchronous Reset; Q0–Q7 = LOW
H	H	H	↗	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↗	Shift Right; $D_{S0} \rightarrow Q0$, $Q0 \rightarrow Q1$, etc.
H	H	L	↗	Shift Left; $D_{S7} \rightarrow Q7$, $Q7 \rightarrow Q6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Clock (CP) Transition

Logic Diagram



Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current	Q0, Q7			−0.4	mA
		I/O0–I/O7			−2.6	mA
I_{OL}	LOW Level Output Current	Q0, Q7			8	mA
		I/O0–I/O7			24	mA
T_A	Free Air Operating Temperature		0		70	°C
$t_S(H)$	Setup Time HIGH or LOW		24			ns
$t_S(L)$	S0 or S1 to CP		24			
$t_H(H)$	Hold Time HIGH or LOW		0			ns
$t_H(L)$	S0 or S1 to CP		0			
$t_S(H)$	Setup Time HIGH or LOW		10			ns
$t_S(L)$	I/O_n, D_{S0}, D_{S7} to CP		10			
$t_H(H)$	Hold Time HIGH or LOW		0			ns
$t_H(L)$	I/O_n, D_{S0}, D_{S7} to CP		0			
$t_W(H)$	CP Pulse Width HIGH or LOW		15			ns
$t_W(L)$			15			
$t_W(L)$	$\overline{MR}$ Pulse Width LOW		15			ns
t_{REC}	Recovery Time $\overline{MR}$ to CP		10			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max	Q0, Q7	2.7	3.4		V
		V_{IL} = Max	I/O0–I/O7	2.4			
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	Inputs			0.1	mA
			Sn			0.2	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V	Sn			40	µA
			Inputs			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V	Sn			−0.8	mA
			Inputs			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	Q_0, Q_7	−20		−100	mA
			I/O_0–I/O_7	−30		−130	
I_{CC}	Supply Current	V_{CC} = Max, $\overline{OE}$ = 4.5V				60	mA
I_{OZH}	3-STATE Output Off Current HIGH	V_{CC} = Max V_O = 2.7V				40	µA
I_{OZL}	3-STATE Output Off Current Low	V_{CC} = Max V_O = 0.4V				−400	µA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

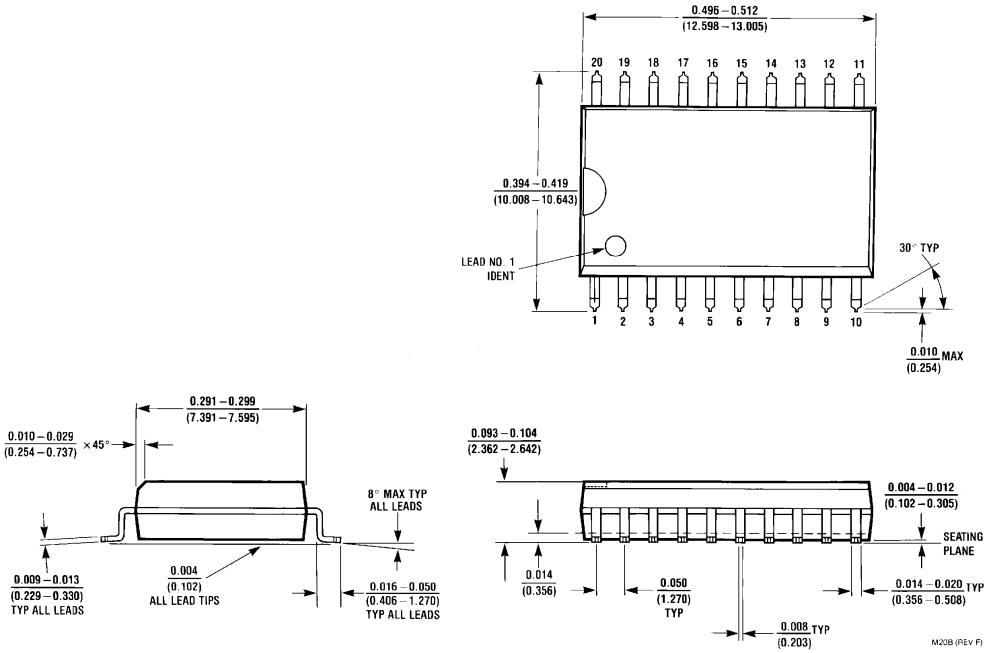
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C

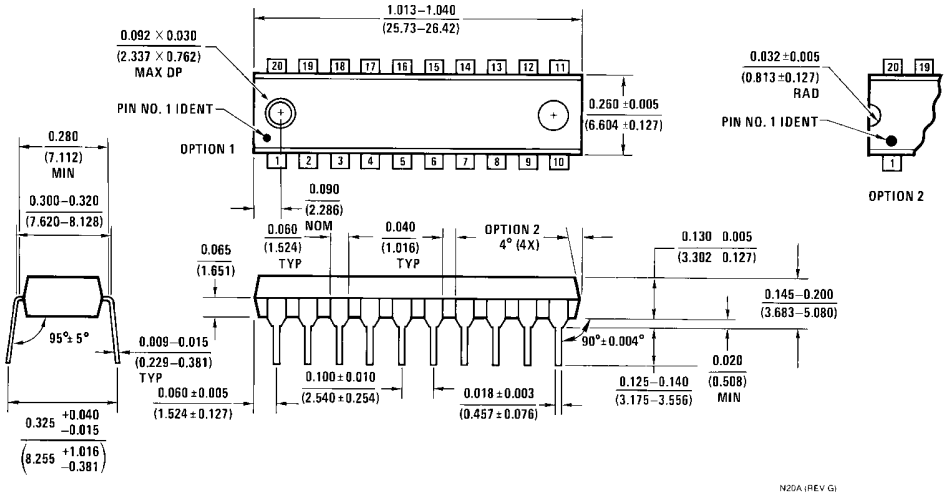
Symbol	Parameter	R_L = 2 kΩ C_L = 15 pF		Units
		Min	Max	
f_{MAX}	Maximum Input Frequency	35		MHz
t_{PLH}	Propagation Delay		26	ns
t_{PHL}	CP to Q0 or Q7		28	
t_{PLH}	Propagation Delay		25	ns
t_{PHL}	CP to I/O_n		35	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q0 or Q7		28	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n		35	ns
t_{PZH}	Output Enable Time		18	ns
t_{PZL}			25	
t_{PHZ}	Output Disable Time		15	ns
t_{PLZ}			20	

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A