FAIRCHILD SEMICONDUCTOR™

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# DM74LS390
# Dual 4-Bit Decade Counter

## General Description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The DM74LS390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The DM74LS390 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

## Features

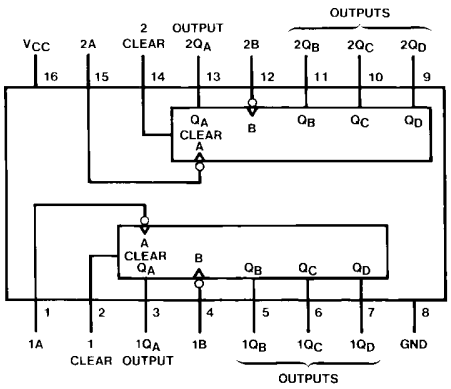
- Dual version of the popular DM74LS90
- DM74LS390…individual clocks for A and B flip-flops provide dual ÷ 2 and ÷ 5 counters
- Direct clear for each 4-bit counter
- Dual 4-bit version can significantly improve system densities by reducing counter package count by 50%
- Typical maximum count frequency…35 MHz
- Buffered outputs reduce possibility of collector commutation

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| DM74LS390M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| DM74LS390N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram



## Function Tables

### BCD Count Sequence

**(Each Counter) (Note 1)**

| Count | Outputs | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

### Bi-Quinary (5-2)

**(Each Counter) (Note 2)**

| Count | Outputs | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

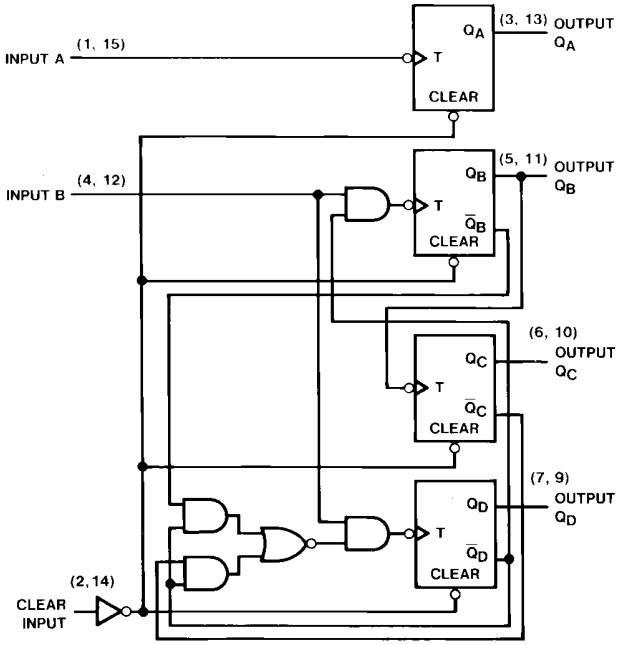
H = HIGH Level

L = LOW Level

**Note 1:** Output $Q_A$ is connected to input B for BCD count.

**Note 2:** Output $Q_D$ is connected to input A for Bi-quinary count.

## Logic Diagram



## Absolute Maximum Ratings(Note 3)

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | |
| Clear | 7V |
| A or B | 5.5V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |

**Note 3:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | | Min | Nom | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | HIGH Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | LOW Level Input Voltage | | | | 0.8 | V |
| $I_{OH}$ | HIGH Level Output Current | | | | −0.4 | mA |
| $I_{OL}$ | LOW Level Output Current | | | | 8 | mA |
| $f_{CLK}$ | Clock Frequency (Note 4) | A to $Q_A$ | 0 | | 25 | MHz |
| | | B to $Q_B$ | 0 | | 20 | |
| $f_{CLK}$ | Clock Frequency (Note 5) | A to $Q_A$ | 0 | | 20 | MHz |
| | | B to $Q_B$ | 0 | | 15 | |
| $t_W$ | Pulse Width (Note 4) | A | 20 | | | ns |
| | | B | 25 | | | |
| | | Clear HIGH | 20 | | | |
| $t_{REL}$ | Clear Release Time (Note 6)(Note 7) | | 25↓ | | | ns |
| $T_A$ | Free Air Operating Temperature | | 0 | | 70 | °C |

**Note 4:** $C_L$ = 15 pF, $R_L$ = 2 kΩ, $T_A$ = 25°C and $V_{CC}$ = 5V.

**Note 5:** $C_L$ = 50 pF, $R_L$ = 2 kΩ, $T_A$ = 25°C and $V_{CC}$ = 5V.

**Note 6:** The symbol (↓) indicates the falling edge of the clear pulse is used for reference.

**Note 7:** $T_A$ = 25°C and $V_{CC}$ = 5V.

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | | Min | Typ (Note 8) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | −1.5 | V |
| $V_{OH}$ | HIGH Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max<br>$V_{IL}$ = Max, $V_{IH}$ = Min | | 2.7 | 3.4 | | V |
| $V_{OL}$ | LOW Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max<br>$V_{IL}$ = Max, $V_{IH}$ = Min | | | 0.35 | 0.5 | V |
| | | $I_{OL}$ = 4 mA, $V_{CC}$ = Min | | | 0.25 | 0.4 | |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = Max, $V_I$ = 7V | Clear | | | 0.1 | mA |
| | | $V_{CC}$ = Max | A | | | 0.2 | |
| | | $V_I$ = 5.5V | B | | | 0.4 | |
| $I_{IH}$ | HIGH Level Input Current | $V_{CC}$ = Max | Clear | | | 20 | µA |
| | | $V_I$ = 2.7V | A | | | 40 | |
| | | | B | | | 80 | |
| $I_{IL}$ | LOW Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4V | Clear | | | −0.4 | mA |
| | | | A | | | −1.6 | |
| | | | B | | | −2.4 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (Note 9) | | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (Note 10) | | | 15 | 26 | mA |

**Note 8:** All typicals are at $V_{CC}$ = 5V, $T_A$ = 25°C.

**Note 9:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

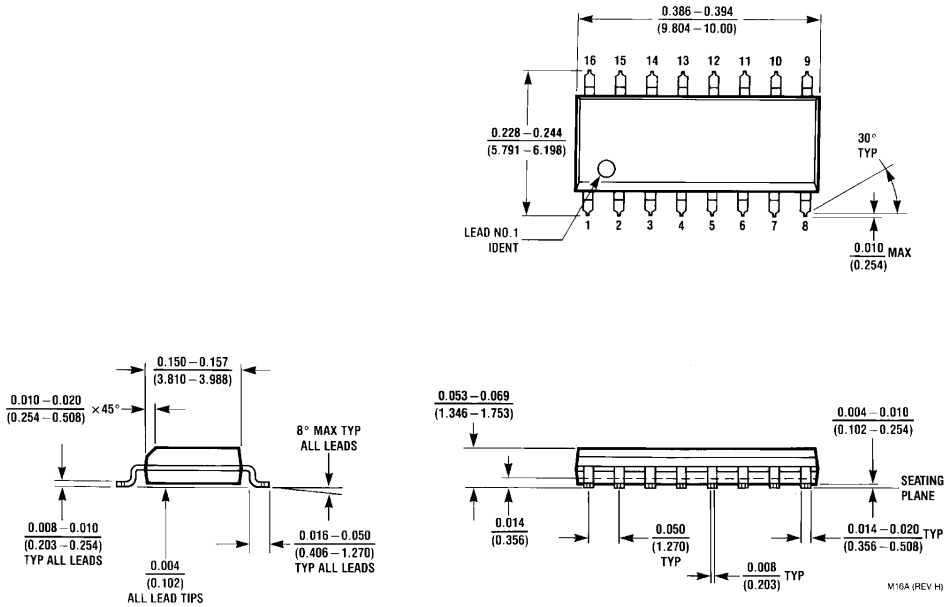
**Note 10:** $I_{CC}$ is measured with all outputs OPEN, both CLEAR inputs grounded following momentary connection to 4.5 and all other inputs grounded.

## Switching Characteristics

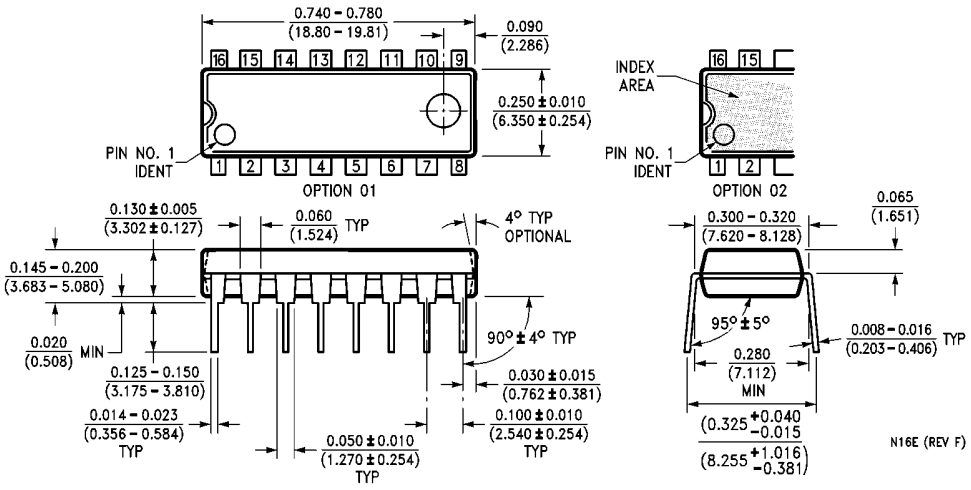
at $V_{CC} = 5V$ and $T_A = 25°C$

| Symbol | Parameter | From (Input) To (Output) | $R_L = 2\ k\Omega$ | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | $C_L = 15$ pF | | $C_L = 50$ pF | | |
| | | | Min | Max | Min | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | A to $Q_A$ | 25 | | 20 | | MHz |
| | | B to $Q_B$ | 20 | | 15 | | |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | A to $Q_A$ | | 20 | | 24 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | A to $Q_A$ | | 20 | | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | A to $Q_C$ | | 60 | | 81 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | A to $Q_C$ | | 60 | | 81 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | B to $Q_B$ | | 21 | | 27 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | B to $Q_B$ | | 21 | | 33 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | B to $Q_C$ | | 39 | | 51 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | B to $Q_C$ | | 39 | | 54 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | B to $Q_D$ | | 21 | | 27 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | B to $Q_D$ | | 21 | | 33 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | Clear to Any Q | | 39 | | 45 | ns |

## Physical Dimensions inches (millimeters) unless otherwise noted




**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow**
**Package Number M16A**




**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N16E**