FAIRCHILD SEMICONDUCTOR™

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DM93S62
9-Input Parity Checker/Generator

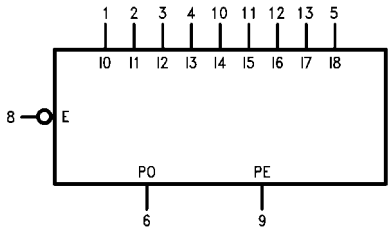
General Description

The DM93S62 is a very high speed 9-input parity checker/generator for use in error detection and error correction applications. The DM93S62 provides odd and even parity for up to nine data bits. The even parity output (PE) is HIGH if an even number of inputs are HIGH and $\overline{E}$ is LOW. The odd parity output (PO) will be HIGH if an odd number of inputs are HIGH and $\overline{E}$ is LOW. A HIGH level on the Enable ($\overline{E}$) input forces both outputs LOW.

Ordering Code:

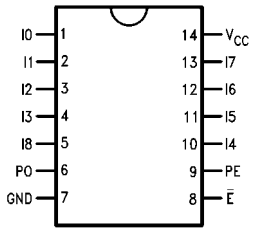
Order Number	Package Number	Package Description
DM93S62N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

Connection Diagram



Pin Descriptions

Pin Name	Description
I0–I8	Data Inputs
$\overline{E}$	Output Enable (Active LOW)
PO	Odd Parity Output
PE	Even Parity Output

Truth Table

($\overline{E}$ = LOW)

Number of Inputs I0–I8 that are HIGH	Outputs PO	Outputs PE
1, 3, 5, 7, 9	H	L
0, 2, 4, 6, 8	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

Functional Description

The DM93S62 is a very high speed 9-input parity checker or generator. It is intended primarily for error detection in systems which transmit data in 8-bit bytes, but it can be expanded to any number of data inputs. Both even and odd parity outputs are available to allow maximum flexibility for both parity generation and parity checking. When the device is enabled ($\overline{E}$ = LOW), the Even Parity output (PE) is HIGH when an even number of inputs is HIGH, and the Odd Parity output (PO) is HIGH when an odd number of inputs is HIGH. The active LOW Enable ($\overline{E}$) controls the state of both outputs; when the Enable ($\overline{E}$) is HIGH, both outputs will be LOW. The Enable may be used to strobe the outputs at very high speeds to synchronize or inhibit the parity data.

The DM93S62 has been designed with two sections using Exclusive-NOR comparison techniques. Eight data inputs I0–I7 represent one section which will generate a parity bit in 16 ns to 20 ns. The ninth input (I8) bypasses three levels of logic and switches the outputs in 6.0 ns to 9.0 ns. This feature may be used to compensate for delayed arrival of the parity bit, allowing faster system cycle times (Figure 1). The fast I8 input is also useful when more than nine bits are to be checked. The output of one DM93S62 drives the I8 input of a second DM93S62, providing a 17-bit parity check in 29 ns (typ).

When some inputs of the DM93S62 are not used, such as for words of less than nine bits or when using parallel expansion techniques, there is an optimum delay scheme for termination of the unused inputs (see Table 1). In essence, if one of the inputs of any Exclusive-NOR stays HIGH, the delay from the other input to the output is minimized.

TABLE 1. Termination Recommendations for Less than Nine Bits

Number of Data Inputs	I0	I1	I2	I3	I4	I5	I6	I7	I8
3	D0	L	D1	L	D2	L	L	L	L
4	D0	L	D1	L	D2	L	D3	L	L
5	D0	L	D1	L	D2	L	D3	L	D4
6	D0	D1	D2	D3	D4	L	D5	L	L
7	D0	D1	D2	D3	D4	L	D5	L	D6
8	D0	D1	D2	D3	D4	D5	D6	D7	L

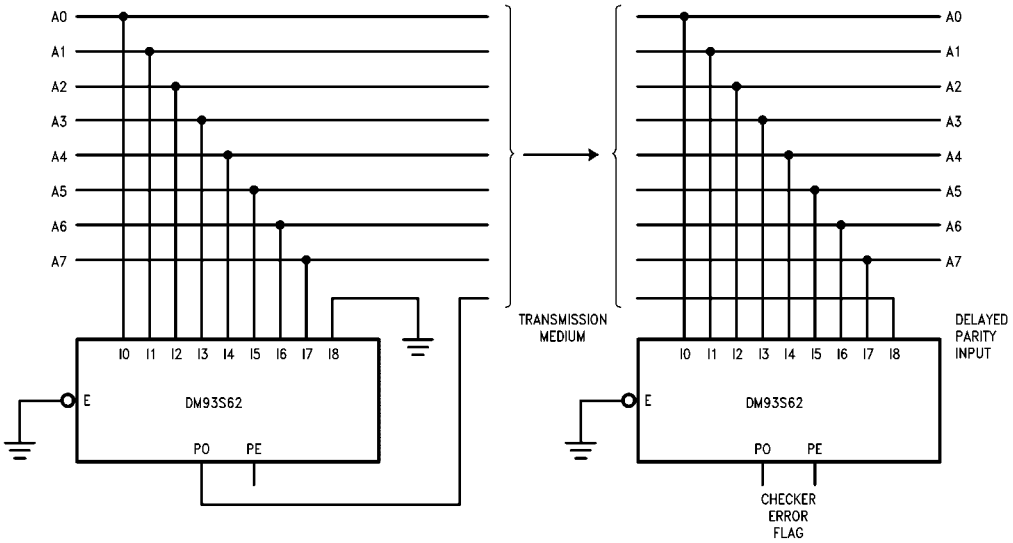
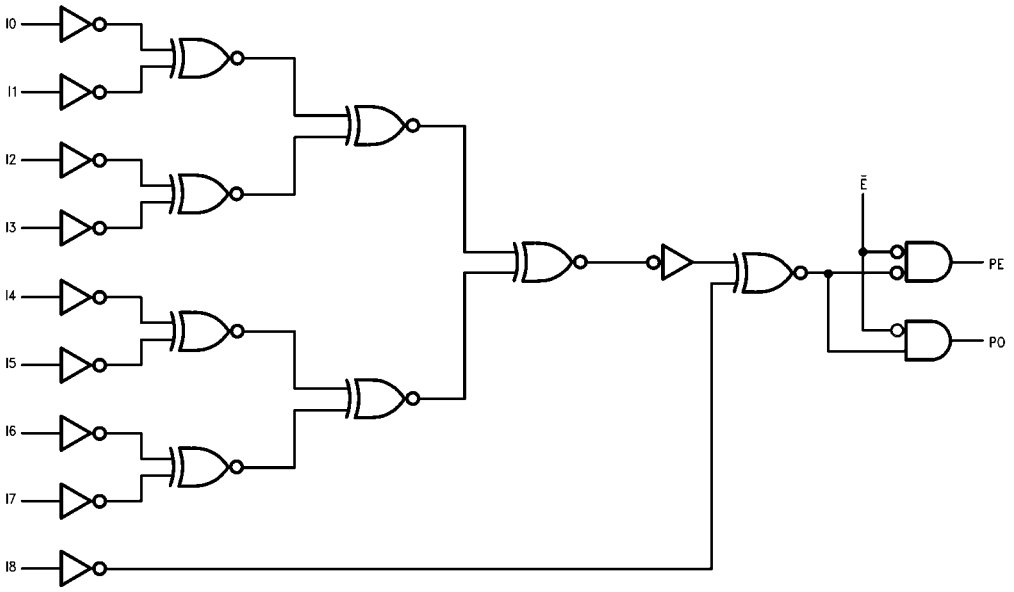


FIGURE 1. Fast Input I8 allows Higher System Speed

Logic Diagram



$$PO = (I0 \oplus I1 \oplus I2 \oplus I3 \oplus I4 \oplus I5 \oplus I6 \oplus I7 \oplus I8) \cdot \bar{E}$$

$$PE = \overline{(I0 \oplus I1 \oplus I2 \oplus I3 \oplus I4 \oplus I5 \oplus I6 \oplus I7 \oplus I8) \cdot \bar{E}}$$

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−1	mA
I_{OL}	LOW Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			50	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.5V, I0–I8			−1.6	mA
		V_{CC} = Max, V_I = 0.5V, $\overline{E}$ Only			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			65	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

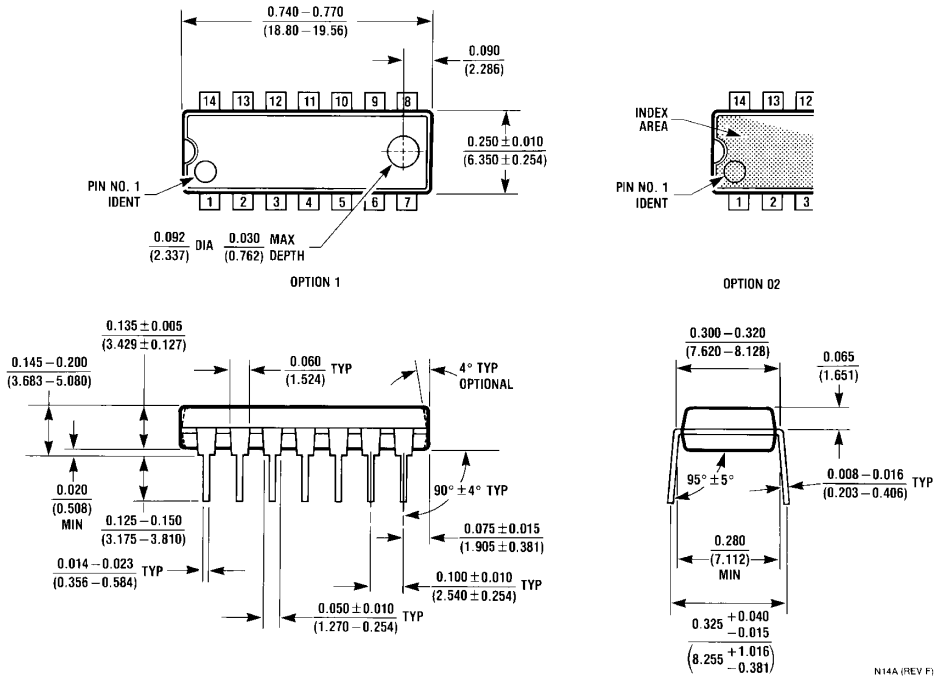
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay		26	ns
t_{PHL}	I0–I7 to PE		22	
t_{PLH}	Propagation Delay		12	ns
t_{PHL}	I8 to PE		9.0	
t_{PLH}	Propagation Delay		26	ns
t_{PHL}	I0–I7 to PO		26	
t_{PLH}	Propagation Delay		13	ns
t_{PHL}	I8 to PO		13	
t_{PLH}	Propagation Delay		7.0	ns
t_{PHL}	$\overline{E}$ to PE		7.0	
t_{PLH}	Propagation Delay		7.0	ns
t_{PHL}	$\overline{E}$ to PO		7.0	

Physical Dimensions inches (millimeters) unless otherwise noted



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