

## FDC6321C Dual N & P Channel , Digital FET

### General Description

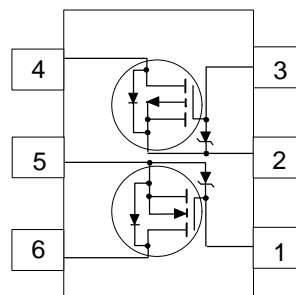
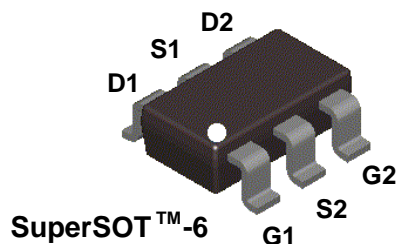
These dual N & P Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors in load switching applications. Since bias resistors are not required this dual digital FET can replace several digital transistors with different bias resistors.

### Features

- N-Ch 25 V, 0.68 A,  $R_{DS(ON)} = 0.45 \Omega @ V_{GS} = 4.5 V$
- P-Ch -25 V, -0.46 A,  $R_{DS(ON)} = 1.1 \Omega @ V_{GS} = -4.5 V$ .
- Very low level gate drive requirements allowing direct operation in 3 V circuits.  $V_{GS(th)} < 1.0V$ .
- Gate-Source Zener for ESD ruggedness. >6kV Human Body Model
- Replace multiple dual NPN & PNP digital transistors.



Mark: .321



### Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
$V_{DSS}, V_{CC}$	Drain-Source Voltage, Power Supply Voltage	25	-25	V
$V_{GSS}, V_{IN}$	Gate-Source Voltage,	8	-8	V
$I_D, I_O$	Drain/Output Current - Continuous - Pulsed	0.68	-0.46	A
		2	-1.5	
$P_D$	Maximum Power Dissipation (Note 1a) (Note 1b)	0.9		W
		0.7		
$T_J, T_{STG}$	Operating and Storage Temperature Ranges	-55 to 150		$^\circ C$
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)	6		kV

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	140	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	60	$^\circ C/W$

**Electrical Characteristics** ( $T_A = 25\text{ }^\circ\text{C}$  unless otherwise noted )

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	25			V
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-25			
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$	N-Ch		26		$\text{mV}/^\circ\text{C}$
		$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$	P-Ch		-22		
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$ , $T_J = 55^\circ\text{C}$	N-Ch			1 10	$\mu\text{A}$
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$ , $T_J = 55^\circ\text{C}$	P-Ch			-1 -10	
$I_{GSS}$	Gate - Body Leakage Current	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$	N-Ch			100	nA
		$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$	P-Ch			-100	
<b>ON CHARACTERISTICS</b> (Note 2)							
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$	N-Ch		-2.6		$\text{mV}/^\circ\text{C}$
		$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$	P-Ch		2.1		
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.65	0.8	1.5	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.65	-0.86	-1.5	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 0.5\text{ A}$ , $T_J = 125^\circ\text{C}$	N-Ch		0.33	0.45	$\Omega$
					0.51	0.72	
		$V_{GS} = 2.7\text{ V}, I_D = 0.25\text{ A}$			0.44	0.6	
		$V_{GS} = -4.5\text{ V}, I_D = -0.5\text{ A}$ , $T_J = 125^\circ\text{C}$	P-Ch		0.87	1.1	
$V_{GS} = -2.7\text{ V}, I_D = -0.25\text{ A}$		1.21		1.8			
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	N-Ch	1			A
		$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	P-Ch	-1			
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 0.5\text{ A}$	N-Ch		1.45		S
		$V_{DS} = -5\text{ V}, I_D = -0.5\text{ A}$	P-Ch		0.8		
<b>DYNAMIC CHARACTERISTICS</b>							
$C_{iss}$	Input Capacitance	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}$	N-Ch		50		pF
			P-Ch		63		
$C_{oss}$	Output Capacitance	f = 1.0 MHz P-Channel	N-Ch		28		pF
			P-Ch		34		
$C_{rss}$	Reverse Transfer Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}$ , f = 1.0 MHz	N-Ch		9		pF
			P-Ch		10		

## Electrical Characteristics ( $T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted )

### SWITCHING CHARACTERISTICS (Note 2)

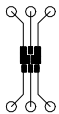
Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
$t_{D(on)}$	Turn - On Delay Time	N-Channel $V_{DD} = 6\text{ V}, I_D = 0.5\text{ A},$	N-Ch		3	6	nS
			P-Ch		7	20	
$t_r$	Turn - On Rise Time	$V_{GS} = 4.5\text{ V}, R_{GEN} = 50\ \Omega$	N-Ch		8	16	nS
			P-Ch		9	18	
$t_{D(off)}$	Turn - Off Delay Time	P-Channel $V_{DD} = -6\text{ V}, I_D = -0.5\text{ A},$	N-Ch		17	30	nS
			P-Ch		55	110	
$t_f$	Turn - Off Fall Time	$V_{Gen} = -4.5\text{ V}, R_{GEN} = 50\ \Omega$	N-Ch		13	25	nS
			P-Ch		35	70	
$Q_g$	Total Gate Charge	N-Channel $V_{DS} = 5\text{ V}, I_D = 0.5\text{ A},$	N-Ch		1.64	2.3	nC
			P-Ch		1.1	1.5	
$Q_{gs}$	Gate-Source Charge	$V_{GS} = 4.5\text{ V}$	N-Ch		0.38		nC
			P-Ch		0.32		
$Q_{gd}$	Gate-Drain Charge	$V_{DS} = -5\text{ V},$ $I_D = -0.25\text{ A}, V_{GS} = -4.5\text{ V}$	N-Ch		0.45		nC
			P-Ch		0.25		

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

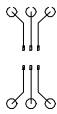
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			0.3	A
			P-Ch			-0.5	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.5\text{ A}$ (Note)	N-Ch		0.83	1.2	V
				$T_J = 125^\circ\text{C}$		0.69	
		$V_{GS} = 0\text{ V}, I_S = -0.5\text{ A}$ (Note)	P-Ch		-0.89	-1.2	
				$T_J = 125^\circ\text{C}$		-0.75	

#### Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.
- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .



a.  $140^\circ\text{C/W}$  on a  $0.125\text{ in}^2$  pad of 2oz copper.



b.  $180^\circ\text{C/W}$  on a  $0.005\text{ in}^2$  of pad of 2oz copper.

## Typical Electrical Characteristics: N-Channel

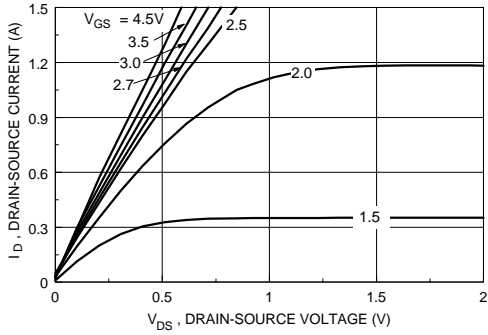


Figure 1. On-Region Characteristics.

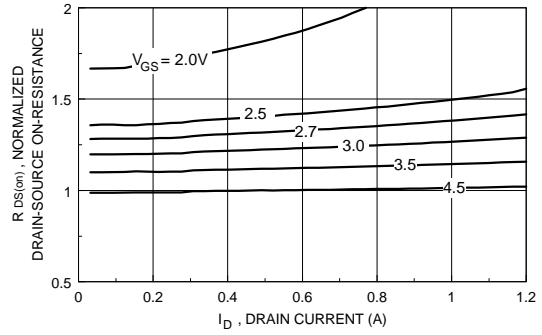


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

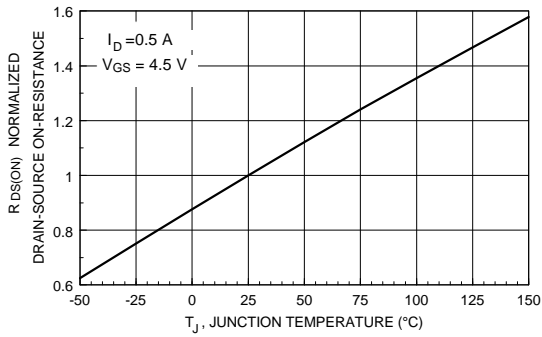


Figure 3. On-Resistance Variation with Temperature.

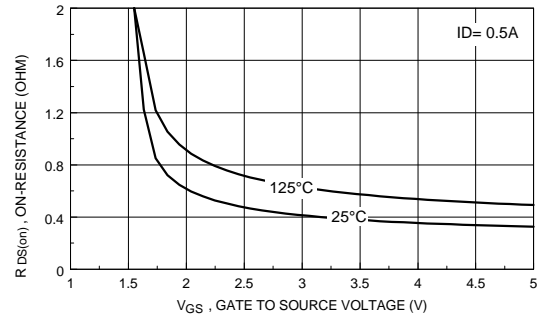


Figure 4. On Resistance Variation with Gate-To-Source Voltage.

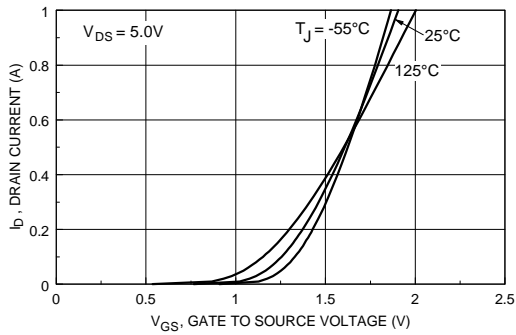


Figure 5. Transfer Characteristics.

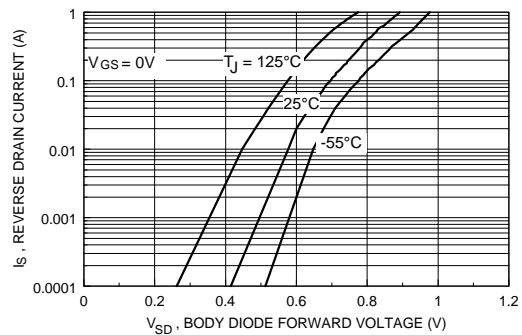


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Electrical Characteristics: N-Channel (continued)

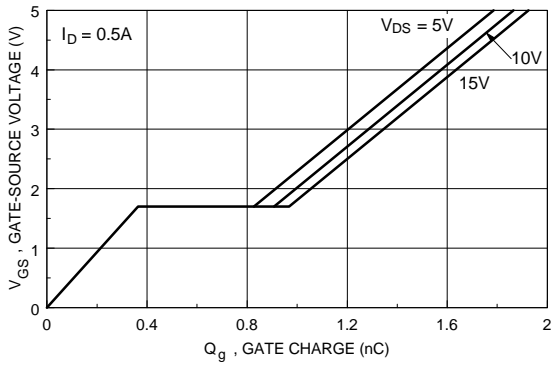


Figure 7. Gate Charge Characteristics.

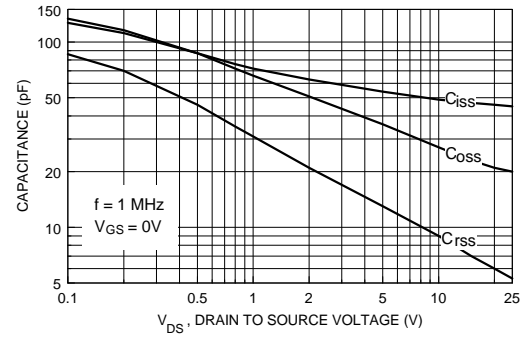


Figure 8. Capacitance Characteristics.

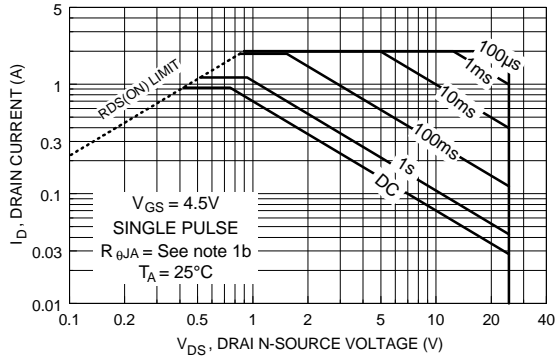


Figure 9. Maximum Safe Operating Area.

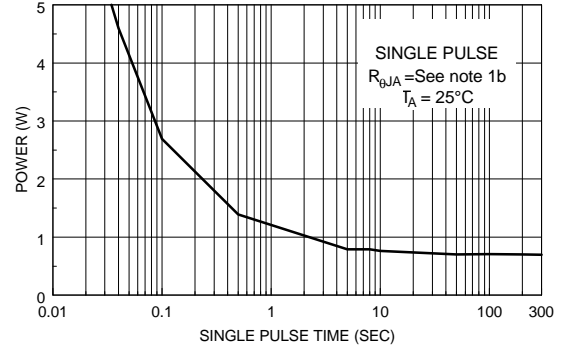


Figure 10. Single Pulse Maximum Power Dissipation.

## Typical Electrical Characteristics: P-Channel

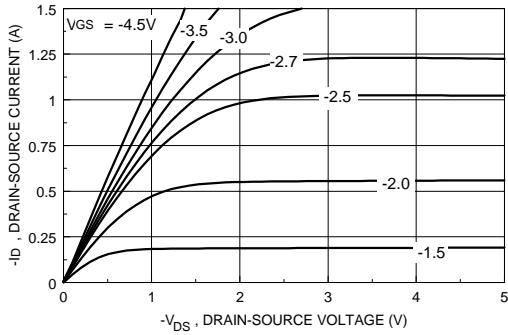


Figure 11. On-Region Characteristics.

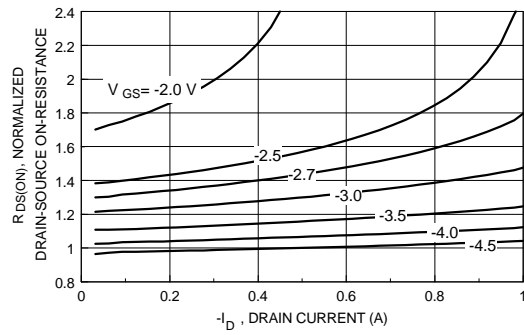


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

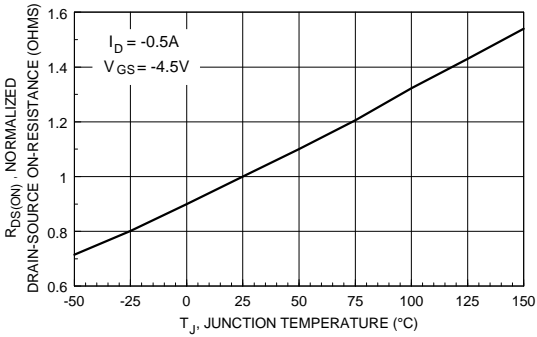


Figure 13. On-Resistance Variation with Temperature.

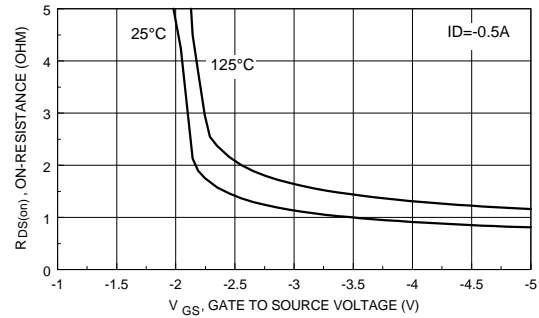


Figure 14. On Resistance Variation with Gate-To-Source Voltage.

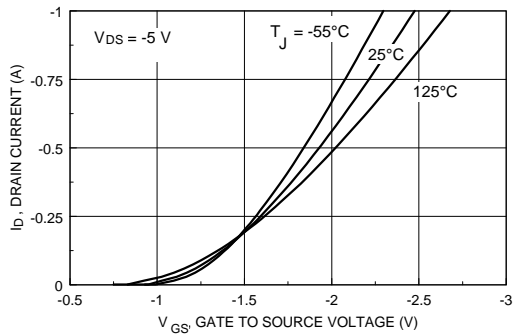


Figure 15. Transfer Characteristics.

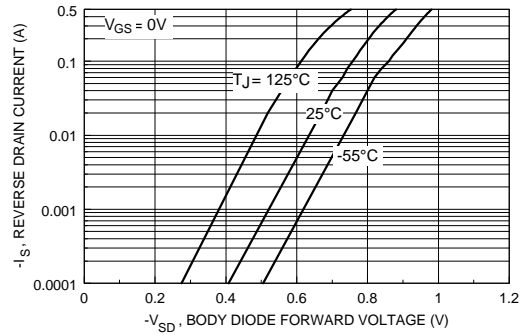


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Electrical Characteristics: P-Channel (continued)

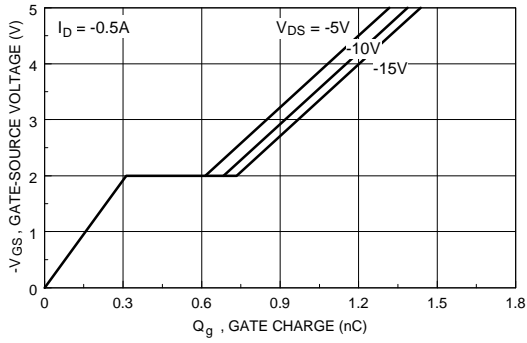


Figure 17. Gate Charge Characteristics.

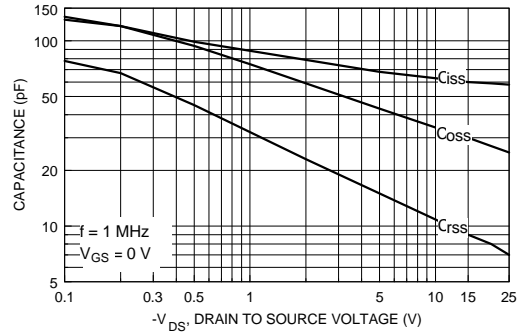


Figure 18. Capacitance Characteristics.

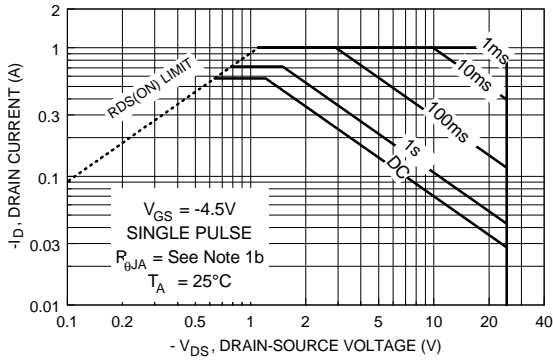


Figure 19. Maximum Safe Operating Area.

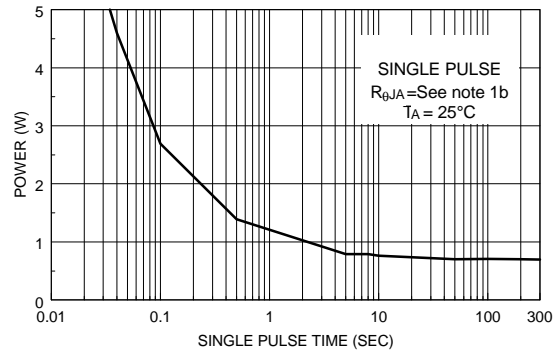


Figure 20. Single Pulse Maximum Power Dissipation.

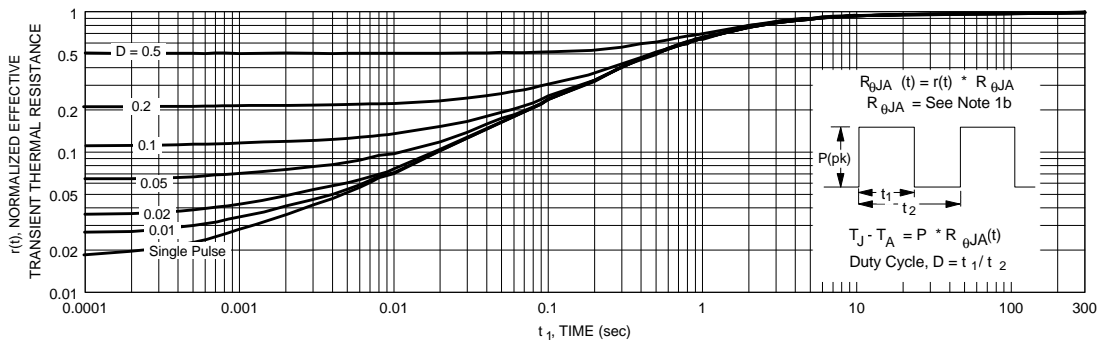
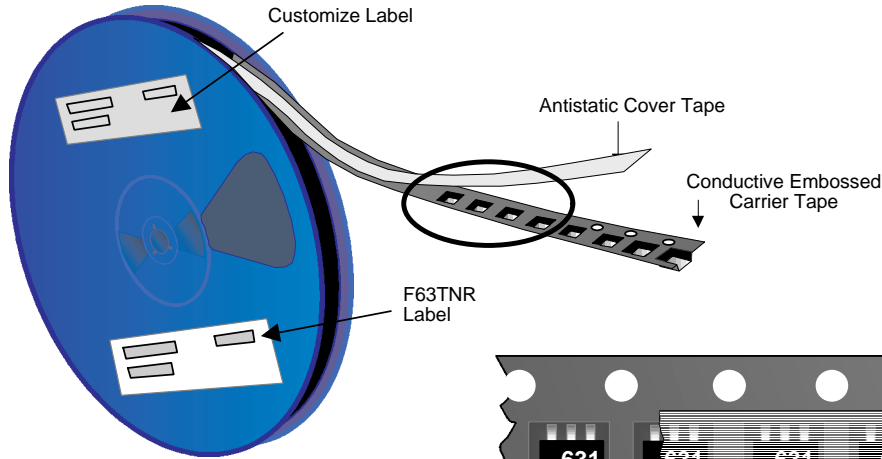


Figure 21. Transient Thermal Response Curve.

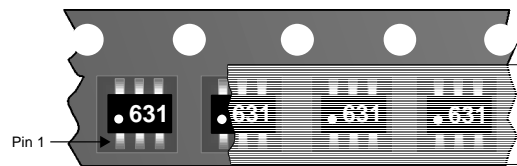
Note: Thermal characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

# SuperSOT™-6 Tape and Reel Data and Package Dimensions

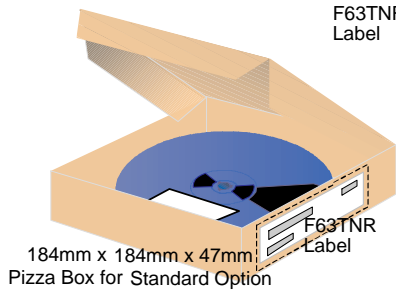
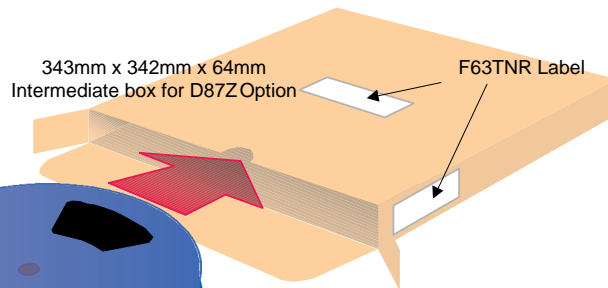
**SSOT-6 Packaging**  
Configuration: Figure 1.0



SSOT-6 Packaging Information		
Packaging Option	Standard (no flow code)	D87Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	10,000
Reel Size	7" Dia	13"
Box Dimension (mm)	184x187x47	343x343x64
Max qty per Box	9,000	20,000
Weight per unit (gm)	0.0158	0.0158
Weight per Reel (kg)	0.1440	0.4700
Note/Comments		



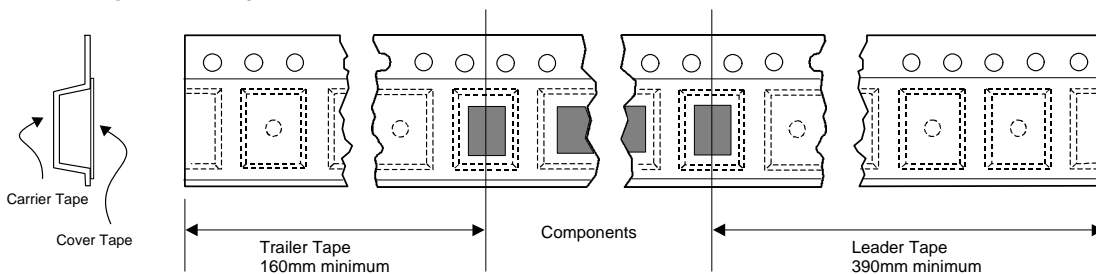
**SSOT-6 Unit Orientation**



**F63TNR Label sample**



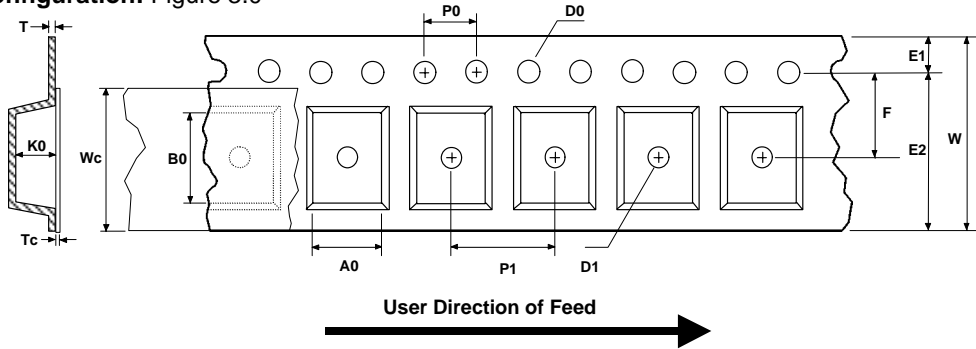
**SSOT-6 Tape Leader Trailer Configuration: Figure 2.0**





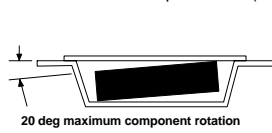
# SuperSOT™-6 Tape and Reel Data and Package Dimensions, continued

## SSOT-6 Embossed Carrier Tape Configuration: Figure 3.0

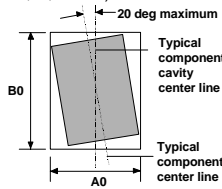


Dimensions are in millimeter														
Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SSOT-6 (8mm)	3.23 +/-0.10	3.18 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.00 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.255 +/-0.150	5.2 +/-0.3	0.06 +/-0.02

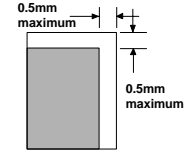
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)  
Component Rotation

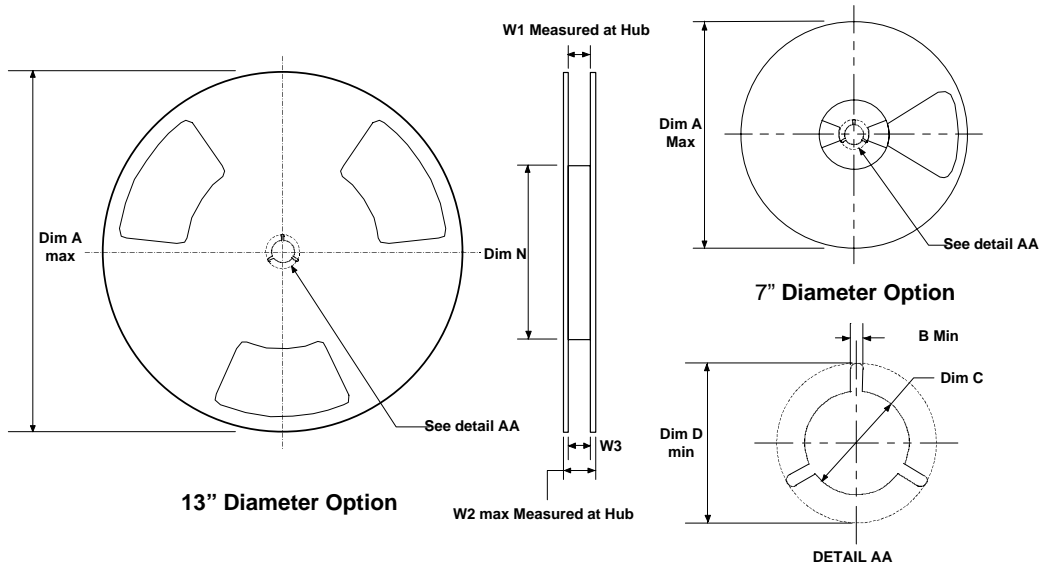


Sketch B (Top View)  
Component Rotation



Sketch C (Top View)  
Component lateral movement

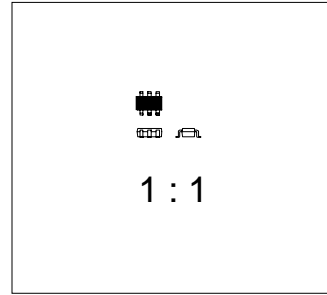
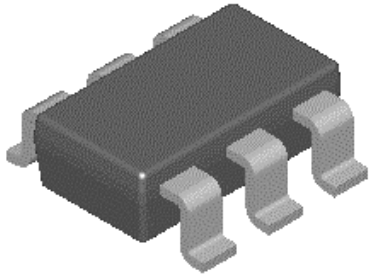
## SSOT-6 Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9

**SuperSOT™-6 Tape and Reel Data and Package Dimensions, continued**

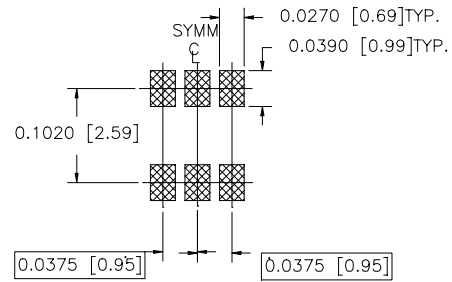
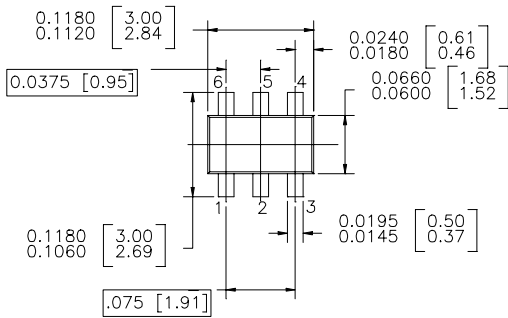
**SuperSOT™-6 (FS PKG Code 31, 33)**



Scale 1:1 on letter size paper

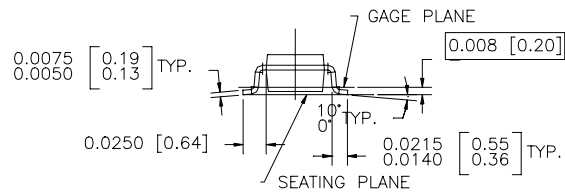
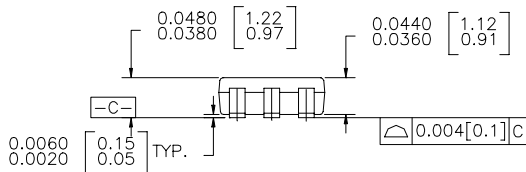
Dimensions shown below are in:  
inches [millimeters]

Part Weight per unit (gram): 0.0158



LAND PATTERN RECOMMENDATION

CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS



SUPER SOT 6 LEADS

NOTES : UNLESS OTHERWISE SPECIFIED

1.0 STANDARD LEAD FINISH : 150 MICRONS 93.81 MICROMETERS)  
MINIMUM TIN / LEAD (SOLDER) ON COPPER.

2.0 NO JEDEC REGISTRATION AS OF JULY 1996

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FACT™	QS™
FACT Quiet Series™	Quiet Series™
FAST®	SuperSOT™-3
FASTr™	SuperSOT™-6
GTO™	SuperSOT™-8
HiSeC™	TinyLogic™

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.