

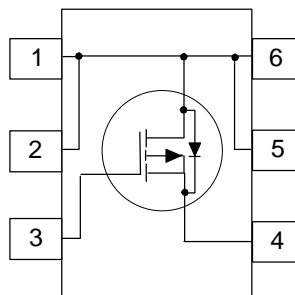
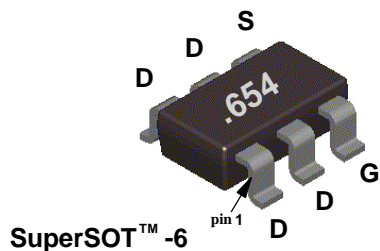
## FDC654P P-Channel Enhancement Mode Field Effect Transistor

### General Description

These P-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

### Features

- -3.6 A, -30 V.  $R_{DS(ON)} = 0.075 \Omega @ V_{GS} = -10 \text{ V}$   
 $R_{DS(ON)} = 0.125 \Omega @ V_{GS} = -4.5 \text{ V}$ .
- SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- Exceptional on-resistance and maximum DC current capability.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise note

Symbol	Parameter	FDC654P	Units
$V_{DSS}$	Drain-Source Voltage	-30	V
$V_{GSS}$	Gate-Source Voltage - Continuous	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1a)	-3.6	A
	- Pulsed	-10	
$P_D$	Maximum Power Dissipation (Note 1a) (Note 1b)	1.6	W
		0.8	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	30	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>OFF CHARACTERISTICS</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-30			V	
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-29		$\text{mV}/^\circ\text{C}$	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$	
					-10	$\mu\text{A}$	
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA	
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA	
<b>ON CHARACTERISTICS</b> (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1	-1.7	-3	V	
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		3.6		$\text{mV}/^\circ\text{C}$	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -3.6\text{ A}$		0.065	0.075	$\Omega$	
					0.094		0.127
					0.11		0.125
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-5			A	
$g_{FS}$	Forward Transconductance	$V_{DS} = -10\text{ V}, I_D = -3.6\text{ A}$		3		S	
<b>DYNAMIC CHARACTERISTICS</b>							
$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		435		pF	
$C_{oss}$	Output Capacitance			245		pF	
$C_{rss}$	Reverse Transfer Capacitance			70		pF	
<b>SWITCHING CHARACTERISTICS</b> (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = -15\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$		10	18	ns	
$t_r$	Turn - On Rise Time			7	14	ns	
$t_{D(off)}$	Turn - Off Delay Time			26	42	ns	
$t_f$	Turn - Off Fall Time			18	29	ns	
$Q_g$	Total Gate Charge		$V_{DS} = -15\text{ V}, I_D = -3.6\text{ A},$		10.5	15	nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = -10\text{ V}$		2		nC	
$Q_{gd}$	Gate-Drain Charge			2.6		nC	
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>							
$I_S$	Continuous Source Diode Current				-1.3	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)		-0.8	-1.2	V	
				-0.62	-1		

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

- $78^\circ\text{C}/\text{W}$  when mounted on a minimum on a  $1\text{ in}^2$  pad of 2oz Cu in FR-4 board.
- $156^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2oz Cu in FR-4 board.

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

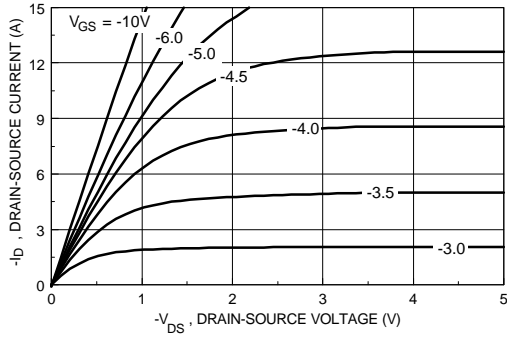


Figure 1. On-Region Characteristics.

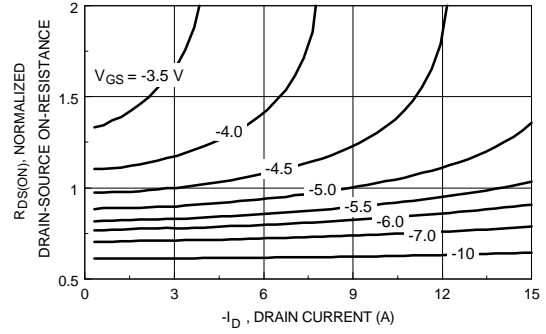


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

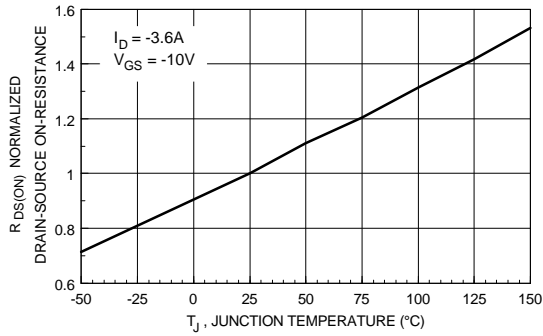


Figure 3. On-Resistance Variation with Temperature.

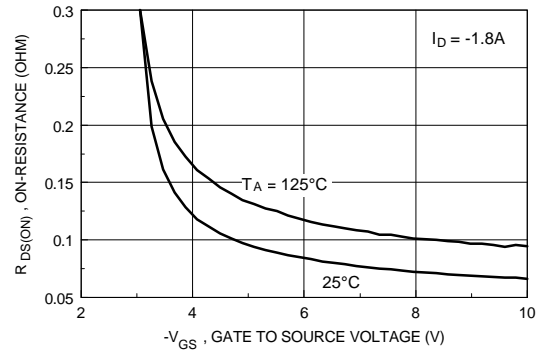


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

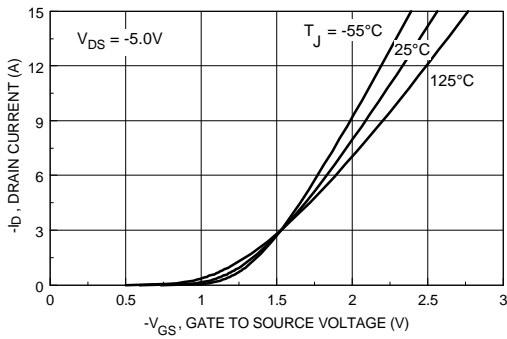


Figure 5. Transfer Characteristics.

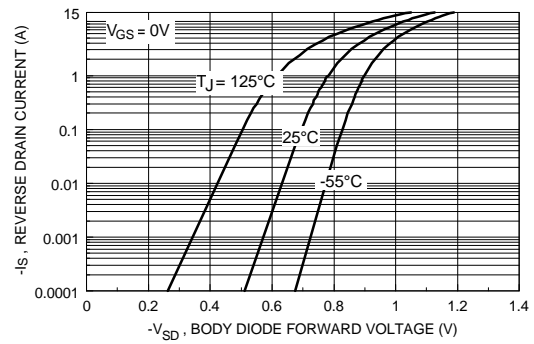


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Electrical And Thermal Characteristics

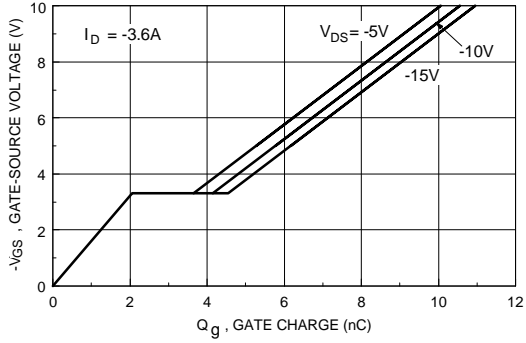


Figure 7. Gate Charge Characteristics.

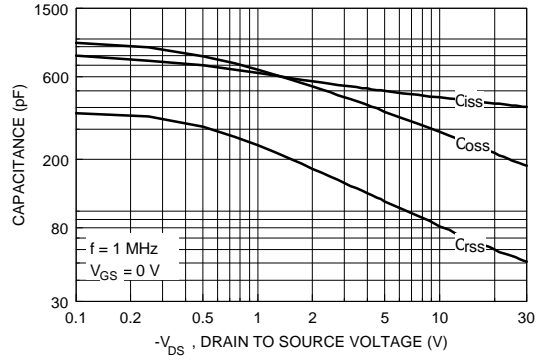


Figure 8. Capacitance Characteristics.

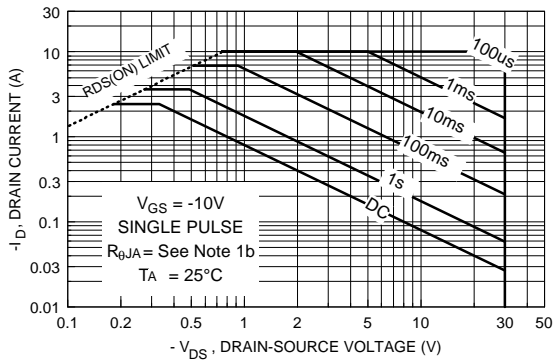


Figure 9. Maximum Safe Operating Area.

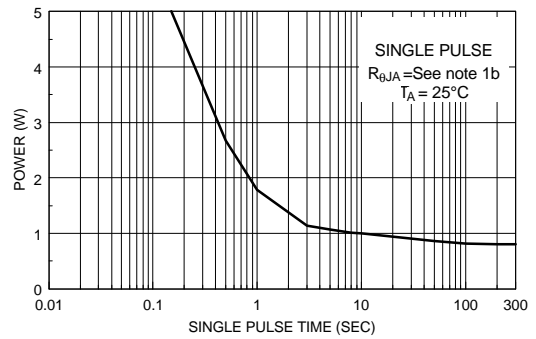


Figure 10. Single Pulse Maximum Power Dissipation.

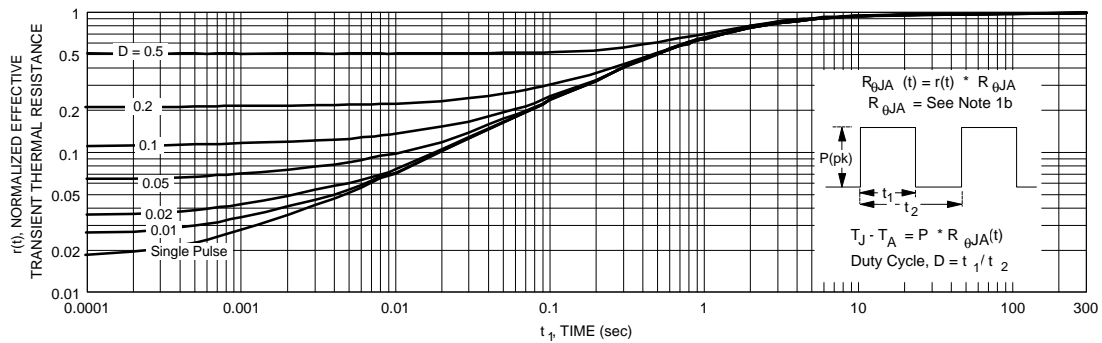


Figure 11. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.