

## FDP7042L / FDB7042L

## N-Channel Logic Level PowerTrench® MOSFET

### **General Description**

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for "low side" synchronous rectifier operation, providing an extremely low  $R_{\text{DS}(\text{ON})}$ .

### **Applications**

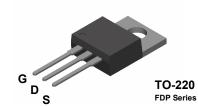
- · Synchronous rectifier
- DC/DC converter

#### **Features**

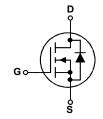
**TO-263AB** 

**FDB Series** 

- 50 A, 30 V.  $R_{DS(ON)} = 9 \text{ m}\Omega$  @  $V_{GS} = 4.5 \text{ V}$  $R_{DS(ON)} = 7.5 \text{ m}\Omega$  @  $V_{GS} = 10 \text{ V}$
- Critical DC electrical parameters specified at elevated temperature
- High performance trench technology for extremely low R<sub>DS(ON)</sub>
- 175°C maximum junction temperature rating







Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage		30	V
V <sub>GSS</sub>	Gate-Source Voltage		± 12	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1)	50	А
	– Pulsed	(Note 1)	150	
P <sub>D</sub>	Total Power Dissipation @ T <sub>C</sub> = 25°C		83	W
	Derate a	above 25°C	0.48	W∘C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temp	erature Range	-65 to +175	°C

### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	°C/W

**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape width	Quantity
FDB7042L	FDB7042L	13"	24mm	800 units
FDP7042L	FDP7042L	Tube	n/a	45

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics		l	ı	l	l
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
ΔBV <sub>DSS</sub> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		24		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage, Forward	V <sub>GS</sub> = 12 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	$V_{GS} = -12 \text{ V}$ $V_{DS} = 0 \text{ V}$			-100	nA
On Char	racteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	0.8	1.2	2	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		-4.1		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	$V_{GS} = 4.5 \text{ V}, \qquad I_D = 25 \text{A}$ $V_{GS} = 10 \text{ V}, \qquad I_D = 25 \text{A}$ $V_{GS} = 4.5 \text{ V}, I_D = 25 \text{A}, T_J = 125 ^{\circ}\text{C}$		6.2 5.5 9.6	9 7.5 16	mΩ
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 10 V	60			Α
<b>g</b> <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5V$ , $I_{D} = 25 A$		117		S
Dvnamio	Characteristics					
C <sub>iss</sub>	Input Capacitance			2418		pF
Coss	Output Capacitance	$V_{DS} = 15 \text{ V},  V_{GS} = 0 \text{ V},$		549		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f = 1.0 MHz		243		pF
Switchin	ng Characteristics (Note 2)		•	•	•	•
t <sub>d(on)</sub>	Turn–On Delay Time			21	34	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 15 \text{ V}, I_D = 1 \text{ A},$		20	32	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time	$V_{GS} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$		60	96	ns
t <sub>f</sub>	Turn-Off Fall Time			30	48	ns
Qg	Total Gate Charge			32	51	nC
Q <sub>gs</sub>	Gate-Source Charge	$V_{DS} = 15 \text{ V}, I_{D} = 50 \text{ A}, V_{GS} = 4.5 \text{ V}$		10		nC
$Q_{gd}$	Gate-Drain Charge	VG3 4.0 V		9		nC
Drain-S	ource Diode Characteristics a	and Maximum Ratings				
Is	Maximum Continuous Drain–Source				50	Α
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 25 A (Note 2)		0.8	1.3	V

#### Notes:

- 1. Maximum continuous current is limited by the package.
- 2. Pulse Test: Pulse Width < 300 $\mu$ s, Duty Cycle < 2.0%

## **Typical Characteristics**

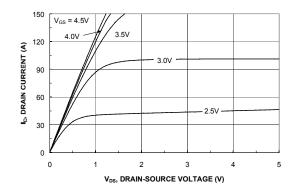
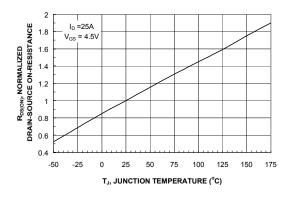


Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.



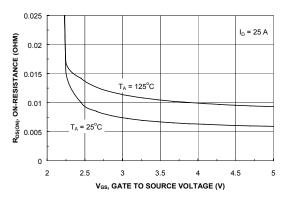
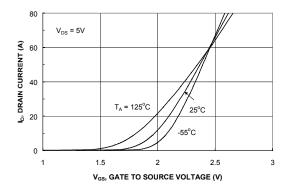


Figure 3. On-Resistance Variation withTemperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



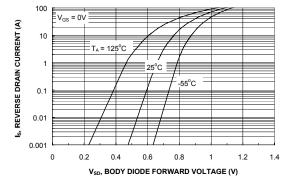
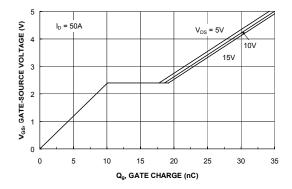


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## **Typical Characteristics**



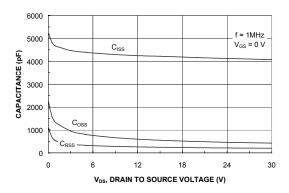
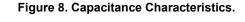
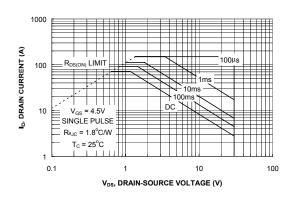


Figure 7. Gate Charge Characteristics.





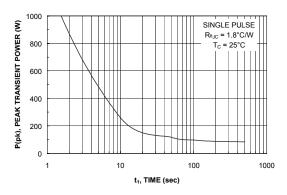


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

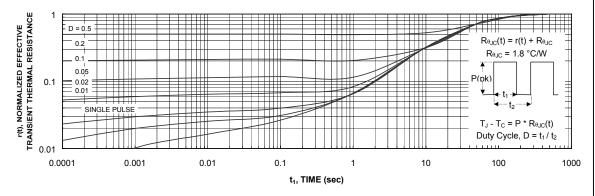
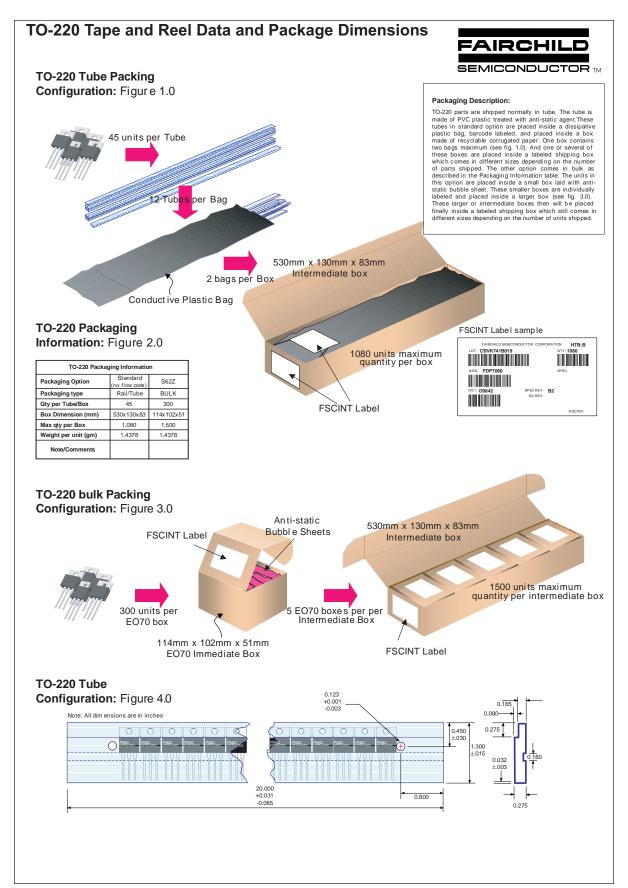


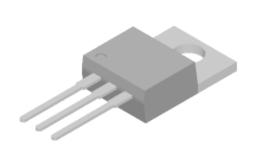
Figure 11. Transient Thermal Response Curve.

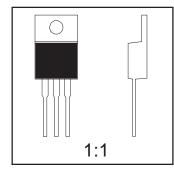
Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.



## TO-220 Tape and Reel Data and Package Dimensions, continued

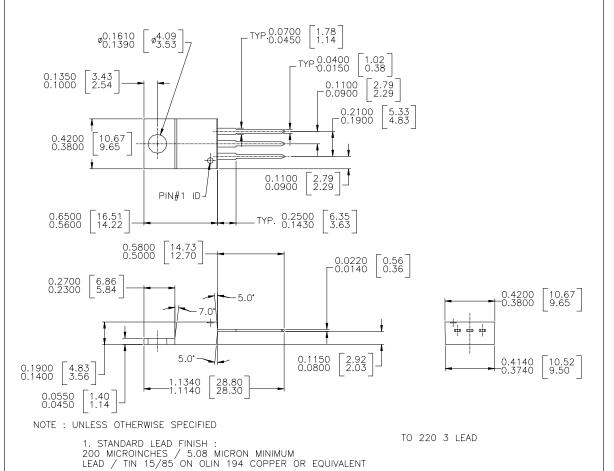
## TO-220 (FS PKG Code 37)

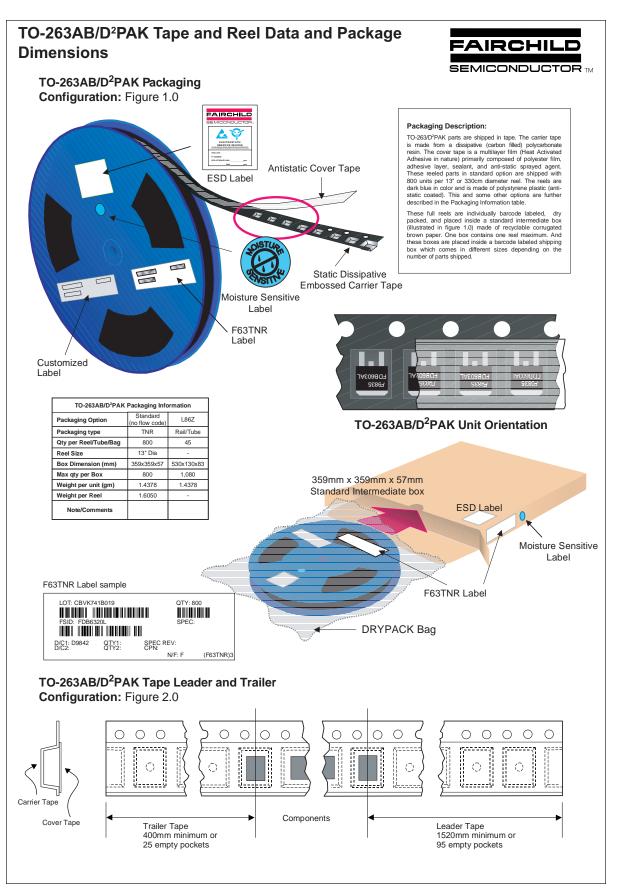




Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

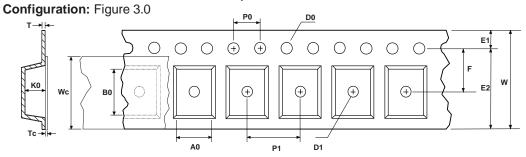
Part Weight per unit (gram): 1.4378





## TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions, continued

### TO-263AB/D<sup>2</sup>PAK Embossed Carrier Tape



## User Direction of Feed

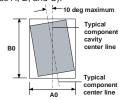
Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
TO263AB/ D <sup>2</sup> PAK (24mm)	10.60 +/-0.10	15.80 +/-0.10	24.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	22.25 min	11.50 +/-0.10	16.0 +/-0.1	4.0 +/-0.1	4.90 +/-0.10	0.450 +/-0.150	21.0 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)

Component Rotation

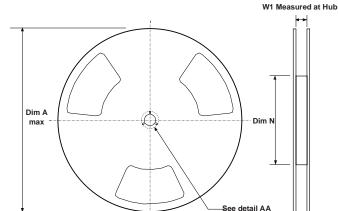


Sketch B (Top View)
Component Rotation

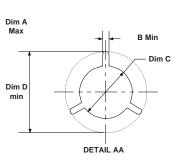


Sketch C (Top View)
Component lateral movement

# **TO-263AB/D<sup>2</sup>PAK Reel Configuration:** Figure 4.0



13" Diameter Option

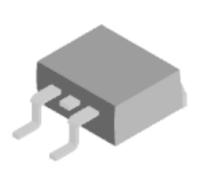


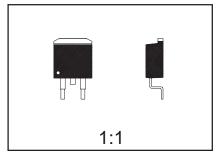
W2 max Measured at Hub

Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
24mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.961 +0.078/-0.000 24.4 +2/0	1.197 30.4	0.941 - 0.1.079 23.9 - 27.4

## TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions, continued

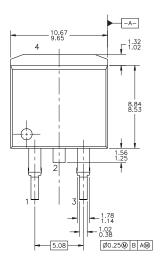
## TO-263AB/D<sup>2</sup>PAK (FS PKG Code 45)

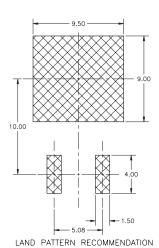


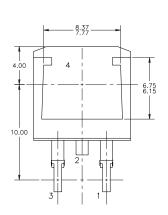


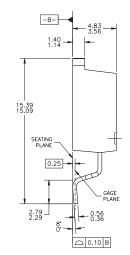
Scale 1:1 on letter size paper Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 1.4378









- NOTES: UNLESS OTHERWISE SPECIFIED

  A) ALL DIMENSIONS ARE IN MILLIMETERS.
  B) STANDARD LEAD FINISH:
  200 MICROINCHES / 5.08 MICROMETERS MIN.
  LEAD/TIN 15/85 ON OLIN 194 COPPER OR
  EQUIVALENT.
  C) MAXIMUM YERTICAL BURR ON HEATSINK NOT
  TO EXCEED 0.003 INCH / 0.05mm.
  D) NO PACKAGE CHIPS, CRACKS OR SURFACE
  IDENTIFICATION ALLOWED AFTER FORMING.
  E) REFERENCE JEDEC, TO—265, ISSUE C,
  VARIATION AB, DATED 2/92.

#### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

FACT™ QFET™ FACT Quiet Series™ QS™

FAST<sup>®</sup> Quiet Series<sup>™</sup> SuperSOT<sup>™</sup>-3 GTO<sup>™</sup> SuperSOT<sup>™</sup>-6

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

#### PRODUCT STATUS DEFINITIONS

#### **Definition of Terms**

Datasheet Identification	Product Status	Definition			
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.			
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.			
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.			
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.			