FAIRCHILD SEMICONDUCTOR™

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FST16211
24-Bit Bus Switch

General Description

The Fairchild Switch FST16211 provides 24-bits of high-speed CMOS TTL-compatible bus switching. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as a 12-bit or 24-bit bus switch. When $\overline{OE}_1$ is LOW, the switch is ON and Port 1A is connected to Port 1B. When $\overline{OE}_2$ is LOW, Port 2A is connected to Port 2B. When $\overline{OE}_{1/2}$ is HIGH, a high impedance state exists between the A and B Ports.

Features

- 4Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level
- Also packaged in plastic Fine Pitch Ball Grid Array (FBGA)

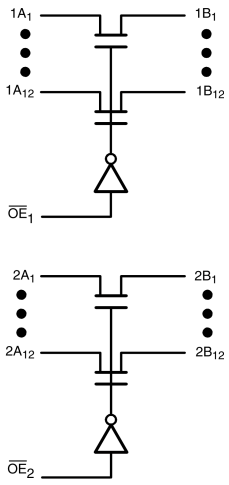
Ordering Code:

Order Number	Package Number	Package Description
FST16211GX (Note 1)	BGA54A Preliminary	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-195, 5.5mm Wide [TAPE and REEL]
FST16211MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
FST16211MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Note 1: BGA package available in Tape and Reel only.

Logic Diagram



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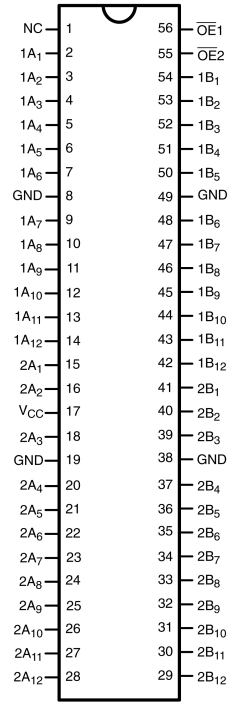
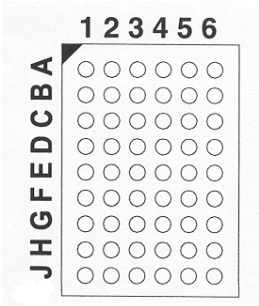
Connection Diagrams

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



TOP VIEW

Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B

FBGA Pin Assignments

	1	2	3	4	5	6
A	$1A_2$	$1A_1$	NC	OE_2	$1B_1$	$1B_2$
B	$1A_4$	$1A_3$	$1A_7$	OE_1	$1B_3$	$1B_4$
C	$1A_6$	$1A_5$	GND	$1B_7$	$1B_5$	$1B_6$
D	$1A_{10}$	$1A_9$	$1A_8$	$1B_8$	$1B_9$	$1B_{10}$
E	$1A_{12}$	$1A_{11}$	$2A_1$	$2B_1$	$1B_{11}$	$1B_{12}$
F	$2A_4$	$2A_3$	$2A_2$	$2B_2$	$2B_3$	$2B_4$
G	$2A_6$	$2A_5$	V_{CC}	GND	$2B_5$	$2B_6$
H	$2A_8$	$2A_7$	$2A_{11}$	$2B_{11}$	$2B_7$	$2B_8$
J	$2A_{10}$	$2A_9$	$2A_{12}$	$2B_{12}$	$2B_9$	$2B_{10}$

Truth Table

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S) (Note 3)	−0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 4)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 5)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	-40 °C to +85 °C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: V_S is the voltage observed/applied at either A or B Ports across the switch.

Note 4: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 5: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 6)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ A, B ≤ V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 7)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	12	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 6: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 7: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\ °C$ to $+85\ °C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 – 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 8)		0.25		0.25	ns	V_I = OPEN	Figures 1, 2
t_{PZH}, t_{PZL}	Output Enable Time	1.5	6.0		6.5	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figures 1, 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.5	7.0		7.2	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figures 1, 2

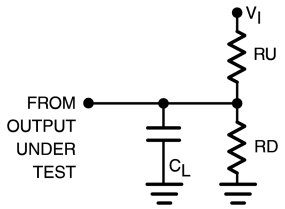
Note 8: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 9)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	6		pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 9: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

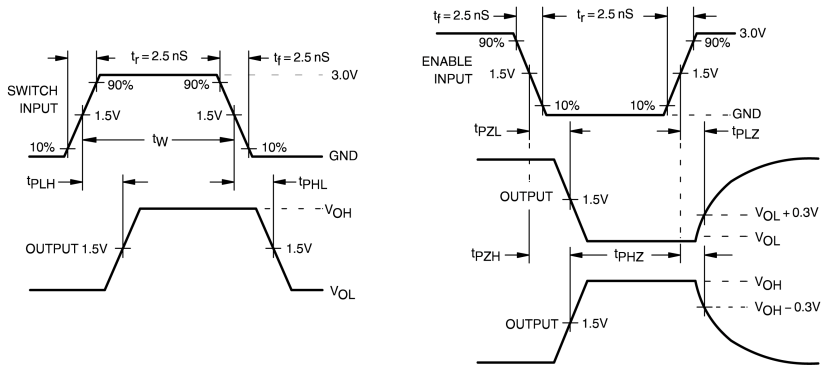
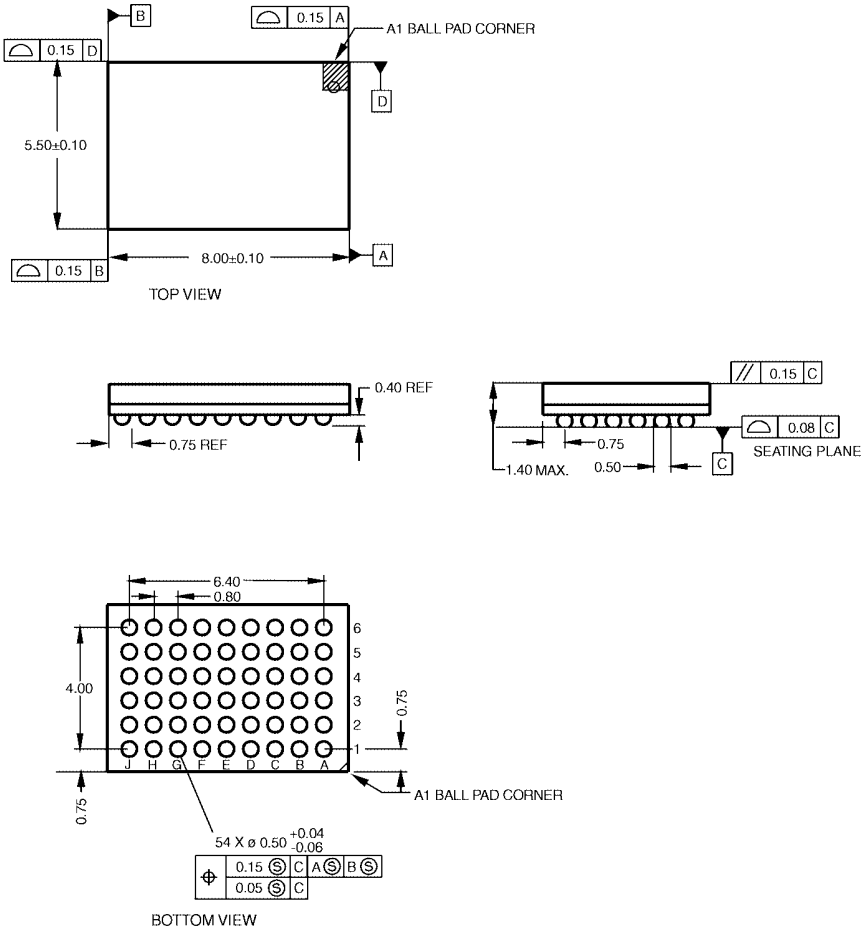


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

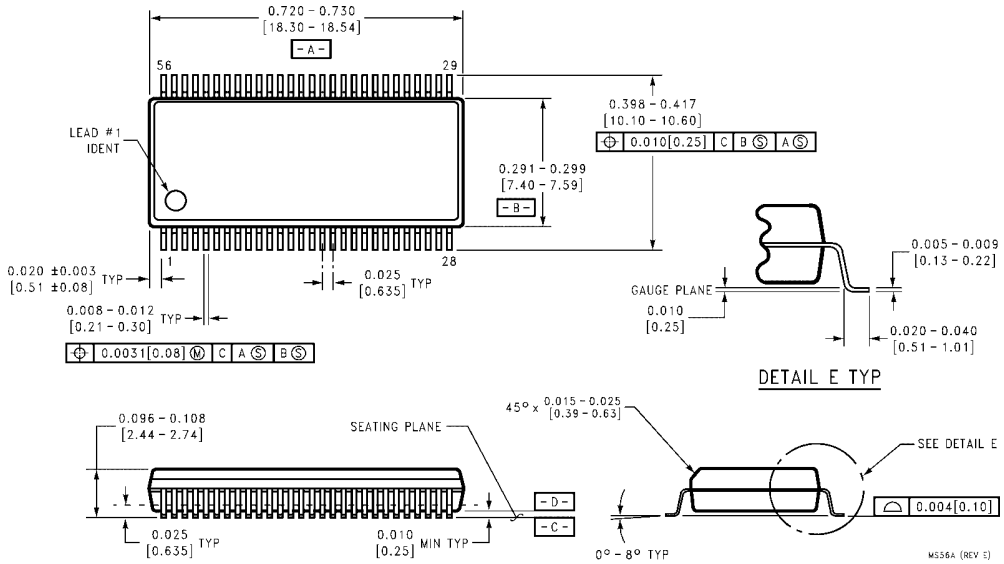


NOTES:
A. CONFORMS TO JEDEC REGISTRATION OUTLINE MO-195/B.
B. DIMENSIONS ARE IN MILLIMETERS.
C. PIN # 1 CORNER I.D. IS IDENTIFIED BY LASER MARKED DOT AT THE CORNER.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994.
E. LANDPATTERN RECOMMENDATION: .35MM DIA PADS
SOLDERMASK OPENING: .45MM CONCENTRIC TO PADS.

BGA54ARevA

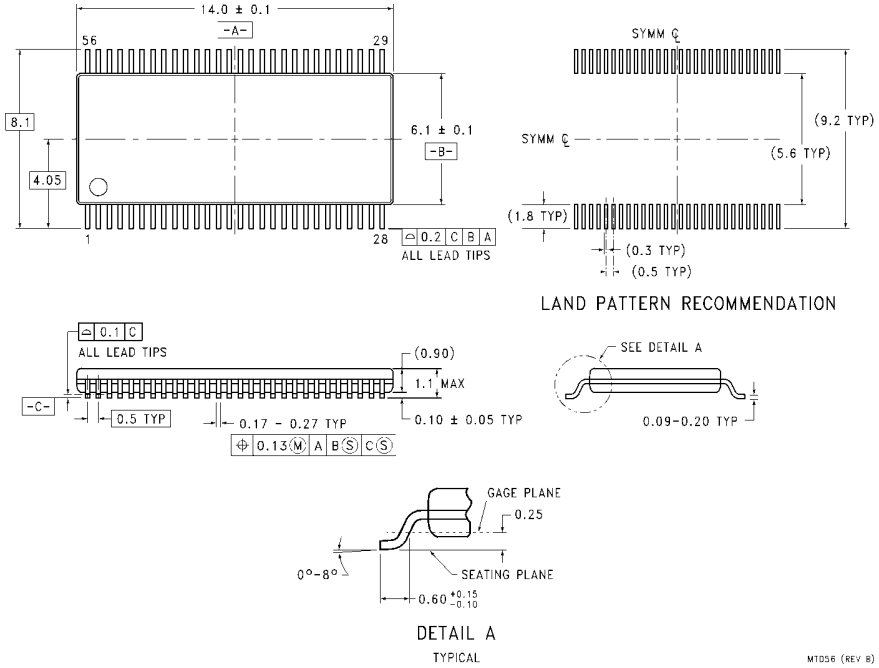
54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-195, 5.5mm Wide
Package Number BGA54A
Preliminary

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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