FAIRCHILD SEMICONDUCTOR™

August 1999
Revised April 2000

FSTU3257
Quad 2:1 Multiplexer/Demultiplexer Bus Switch with −2V Undershoot Protection

General Description

The Fairchild Switch FSTU3257 is a quad 2:1 high-speed CMOS TTL-compatible multiplexer/demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When $\overline{OE}$ is LOW, the select pin connects the A Port to the selected B Port output. The A and B Ports are "undershoot hardened" with UHC™ protection to support an extended range of 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit UHC senses undershoot at the I/O and responds by preventing voltage differentials from developing and turning on the switch. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

- Undershoot hardened to −2V (A and B Ports)
- Soft enable turn-on to minimize bus to bus charge sharing during enable
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.
- See Applications Note AN-5008 for details

Ordering Code:

Order Number	Package Number	Package Description
FSTU3257M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
FSTU3257QSC	MQA16	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FSTU3257MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

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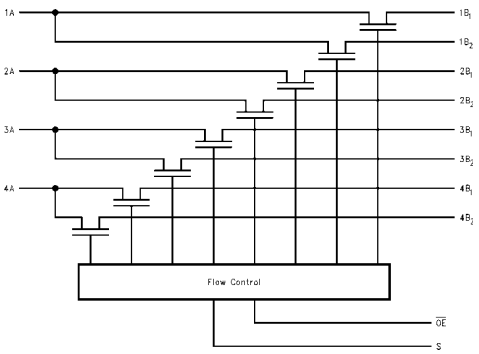
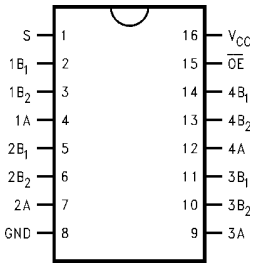
Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}$	Bus Switch Enable
S	Select Input
A	Bus A
B_1–B_2	Bus B

Truth Table

S	$\overline{OE}$	Function
X	H	Disconnect
L	L	$A = B_1$
H	L	$A = B_2$

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S) (Note 2)	−2.0V to +7.0V
DC Input Control Pin Voltage (V_{IN})(Note 3)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−50mA
DC Output (I_{OUT})	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 4)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	−40 °C to +85 °C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 2: V_S is the voltage observed/applied at either the A or B Ports across the switch.

Note 3: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 4: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance (Note 6)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
		4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	15	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND
V_{IKU}	Voltage Undershoot	5.5			−2.0	V	0.0 mA ≥ I_{IN} ≥ −50 mA $\overline{OE}$ = 5.5V

Note 5: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 6: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50pF$, RU = RD = 500Ω				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 7)		0.25		0.25	ns	V_I = OPEN	Figures 2, 3
	Prop Delay, Select to Bus A	7.0	30.0		35.0			
t_{PZH}, t_{PZL}	Output Enable Time, Select to Bus B	7.0	30.0		35.0	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figures 2, 3
	Output Enable Time, $\overline{OE}$ to Bus A, B	7.0	30.0		35.0			
t_{PHZ}, t_{PLZ}	Output Disable Time, Select to Bus B	1.5	8.4		9.8	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figures 2, 3
	Output Disable Time, Output Enable Time, $\overline{OE}$ to Bus A, B	1.5	8.8		9.8			

Note 7: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 8)

Symbol		Parameter	Typ	Max	Units	Conditions
C_{IN}		Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	A Port	Input/Output Capacitance	7.5		pF	V_{CC}, $\overline{OE}$ = 5.0V
	B Port		5.5		pF	
$C_{I/O}$ ON State		Input/Output Capacitance ON State (A or B Port)	14		pF	V_{CC} = 5.0V Switch ON

Note 8: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

Undershoot Characteristic (Note 9)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OUTU}	Output Voltage During Undershoot	2.5	V_{OH} − 0.3		V	Figure 1

Note 9: This is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

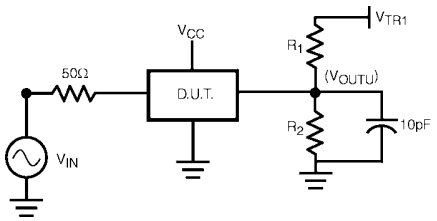
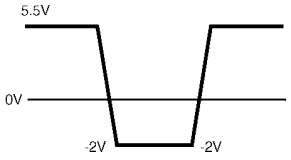


FIGURE 1.

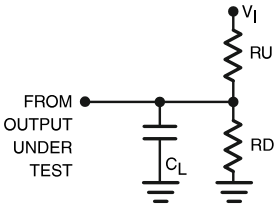
Device Test Conditions

Parameter	Value	Units
V_{IN}	See Waveform	V
R_1 - R_2	100K	Ω
V_{TRI}	11.0	V
V_{CC}	5.5	V

Transient Input Voltage (V_{IN}) Waveform



AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 nS

FIGURE 2. AC Test Circuit

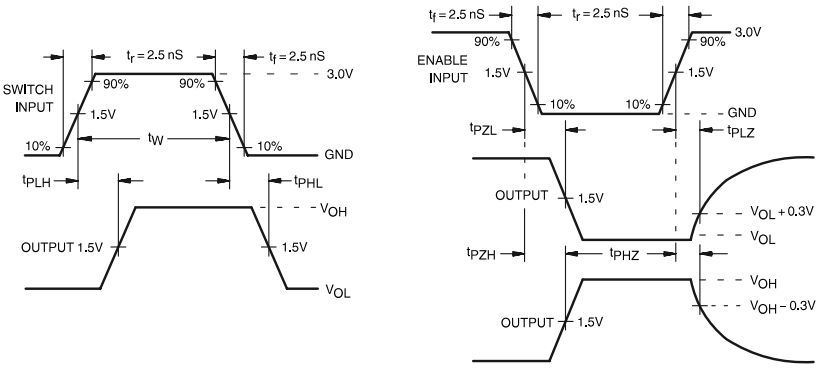
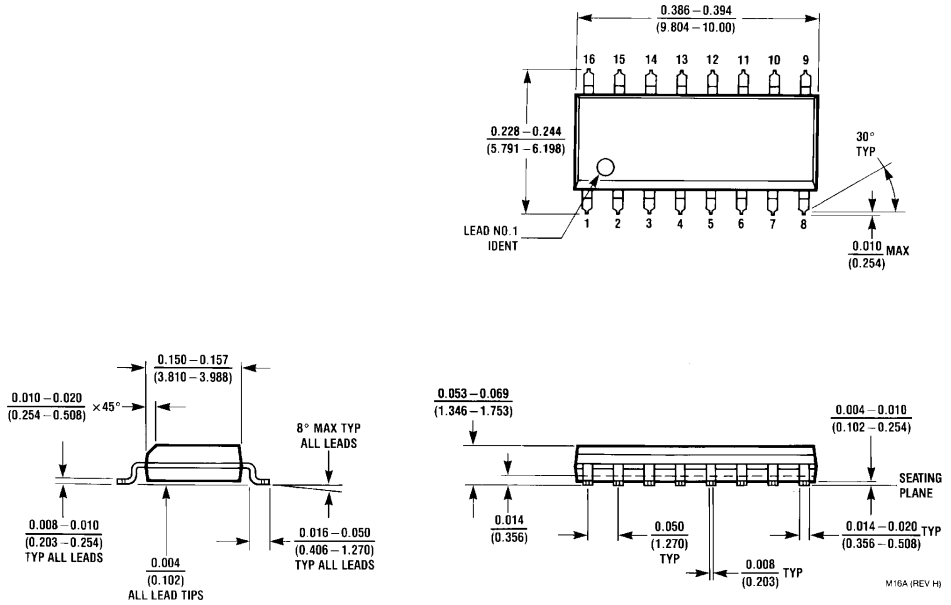
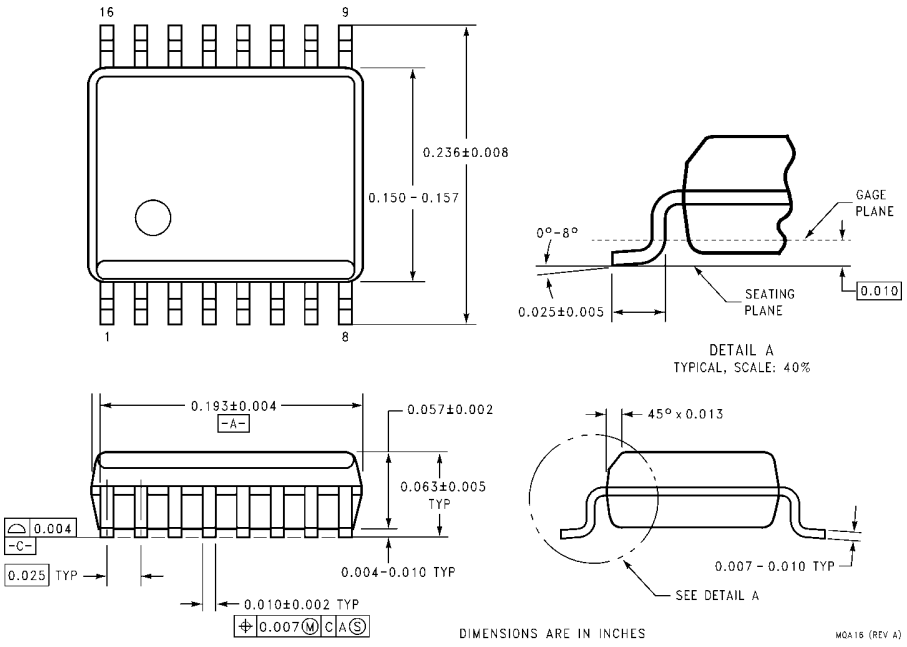


FIGURE 3. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

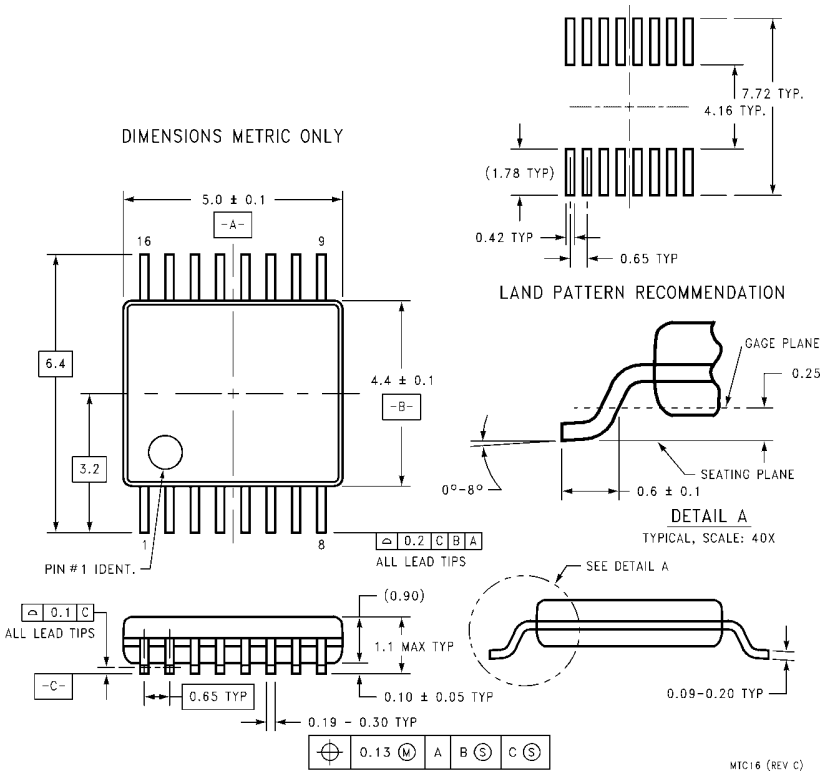


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A



16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
Package Number MQA16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.