



June 1997
Revised October 1998

GTLP16616 17-Bit TTL/GTLP Bus Transceiver with Buffered Clock

GTLP16616 17-Bit TTL/GTLP Bus Transceiver with Buffered Clock

General Description

The GTLP16616 is a 17-bit registered bus transceiver that provides TTL to GTLP signal level translation. It allows for transparent, latched and clocked modes of data flow and provides a buffered GTLP (CLKOUT) clock output from the TTL CLKAB. The device provides a high speed interface between cards operating at TTL logic levels and a backplane operating at GTLP logic levels. High speed backplane operation is a direct result of GTLP's reduced output swing (<1V), reduced input threshold levels and output edge rate control. The edge rate control minimizes bus settling time. GTLP is a Fairchild Semiconductor derivative of the Gunning Transceiver logic (GTL) JEDEC standard JESD8-3.

Fairchild's GTLP has internal edge-rate control and is process, voltage, and temperature (PVT) compensated. Its function is similar to BTL and GTL but with different output levels and receiver threshold. GTLP output LOW level is typically less than 0.5V, the output level HIGH is 1.5V and the receiver threshold is 1.0V.

Features

- Bidirectional interface between GTLP and TTL logic levels
- Edge Rate Control to minimize noise on the GTLP port
- Power up/down/off high impedance for live insertion
- External V_{REF} pin for receiver threshold
- CMOS technology for low power dissipation
- 5 V tolerant inputs and outputs on the A-Port
- Bus-hold data inputs on the A-Port eliminates the need for external pull-up resistors on unused inputs.
- TTL compatible driver and control inputs
- Flow through pinout optimizes PCB layout
- Open drain on GTLP to support wired-or connection
- A-port source/sink -32 mA/+32 mA
- D-type flip-flop, latch and transparent data paths
- GTLP Buffered CLKAB signal available (CLKOUT)
- Recommended Operating Temperature -40°C to 85°C

Ordering Code:

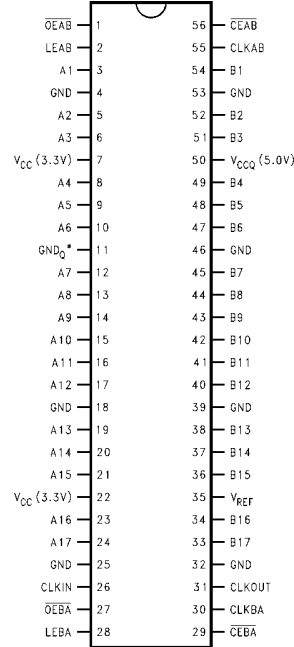
Order Number	Package Number	Package Description
GTLP16616MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118 0.300" Wide
GTLP16616MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Pin Descriptions

Pin Names	Description
\overline{OEAB}	A-to-B Output Enable (Active LOW)
\overline{OEBA}	B-to-A Output Enable (Active LOW)
\overline{CEAB}	A-to-B Clock Enable (Active LOW)
\overline{CEBA}	B-to-A Clock Enable (Active LOW)
LEAB	A-to-B Latch Enable (Transparent HIGH)
LEBA	B-to-A Latch Enable (Transparent HIGH)
V_{REF}	GTLP Reference Voltage
CLKAB	A-to-B Clock
CLKBA	B-to-A Clock
A1-A17	A-to-B Data Inputs or B-to-A 3-STATE Outputs
B1-B17	B-to-A Data Inputs or A-to-B Open Drain Outputs
CLKIN	B-to-A Buffered Clock Output
CLKOUT	GTLP Buffered Clock Output of CLKAB

Connection Diagram



Functional Description

The GTLP16616 is a 17 bit registered transceiver containing D-type flip-flop, latch and transparent modes of operation for the data path and a GTLP translation of the CLKAB signal (CLKOUT). Data flow in each direction is controlled by the clock enables (\overline{CEAB} and \overline{CEBA}), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA) and output enables (\overline{OEAB} and \overline{OEBA}). The clock enables (\overline{CEAB} and \overline{CEBA}) enable all 17 bits. The output enables (\overline{OEAB} and \overline{OEBA}) control both the 17 bits of data and the CLKOUT/CLKIN buffered clock path.

For A-to-B data flow, when \overline{CEAB} is LOW, the device operates on the LOW-to-HIGH transition of CLKAB for the flip-flop and on the HIGH-to-LOW transition of LEAB for the latch path. That is, if \overline{CEAB} is LOW and LEAB is LOW the A data is latched regardless as to the state of CLKAB (HIGH or LOW) and if LEAB is HIGH the device is in transparent mode. When \overline{OEAB} is LOW the outputs are active. When \overline{OEAB} is HIGH the outputs are HIGH impedance. The data flow of B-to-A is similar except that \overline{CEBA} , \overline{OEBA} , LEBA and CLKBA are used.

Truth Table

(Note 1)

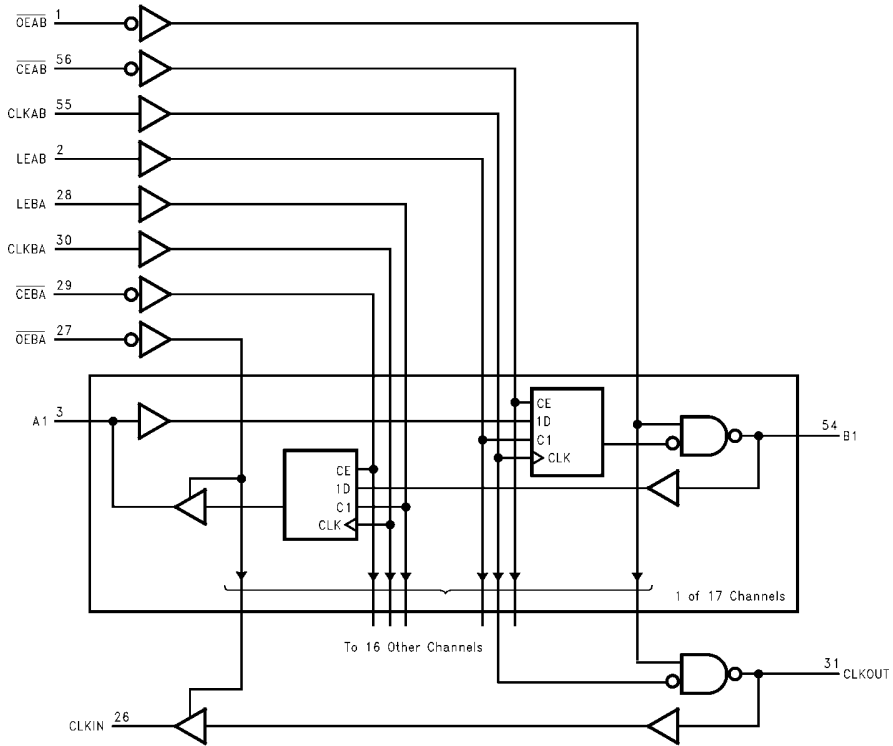
Inputs					Output B	Mode
\overline{CEAB}	\overline{OEAB}	LEAB	CLKAB	A		
X	H	X	X	X	Z	Latched storage
L	L	L	H or L	X	B_0 (Note 2)	of A data
L	L	L	H or L	X	B_0 (Note 3)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0 (Note 3)	Clock inhibit

Note 1: A-to-B data flow is shown. B-to-A data flow is similar but uses \overline{OEBA} , LEBA, CLKBA, and \overline{CEBA} .

Note 2: Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH prior to LEAB going LOW.

Note 3: Output level before the indicated steady-state input conditions were established.

Logic Diagram



Absolute Maximum Ratings (Note 4)		Recommended Operating Conditions (Note 6)	
Supply Voltage (V_{CC})	-0.5V to +7.0V	Supply Voltage V_{CC}	
DC Input Voltage (V_I)	-0.5V to +7.0V	V_{CC}	3.15V to 3.45V
DC Output Voltage (V_O)		V_{CCQ}	4.75V to 5.25V
Outputs 3-STATE	-0.5V to +7.0V	Bus Termination Voltage (V_{TT}) GTLP	1.35V to 1.65V
Outputs Active (Note 5)	-0.5V to $V_{CC} + 0.5V$	Input Voltage (V_I)	
DC Output Sink Current into A-Port I_{OL}	64 mA	on A-Port and Control Pins	0.0V to 5.5V
DC Output Source Current from A-Port I_{OH}	-64 mA	HIGH Level Output Current (I_{OH})	
DC Output Sink Current into B-Port in the LOW State, I_{OL}	80 mA	A-Port	-32 mA
DC Input Diode Current (I_{IK})		LOW Level Output Current (I_{OL})	
$V_I < 0V$	-50 mA	A-Port	+32 mA
DC Output Diode Current (I_{OK})		B-Port	+34 mA
$V_O < 0V$	-50 mA	Operating Temperature (T_A)	-40°C to +85°C
$V_O > V_{CC}$	+50 mA	Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.	
ESD Rating	>2000V	Note 5: I_O Absolute Maximum Rating must be observed.	
Storage Temperature (T_{STG})	-65°C to +150°C	Note 6: Unused inputs must be held high or low.	

DC Electrical Characteristics								
Over Recommended Operating Free-Air Temperature Range, $V_{REF} = 1.0V$ (unless otherwise noted).								
Symbol		Test Conditions		Min	Typ (Note 7)	Max	Units	
V_{IH}	B-Port			$V_{REF} + 0.1$		V_{TT}	V	
	Others			2.0			V	
V_{IL}	B-Port			0.0		$V_{REF} - 0.1$	V	
	Others					0.8	V	
V_{REF}	GTL				1.0		V	
	GTL				0.8		V	
V_{IK}		$V_{CC} = 3.15V,$ $V_{CCQ} = 4.75V$	$I_I = -18\text{ mA}$			-1.2	V	
V_{OH}	A-Port	$V_{CC}, V_{CCQ} = \text{Min to Max (Note 8)}$		$I_{OH} = -100\ \mu A$	$V_{CC} - 0.2$		V	
		$V_{CC} = 3.15V$		$I_{OH} = -8\text{ mA}$	2.4			
		$V_{CCQ} = 4.75V$		$I_{OH} = -32\text{ mA}$	2.0			
V_{OL}	A-Port	$V_{CC}, V_{CCQ} = \text{Min to Max (Note 8)}$		$I_{OL} = 100\ \mu A$		0.2	V	
		$V_{CC} = 3.15V$		$I_{OL} = 32\text{ mA}$		0.5		
		$V_{CCQ} = 4.75V$						
I_I	B-Port	$V_{CC} = 3.15V, V_{CCQ} = 4.75V$		$I_{OL} = 34\text{ mA}$		0.65	V	
	Control Pins	$V_{CC}, V_{CCQ} = 0\text{ or Max}$		$V_I = 5.5V\text{ or }0V$		± 10	μA	
	A-Port	$V_{CC} = 3.45V$		$V_I = 5.5V$		20	μA	
		$V_{CCQ} = 5.25V$		$V_I = V_{CC}$		1		
				$V_I = 0$		-30		
B-Port	$V_{CC} = 3.45V$ $V_{CCQ} = 5.25V$		$V_I = V_{CC}$ $V_I = 0$		5 -5	μA		
I_{OFF}	A-Port and Control Pins	$V_{CC} = V_{CCQ} = 0$		$V_I\text{ or }V_O = 0\text{ to }4.5V$		100	μA	
$I_{I(\text{hold})}$	A-Port	$V_{CC} = 3.15V,$ $V_{CCQ} = 4.75V$		$V_I = 0.8V$	75		μA	
				$V_I = 2.0V$	-20			
I_{OZH}	A-Port	$V_{CC} = 3.45V,$ $V_{CCQ} = 5.25V$		$V_O = 3.45V$		1	μA	
	B-Port			$V_O = 1.5V$		5		
I_{OZL}	A-Port	$V_{CC} = 3.45V,$ $V_{CCQ} = 5.25V$		$V_O = 0$		-20	μA	
	B-Port			$V_O = 0.65V$		-10		
I_{CCQ} (V_{CCQ})	A or B	$V_{CC} = 3.45V,$		Outputs HIGH		30	mA	
	Ports	$V_{CCQ} = 5.25V,$ $I_O = 0,$ $V_I = V_{CCQ}\text{ or GND}$		Outputs LOW		30		
				Outputs Disabled		30		40
I_{CC} (V_{CC})	A or B	$V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0,$		Outputs HIGH		0	mA	
	Ports	$V_I = V_{CC}\text{ or GND}$		Outputs LOW		0		
				Outputs Disabled		0		1
ΔI_{CC} (Note 9)	A-Port and Control Pins	$V_{CC} = 3.45V,$ $V_{CC} = 5.25V,$ A or Control Inputs at $V_{CC}\text{ or GND}$		One Input at 2.7V		0	1	mA
C_{IN}	Control Pins			$V_I = V_{CCQ}\text{ or }0$		8	pF	
C_{IO}	A-Port			$V_I = V_{CCQ}\text{ or }0$		9		
C_{IO}	B-Port			$V_I = V_{CCQ}\text{ or }0$		6		

Note 7: All typical values are at $V_{CC} = 3.3V, V_{CCQ} = 5.0V,$ and $T_A = 25^\circ C$.

Note 8: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

Note 9: This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

AC Operating Requirements

Over recommended ranges of supply voltage and operating free-air temperature, $V_{REF} = 1.0V$ (unless otherwise noted).

Symbol		Min	Max	Unit
f_{CLOCK}	Max Clock Frequency	175		MHz
t_W	Pulse Duration	LEAB or LEBA HIGH	3.0	ns
		CLKAB or CLKBA HIGH or LOW	3.2	
t_S	Setup Time	A before CLKAB \uparrow	0.5	ns
		B before CLKBA \uparrow	3.1	
		A before LEAB \downarrow	1.3	
		B before LEBA \downarrow	3.7	
		\overline{CEAB} before CLKAB \uparrow	0.7	
		\overline{CEBA} before CLKBA \uparrow	1.0	
t_H	Hold Time	A after CLKAB \uparrow	1.5	ns
		B after CLKBA \uparrow	0.0	
		A after LEAB \downarrow	0.5	
		B after LEBA \downarrow	0.0	
		\overline{CEAB} after CLKAB \uparrow	1.5	
		\overline{CEBA} after CLKBA \uparrow	1.7	

AC Electrical Characteristics

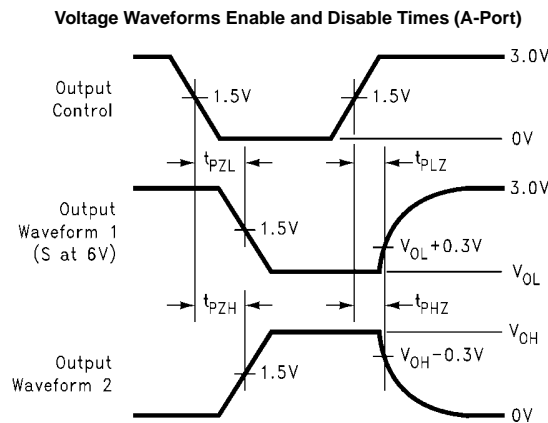
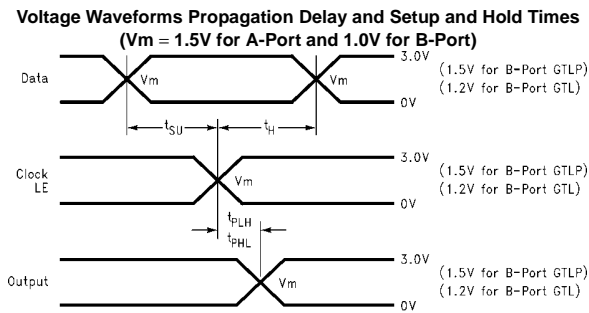
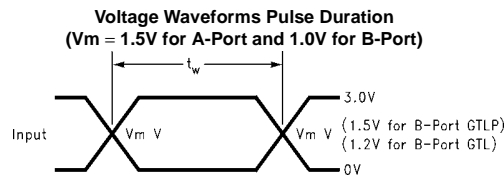
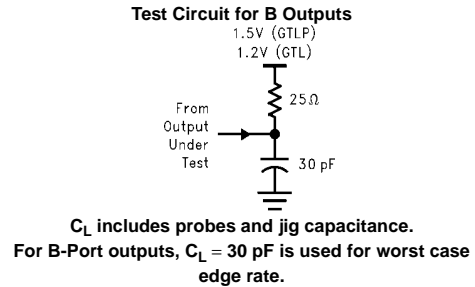
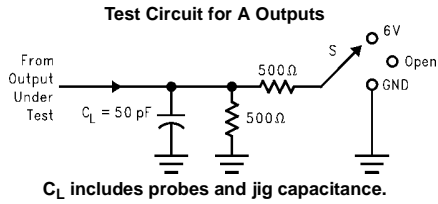
Over recommended range of supply voltage and operating free-air temperature, $V_{REF} = 1.0V$ (unless otherwise noted). $C_L = 30$ pF for B-Port and $C_L = 50$ pF for A-Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 10)	Max	Unit
t_{PLH}	A	B	1.0	4.3	6.5	ns
t_{PHL}			1.0	5.0	8.2	
t_{PLH}	LEAB	B	1.8	4.5	6.7	ns
t_{PHL}			1.5	5.3	8.7	
t_{PLH}	CLKAB	B	1.8	4.6	6.7	ns
t_{PHL}			1.5	5.4	8.7	
t_{PLH}	CLKAB	CLKOUT	3.0	6.2	10.0	ns
t_{PHL}			3.0	5.7	10.0	
t_{PLH}	\overline{OEAB}	B or CLKOUT	1.6	4.4	6.3	ns
t_{PHL}			1.3	6.1	9.8	
t_{SKEW}	B (Note 11)	CLKOUT	0		2	ns
t_{RISE}	Transition time, B outputs (20% to 80%)			2.6		ns
t_{FALL}	Transition time, B outputs (20% to 80%)			2.6		
t_{PLH}	B	A	2.0	5.6	8.2	ns
t_{PHL}			1.4	5.0	7.2	
t_{PLH}	LEBA	A	2.1	4.2	6.3	ns
t_{PHL}			1.9	3.3	5.0	
t_{PLH}	CLKBA	A	2.3	4.4	6.8	ns
t_{PHL}			2.1	3.5	5.2	
t_{PLH}	CLKOUT	CLKIN	3.0	6.0	10.0	ns
t_{PHL}			3.0	6.4	10.0	
t_{PZH}, t_{PZL}	\overline{OEBA}	A or CLKIN	1.5	5.0	6.4	ns
t_{PHZ}, t_{PLZ}			1.4	3.9	8.0	

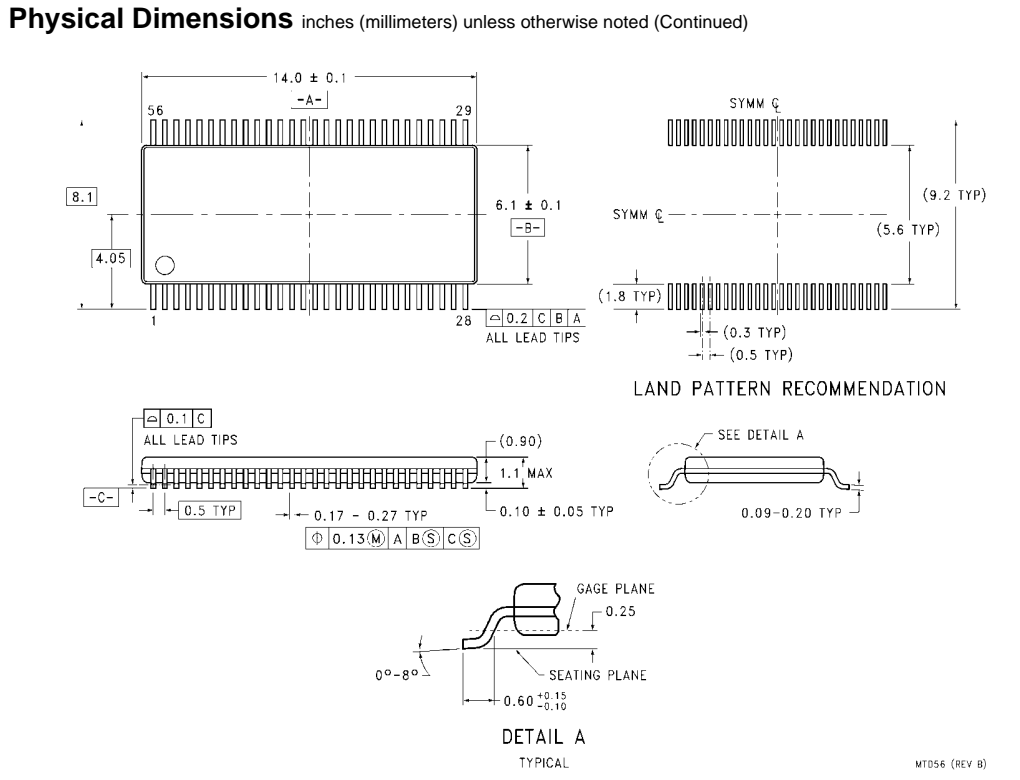
Note 10: All typical values are at $V_{CC} = 3.3V$, $V_{CCQ} = 5.0V$, and $T_A = 25^\circ C$.

Note 11: Skew is defined as the absolute value of the difference between the actual propagation delays for the CLKOUT pin and any B output transition when measured with reference to CLKAB \uparrow . This guarantees the relationship between B output data and CLKOUT such that data is coincident or ahead of CLKOUT. This specification is guaranteed but not tested.

Test Circuits and Timing Waveforms



Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. All input pulses have the following characteristics: frequency = 10 MHz, $t_r = t_f = 2 \text{ ns}$, $Z_0 = 50\Omega$. The outputs are measured one at a time with one transition per measurement.



**56-Lead Thin Shrink Small Outline Package, JEDEC MO-153, 6.1mm Wide
Package Number MTD56**

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com