FAIRCHILD SEMICONDUCTOR TM

June 1998
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GTLP6C816
GTLP-to-TTL 1:6 Clock Driver

General Description

The GTLP6C816 is a clock driver that provides TTL to GTLP signal level translation (and vice versa). The device provides a high speed interface between cards operating at TTL logic levels and a backplane operating at GTLP logic levels. High speed backplane operation is a direct result of GTLP's reduced output swing (<1V), reduced input threshold levels and output edge rate control. The edge rate control minimizes bus settling time. GTLP is a Fairchild Semiconductor derivative of the Gunning Transceiver logic (GTL) JEDEC standard JESD8-3.

Fairchild's GTLP has internal edge-rate control and is process, voltage, and temperature (PVT) compensated. Its function is similar to BTL and GTL but with different output levels and receiver threshold. GTLP output LOW level is typically less than 0.5V, the output level HIGH is 1.5V and the receiver threshold is 1.0V.

Features

- Interface between TTL and GTLP logic levels
- Edge Rate Control to minimize noise on the GTLP port
- Power up/down high impedance for live insertion
- 1:6 fanout clock driver for TTL port
- 1:2 fanout clock driver for GTLP port
- TTL compatible driver and control inputs
- Flow through pinout optimizes PCB layout
- Open drain on GTLP to support wired-or connection
- Recommended Operating Temperature –40°C to +85°C

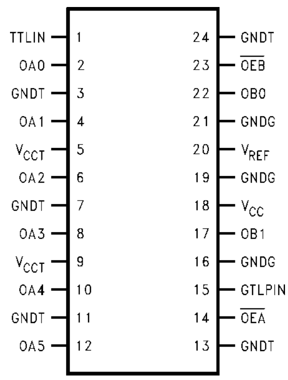
Ordering Code:

Order Number	Package Number	Package Description
GTLP6C816MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Pin Descriptions

Pin Names	Description
TTLIN, GTLPIN	Clock Inputs (TTL and GTLP respectively)
$\overline{OEB}$	Output Enable (Active LOW) GTLP Port (TTL Levels)
$\overline{OEA}$	Output Enable (Active LOW) TTL Port (TTL Levels)
V_{CCT}.GNDT	TTL Output Supplies (5V)
V_{CC}	Internal Circuitry V_{CC} (5V)
GNDG	OBn GTLP Output Grounds
V_{REF}	Voltage Reference Input
OA0–OA5	TTL Buffered Clock Outputs
OB0–OB1	GTLP Buffered Clock Outputs

Connection Diagram



Functional Description

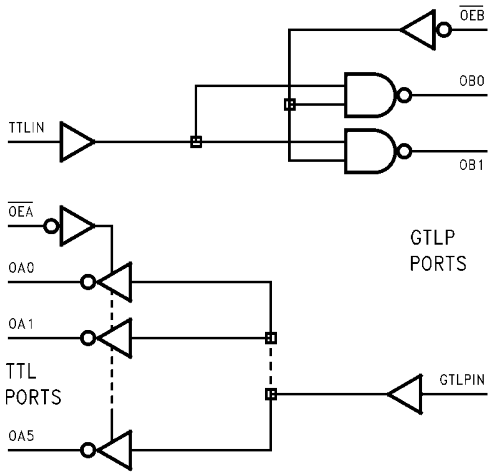
The GTLP6C816 is a clock driver providing TTL-to-GTLP clock translation, and GTLP-to-TTL clock translation in the same package. The TTL-to-GTLP direction is a 1:2 clock driver path with a single Enable pin ($\overline{OEB}$). For the GTLP-to-TTL direction the clock receiver path is a 1:6 buffer with a single Enable control ($\overline{OEA}$). Data polarity is inverting for both directions.

Truth Tables

Inputs		Outputs
TTLIN	**$\overline{OEB}$**	**OBn**
H	L	L
L	L	H
X	H	High Z

Inputs		Outputs
GTLPIN	**$\overline{OEA}$**	**OAn**
H	L	L
L	L	H
X	H	High Z

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
DC Output Voltage (V_O)	
Outputs 3-STATE	−0.5V to +7.0V
Outputs Active (Note 2)	−0.5V to +7.0V
DC Output Sink Current into	
OA-Port I_{OL}	48 mA
DC Output Source Current	
from OA-Port I_{OH}	−48 mA
DC Output Sink Current into	
OB-Port in the LOW State I_{OL}	80 mA
DC Input Diode Current (I_{IK})	
$V_I < 0V$	−50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	−50 mA
$V_O > V_{CC}$	+50 mA
ESD Rating	> 2000V
Storage Temperature (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 3)

Supply Voltage V_{CC}	4.75V to 5.25V
Bus Termination Voltage (V_{TT})	
GTLP	1.47V to 1.53V
V_{REF}	0.98V to 1.02V
Input Voltage (V_I) on INA-Port	
and Control Pins	0.0V to 5.5V
HIGH Level Output Current (I_{OH})	
OA-Port	−24 mA
LOW Level Output Current (I_{OL})	
OA-Port	+24 mA
OB-Port	+34 mA
Operating Temperature (T_A)	−40°C to +85°C

Note 1: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 2: I_o Absolute Maximum Rating must be observed.

Note 3: Unused input must be held high or low.

DC Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 1.0V (unless otherwise noted).

Symbol		Test Conditions		Min	Typ (Note 4)	Max	Units
V_{IH}	GTLPIN			V_{REF} +0.05		V_{TT}	V
	Others			2.0			
V_{IL}	GTLPIN			0.0		V_{REF} –0.05	V
	Others					0.8	
V_{REF} (Note 5)	GTLP				1.0		V
	GTL				0.8		
V_{TT} (Note 5)	GTLP				1.5		V
	GTL				1.2		
V_{IK}		V_{CC} = 4.75V	I_I = –18 mA			–1.2	V
V_{OH}	OAn-Port	V_{CC} = 4.75V	I_{OH} = –100 µA	V_{CC}–0.2			V
			I_{OH} = –18 mA	2.4			
			I_{OH} = –24 mA	2.2			
V_{OL}	OAn-Port	V_{CC} = 4.75V	I_{OL} = 100 µA			0.2	V
			I_{OL} = 18 mA			0.4	
			I_{OL} = 24 mA			0.5	
V_{OL}	OBn-Port	V_{CC} = 4.75V	I_{OL} = 100 µA			0.2	V
			I_{OL} = 34 mA			0.65	
I_I	TTLIN/ Control Pins	V_{CC} = 5.25V	V_I = 5.25V V_I = 0V			5 –5	µA
	GTLPIN	V_{CC} = 5.25V	V_I = V_{TT} V_I = 0			5 –5	µA
I_{OFF}	TTLIN	V_{CC} = 0	V_I or V_O = 0V to 5.25V			100	µA
I_{OZH}	OAn-Port	V_{CC} = 5.25V	V_O = 5.25V			5	µA
	OBn-Port		V_O = 1.5V			5	
I_{OZL}	OAn-Port	V_{CC} = 5.25V	V_O = 0			–5	µA
I_{CC}	OAn or OBn Ports	V_{CC} = 5.25V	Outputs HIGH		7	18	mA
			Outputs LOW		7	20	
		V_I = V_{CC} or GND	Outputs Disabled		7	20	
ΔI_{CC}	TTLIN	V_{CC} = 5.25V	V_I = V_{CC}–2.1			6	mA
C_{IN}	Control Pins/GTLPIN/ TTLIN		V_I = V_{CC} or 0		3.7		pF
C_{OUT}	OAn-Port		V_I = V_{CC} or 0		7		pF
	OBn-Port		V_I = V_{CC} or 0		7		

Note 4: All typical values are at V_{CC} = 5.0V and T_A = 25°C.

Note 5: GTLP V_{REF} and V_{TT} are specified to 2% tolerance since signal integrity and noise margin can be significantly degraded if these supplies are noisy. In addition, V_{TT} and R_{TERM} can be adjusted to accommodate backplane impedances other than 50Ω, within the boundaries of not exceeding the DC Absolute I_{OL} ratings. Similarly V_{REF} can be adjusted to compensate for changes in V_{TT}.

AC Electrical Characteristics

Over recommended range of supply voltage and operating free air temperature. V_{REF} = 1.0V (unless otherwise noted).

C_L = 30 pF for OBn-Port and C_L = 50 pF for OAn-Port.

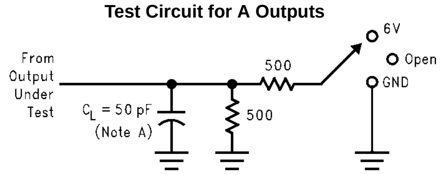
Symbol	From (Input)	To (Output)	Min	Typ (Note 6)	Max	Units
t_{PLH}	TTLIN	OBn	1.5	3.8	6.0	ns
t_{PHL}			1.5	2.8	5.0	
t_{PLH}	$\overline{OEB}$	OBn	1.5	6.4	10.5	ns
t_{PHL}			1.5	3.2	6.0	
t_{RISE}	Transition Time, OB Outputs (20% to 80%)			2.3		ns
t_{FALL}	Transition Time, OB outputs (20% to 80%)			2.3		ns
t_{RISE}	Transition Time, OA outputs (10% to 90%)			2.0		ns
t_{FALL}	Transition Time, OA outputs (10% to 90%)			2.0		ns
t_{PZH}, t_{PZL}	$\overline{OEA}$	OAn	0.5	3.6	6.5	ns
t_{PLZ}, t_{PHZ}			0.5	3.8	6.5	
t_{PLH}	GTLPIN	OAn	1.5	4.4	6.5	ns
t_{PHL}			1.5	4.0	6.0	
t_{OSHL}, t_{OSLH} (Note 7)	Common Edge Skew			0.2	1.0	ns

Note 6: All typical values are at V_{CC} = 5.0V and T_A = 25°C.

Note 7: Skew specs are given for specific worst case V_{CC} Temp. Skew values between the OBn outputs could vary on the backplane due to loading and impedance seen by the device.

Test Circuit and Timing Waveforms

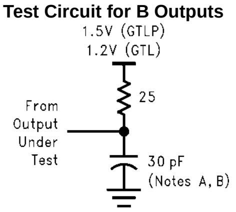
Test Circuit for A Outputs



Test	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

Note A: C_L includes probes and jig capacitance.

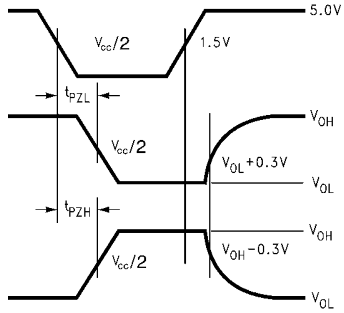
Test Circuit for B Outputs



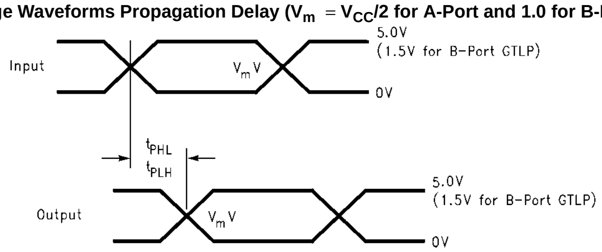
Note A: C_L includes probes and jig capacitance.

Note B: For B-Port $C_L = 30$ pF is used for worst case.

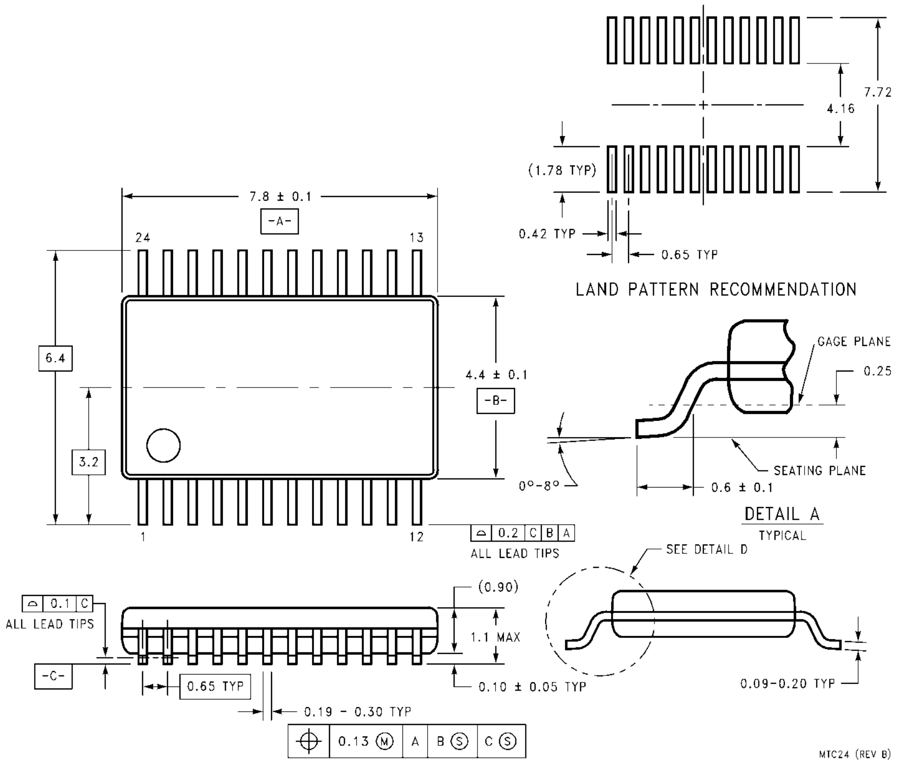
Voltage Waveforms Enable and Disable Times A-Port



Voltage Waveforms Propagation Delay ($V_m = V_{CC}/2$ for A-Port and 1.0 for B-Port)



Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

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