

MM74C86

Quad 2-Input EXCLUSIVE-OR Gate

General Description

The MM74C86 employs complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin these gates provide basic functions used in the implementation of digital integrated circuit systems. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No DC power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

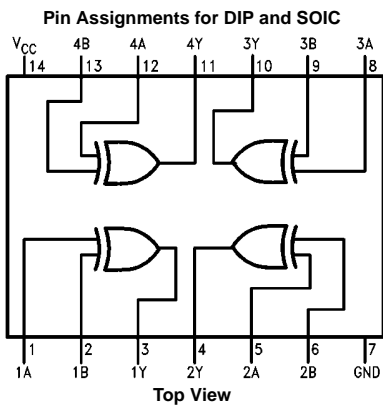
- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: $0.45 V_{CC}$ (typ.)
- Low power: TTL compatibility:
Fan out of 2 driving 74L
- Low power consumption: 10 nW/package (typ.)
- The MM74C86 follows the MM74LS86 Pinout

Ordering Code:

Order Number	Package Number	Package Description
MM74C86M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74C86N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



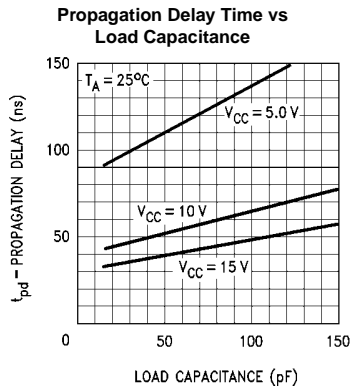
Truth Table

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

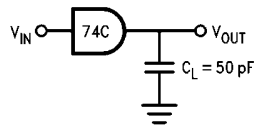
H = HIGH Level
L = LOW Level

Absolute Maximum Ratings (Note 1)		Absolute Maximum (V_{CC})	18V			
Voltage at any Pin (Note 1)	-0.3V to $V_{CC} + 0.3V$	Lead Temperature				
Operating Temperature Range	-40°C to +85°C	(Soldering, 10 seconds)	260°C			
Storage Temperature Range	-65°C to +150°C					
Power Dissipation (P_D)						
Dual-In-Line Package	700 mW					
Small Outline	500 mW					
Operating Range (V_{CC})	3.0V to 15V					
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions for actual device operation.						
DC Electrical Characteristics						
Min/max limits apply across temperature range unless otherwise noted						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$	4.5 9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V, I_O = +10 \mu A$ $V_{CC} = 10V, I_O = +10 \mu A$			0.5 1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.01	15	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V, I_O = -360 \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V, I_O = 360 \mu A$			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	8.0	16		mA
AC Electrical Characteristics (Note 2)						
$T_A = 25^\circ C, C_L = 50 \text{ pF}$, unless otherwise specified						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Time to Logical "1" or "0"	$V_{CC} = 5.0V$ $V_{CC} = 10V$		110 50	185 90	ns
C_{IN}	Input Capacitance	(Note 3)		5.0		pF
C_{PD}	Power Dissipation Capacitance	Per Gate (Note 4)		20		pF
Note 2: AC Parameters are guaranteed by DC correlated testing.						
Note 3: Capacitance is guaranteed by periodic testing.						
Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note—AN-90.						

Typical Performance Characteristics



Test Circuits and Waveforms



Delays Measured with Input $t_r, t_f = 20$ ns

FIGURE 1. AC Test Circuit

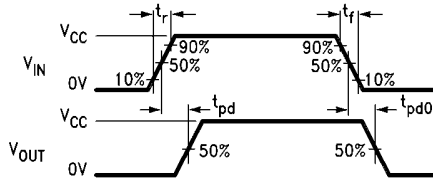
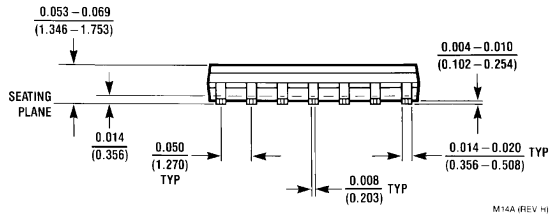
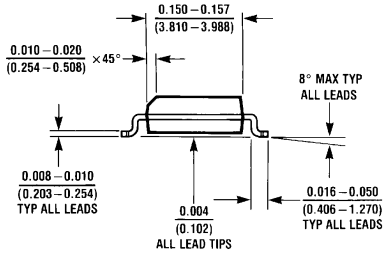
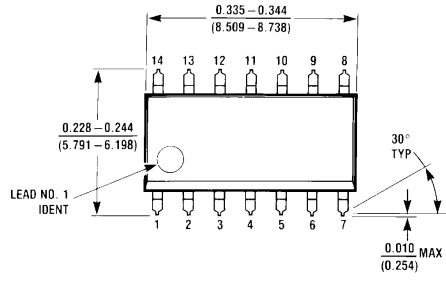


FIGURE 2. Switching Time Waveforms

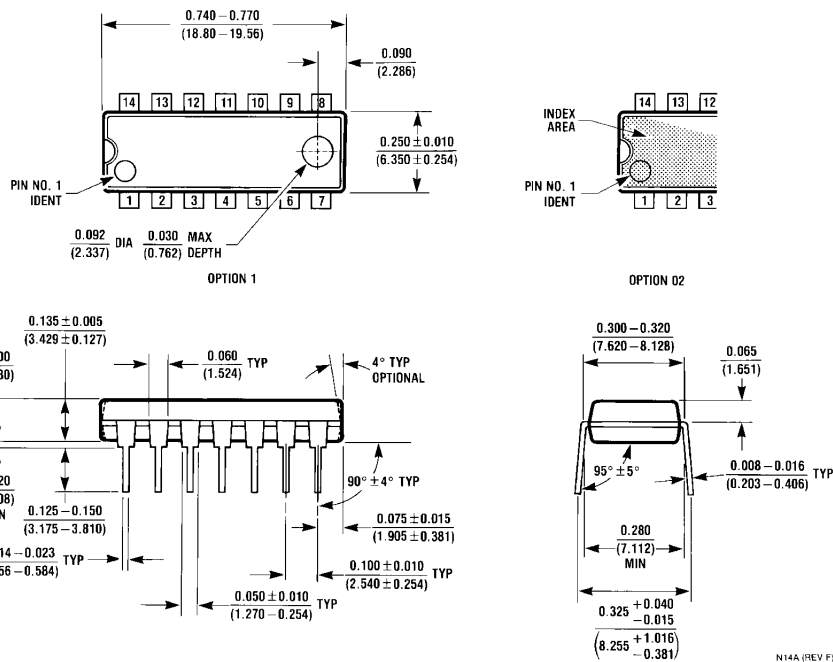
Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
Package Number M14A**

M14A (REV. H)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A**

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