

MM74HC125/MM74HC126 3-STATE Quad Buffers

General Description

The MM74HC125 and MM74HC126 are general purpose 3-STATE high speed non-inverting buffers utilizing advanced silicon-gate CMOS technology. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The MM74HC125 require the 3-STATE control input C to be taken high to put the output into the high impedance

condition, whereas the MM74HC126 require the control input to be low to put the output into high impedance.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μ A maximum
- Low quiescent current: 80 μ A maximum (74HC)
- Fanout of 15 LS-TTL loads

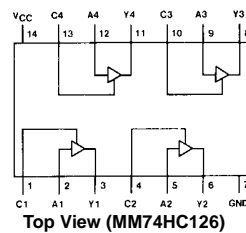
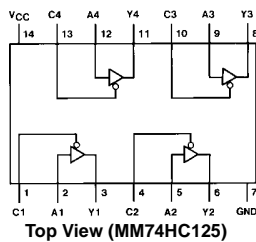
Ordering Code:

Order Number	Package Number	Package Description
MM74HC125M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
MM74HC125SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC125N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HC126M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
MM74HC126SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC126MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC126N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code. (Tape and Reel not available in N14A.)

Connection Diagrams

Pin Assignments for DIP, SOIC, SOP and TSSOP



Truth Tables

Inputs		Output
A	C	Y
H	L	H
L	L	L
X	H	Z

Inputs		Output
A	C	Y
H	H	H
L	H	L
X	L	Z

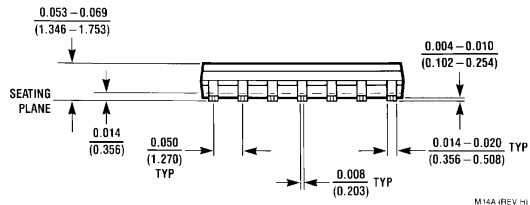
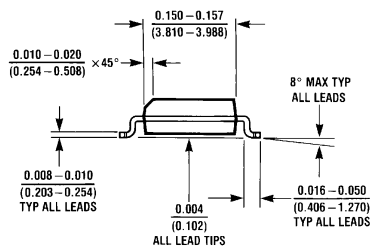
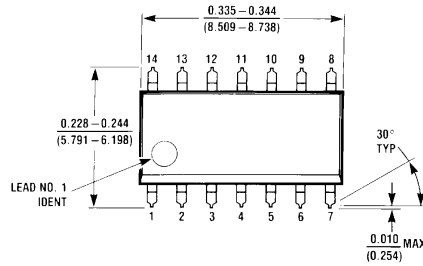
Absolute Maximum Ratings (Note 1)				Recommended Operating Conditions				
(Note 2)								
Supply Voltage (V_{CC})	-0.5 to +7.0V			Supply Voltage (V_{CC})	Min	Max	Units	
DC Input Voltage (V_{IN})	-1.5 to $V_{CC}+1.5V$			DC Input or Output Voltage	2	6	V	
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC}+0.5V$			(V_{IN}, V_{OUT})	0	V_{CC}	V	
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA			Operating Temperature Range (T_A)	-40	+85	$^{\circ}C$	
DC Output Current, per pin (I_{OUT})	± 35 mA			Input Rise or Fall Times (t_r, t_f)				
DC V_{CC} or GND Current, per pin (I_{CC})	± 70 mA			$V_{CC} = 2.0V$		1000	ns	
Storage Temperature Range (T_{STG})	-65 $^{\circ}C$ to +150 $^{\circ}C$			$V_{CC} = 4.5V$		500	ns	
Power Dissipation (P_D)				$V_{CC} = 6.0V$		400	ns	
(Note 3)	600 mW			Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.				
S.O. Package only	500 mW			Note 2: Unless otherwise specified all voltages are referenced to ground.				
Lead Temperature (T_L)				Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/ $^{\circ}C$ from 65 $^{\circ}C$ to 85 $^{\circ}C$.				
(Soldering 10 seconds)	260 $^{\circ}C$							
DC Electrical Characteristics (Note 4)								
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^{\circ}C$		$T_A = -40$ to $85^{\circ}C$	$T_A = -40$ to $125^{\circ}C$	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0$ mA $ I_{OUT} \leq 7.8$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0$ mA $ I_{OUT} \leq 7.8$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
I_{OZ}	Maximum 3-STATE Output Leakage Current	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND $C_n = \text{Disabled}$	6.0V		± 0.5	± 5	± 10	μA
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	μA
Note 4: For a power supply of 5V $\pm 10\%$ the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC}=5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.								

AC Electrical Characteristics					
$V_{CC} = 5V, T_A = 25^\circ C, C_L = 45 \text{ pF}, t_r = t_f = 6 \text{ ns}$					
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time		13	18	ns
t_{PZH}	Maximum Output Enable Time to HIGH Level	$R_L = 1 \text{ k}\Omega$	13	25	ns
t_{PHZ}	Maximum Output Disable Time from HIGH Level	$R_L = 1 \text{ k}\Omega$ $C_L = 5 \text{ pF}$	17	25	ns
t_{PZL}	Maximum Output Enable Time to LOW Level	$R_L = 1 \text{ k}\Omega$	18	25	ns
t_{PLZ}	Maximum Output Disable Time from LOW Level	$R_L = 1 \text{ k}\Omega$ $C_L = 5 \text{ pF}$	13	25	ns

AC Electrical Characteristics								
$V_{CC} = 2.0V \text{ to } 6.0V, C_L = 50 \text{ pF}, t_r = t_f = 6 \text{ ns}$ (unless otherwise specified)								
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$				Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time		2.0V	40	100	125	150	ns
			4.5V	14	20	25	30	ns
			6.0V	12	17	21	25	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	$C_L = 150 \text{ pF}$	2.0V	35	130	163	195	ns
			4.5V	14	26	33	39	ns
			6.0V	12	22	28	39	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1 \text{ k}\Omega$	2.0V	25	125	156	188	ns
			4.5V	14	25	31	38	ns
			6.0V	12	21	26	31	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1 \text{ k}\Omega$	2.0V	25	125	156	188	ns
			4.5V	14	25	31	38	ns
			6.0V	12	21	26	31	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L = 150 \text{ pF}$ $R_L = 1 \text{ k}\Omega$	2.0V	35	140	175	210	ns
			4.5V	15	28	35	42	ns
			6.0V	13	24	30	36	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L = 50 \text{ pF}$	2.0V	30	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{OUT}	Output Capacitance Outputs			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)						
		Enabled		45				pF
		Disabled		6				pF

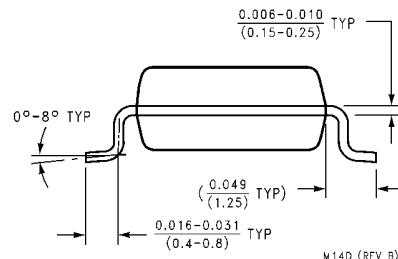
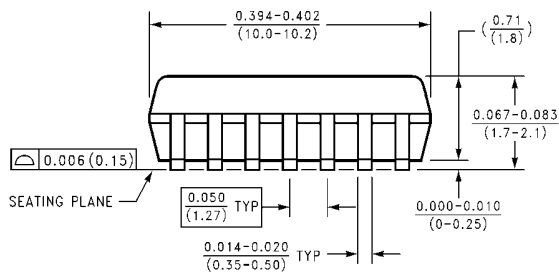
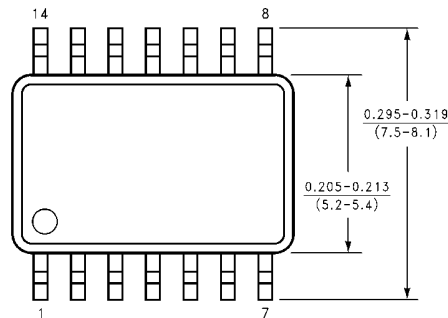
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted



M14A (REV H)

**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
Package Number M14A**

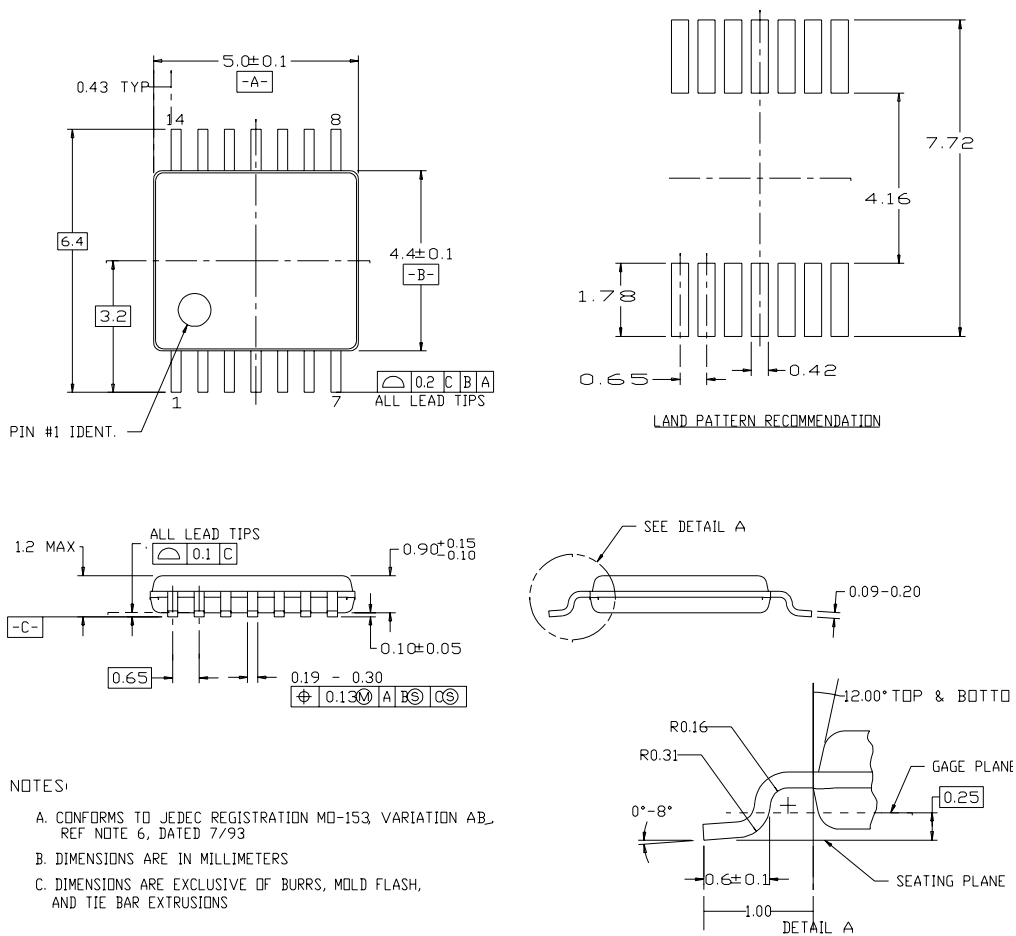


M14D (REV B)

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

14LD, TSSOP, JEDEC MO-153, 4.4MM WIDE

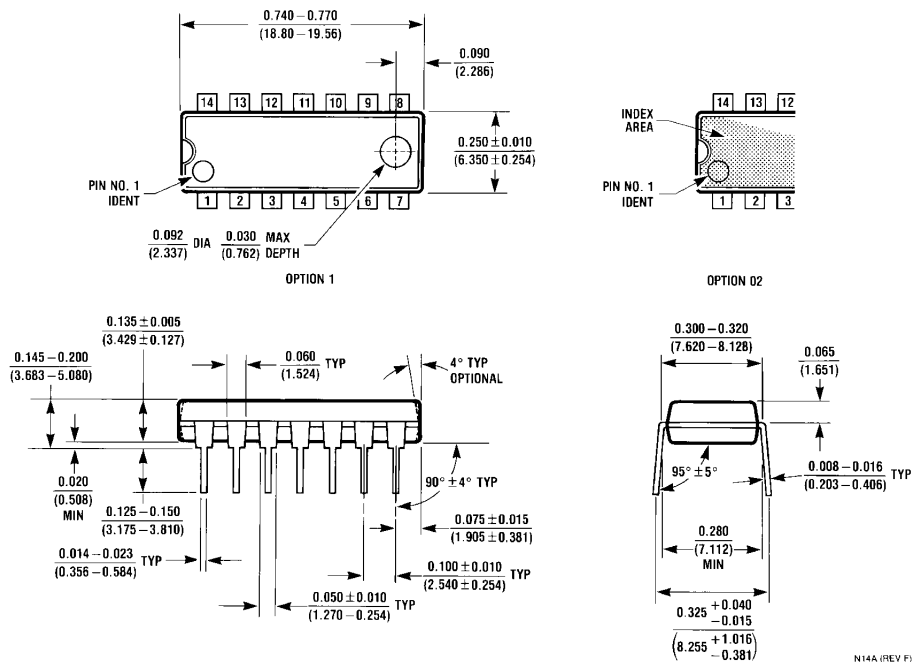


NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153 VARIATION AB, REF NOTE 6, DATED 7/93
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

**14-Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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