

MM74HC244 Octal 3-STATE Buffer

General Description

The MM74HC244 is a non-inverting buffer and has two active low enables (1G and 2G); each enable independently controls 4 buffers. This device does not have Schmitt trigger inputs.

These 3-STATE buffers utilize advanced silicon-gate CMOS technology and are general purpose high speed non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. All three devices have a fanout of 15 LS-TTL equivalent inputs.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

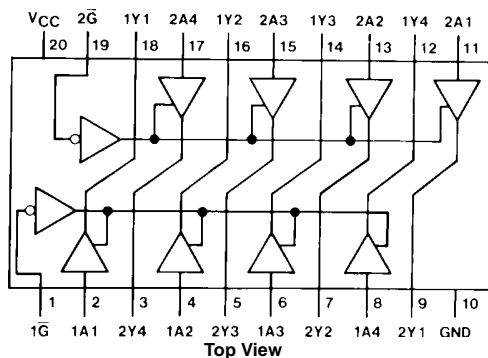
- Typical propagation delay: 14 ns
- 3-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μ A
- Output current: 6 mA

Ordering Code:

Order Number	Package Number	Package Description
MM74HC244WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC244SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC244MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC244N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

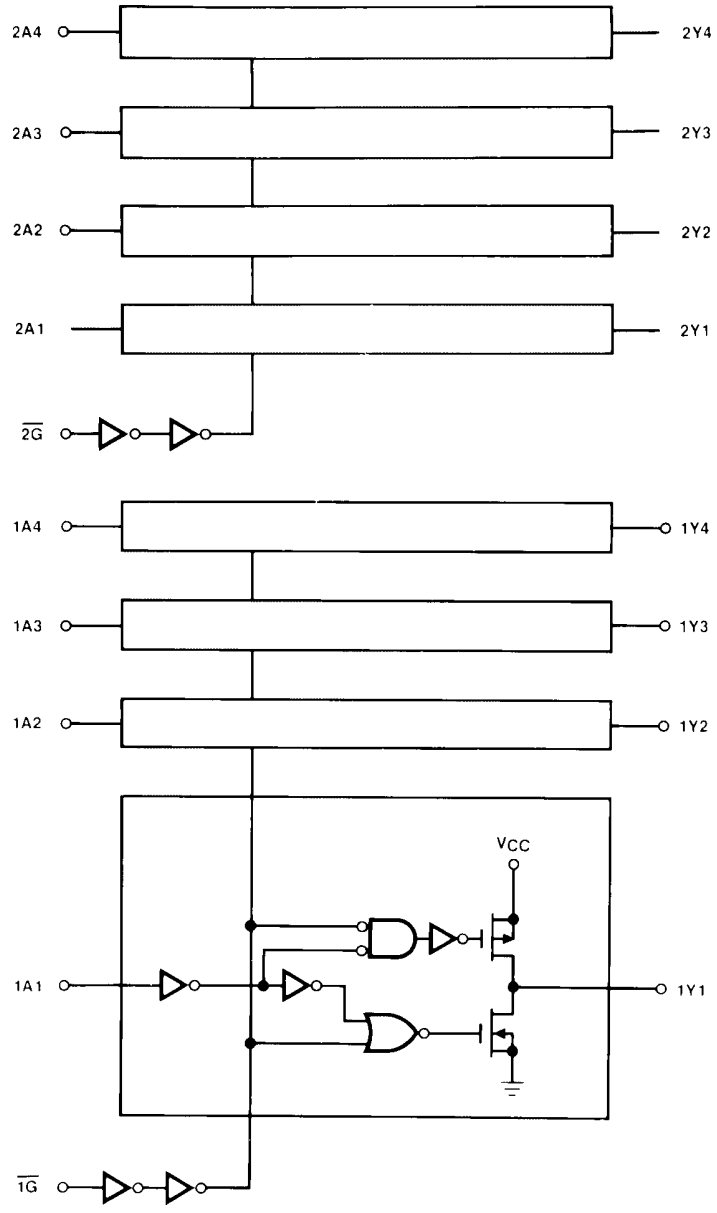


Truth Table

$\overline{1G}$	1A	1Y	$\overline{2G}$	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

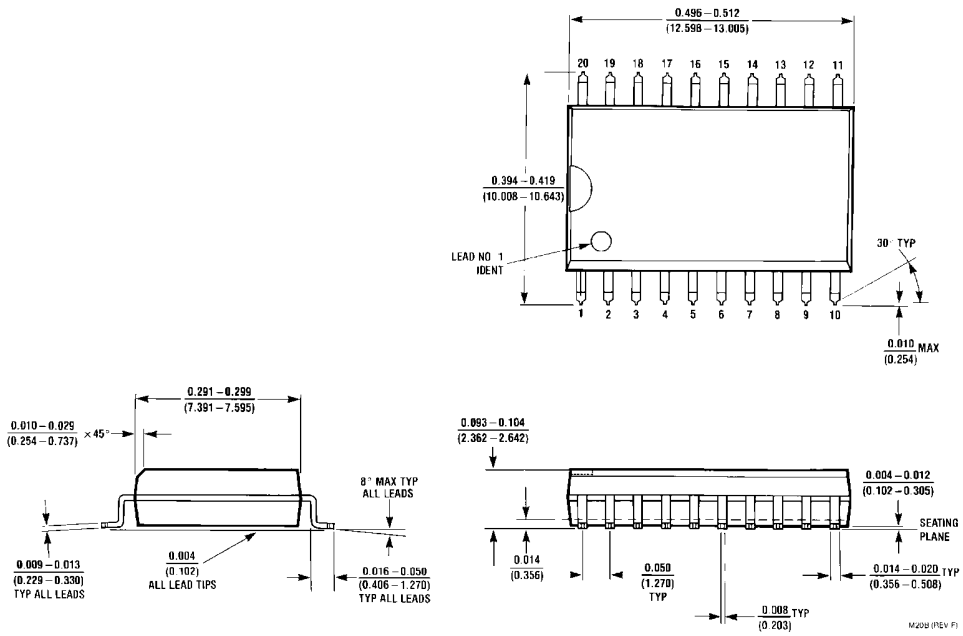
H = HIGH Level
L = LOW Level
Z = High Impedance

Logic Diagram



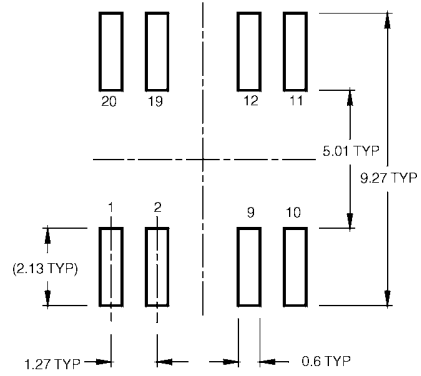
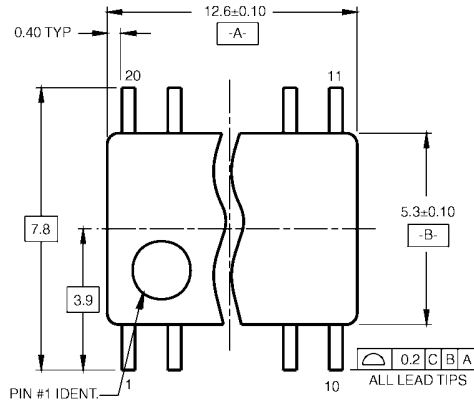
AC Electrical Characteristics								
$V_{CC} = 5V, T_A = 25^\circ C, t_r = t_f = 6 \text{ ns}$								
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 45 \text{ pF}$	14	20	ns			
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	$R_L = 1 \text{ k}\Omega$ $C_L = 45 \text{ pF}$	17	28	ns			
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Output	$R_L = 1 \text{ k}\Omega$ $C_L = 5 \text{ pF}$	15	25	ns			
AC Electrical Characteristics								
$V_{CC} = 2.0V-6.0V, C_L = 50 \text{ pF}, t_r = t_f = 6 \text{ ns}$ (unless otherwise specified)								
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		$T_A = -40 \text{ to } 85^\circ C$	$T_A = -55 \text{ to } 125^\circ C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 50 \text{ pF}$	2.0V	58	115	145	171	ns
		$C_L = 150 \text{ pF}$	2.0V	83	165	208	246	ns
		$C_L = 50 \text{ pF}$	4.5V	14	23	29	34	ns
		$C_L = 150 \text{ pF}$	4.5V	17	33	42	49	ns
		$C_L = 50 \text{ pF}$	6.0V	10	20	25	29	ns
		$C_L = 150 \text{ pF}$	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1 \text{ k}\Omega$						
		$C_L = 50 \text{ pF}$	2.0V	75	150	189	224	ns
		$C_L = 150 \text{ pF}$	2.0V	100	200	252	298	ns
		$C_L = 50 \text{ pF}$	4.5V	15	30	38	45	ns
		$C_L = 150 \text{ pF}$	4.5V	30	40	50	60	ns
		$C_L = 50 \text{ pF}$	6.0V	13	26	32	38	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1 \text{ k}\Omega$	2.0V	75	150	189	224	ns
		$C_L = 50 \text{ pF}$	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer) $\bar{G} = V_{IH}$ $\bar{G} = V_{IL}$		12 50				pF pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF
<p>Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.</p>								

Physical Dimensions inches (millimeters) unless otherwise noted

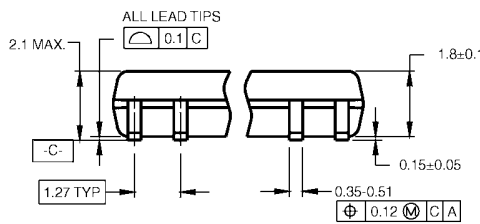


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B**

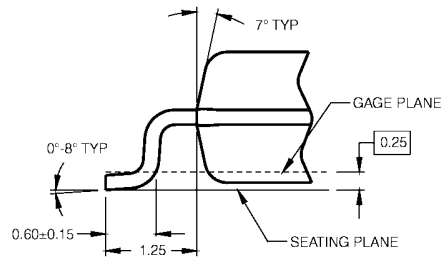
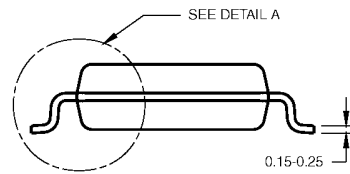
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

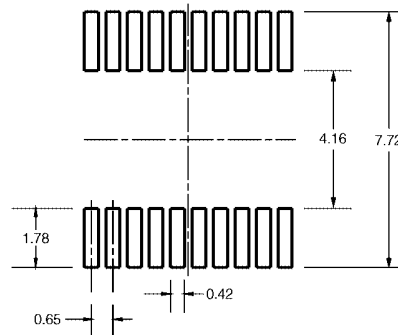
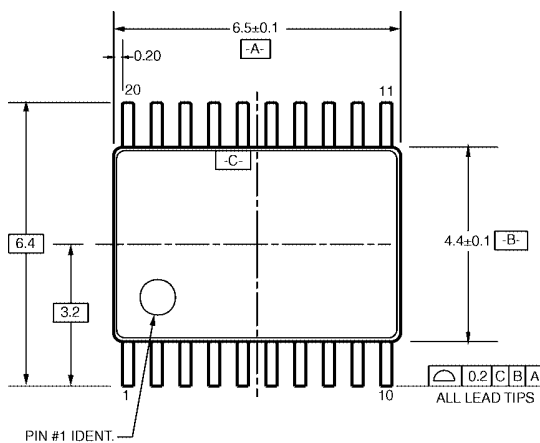
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

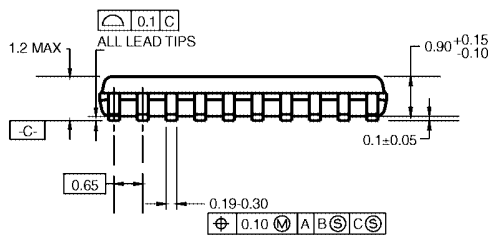
M20DRRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

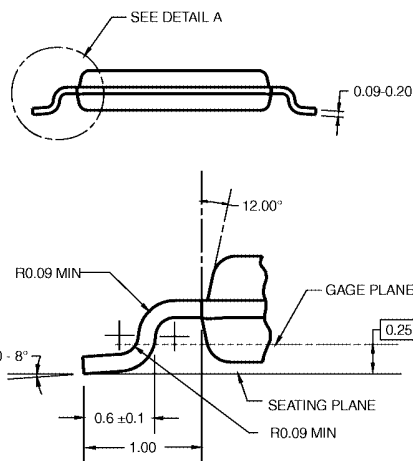


DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1



DETAIL A

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

