

MM74HC595 8-Bit Shift Registers with Output Latches

General Description

The MM74HC595 high speed shift register utilizes advanced silicon-gate CMOS technology. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 3-STATE outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

The 74HC logic family is speed, function, and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low quiescent current: 80 μ A maximum (74HC Series)
- Low input current: 1 μ A maximum
- 8-bit serial-in, parallel-out shift register with storage
- Wide operating voltage range: 2V–6V
- Cascadable
- Shift register has direct clear
- Guaranteed shift frequency: DC to 30 MHz

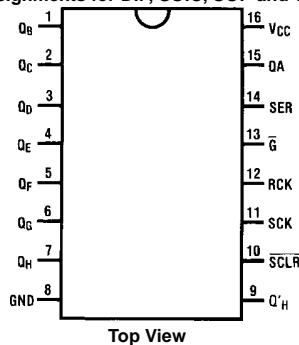
Ordering Code:

Order Number	Package Number	Package Description
MM74HC595M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC595WMM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC595SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC595MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC595N	N16E	16-Lead Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP

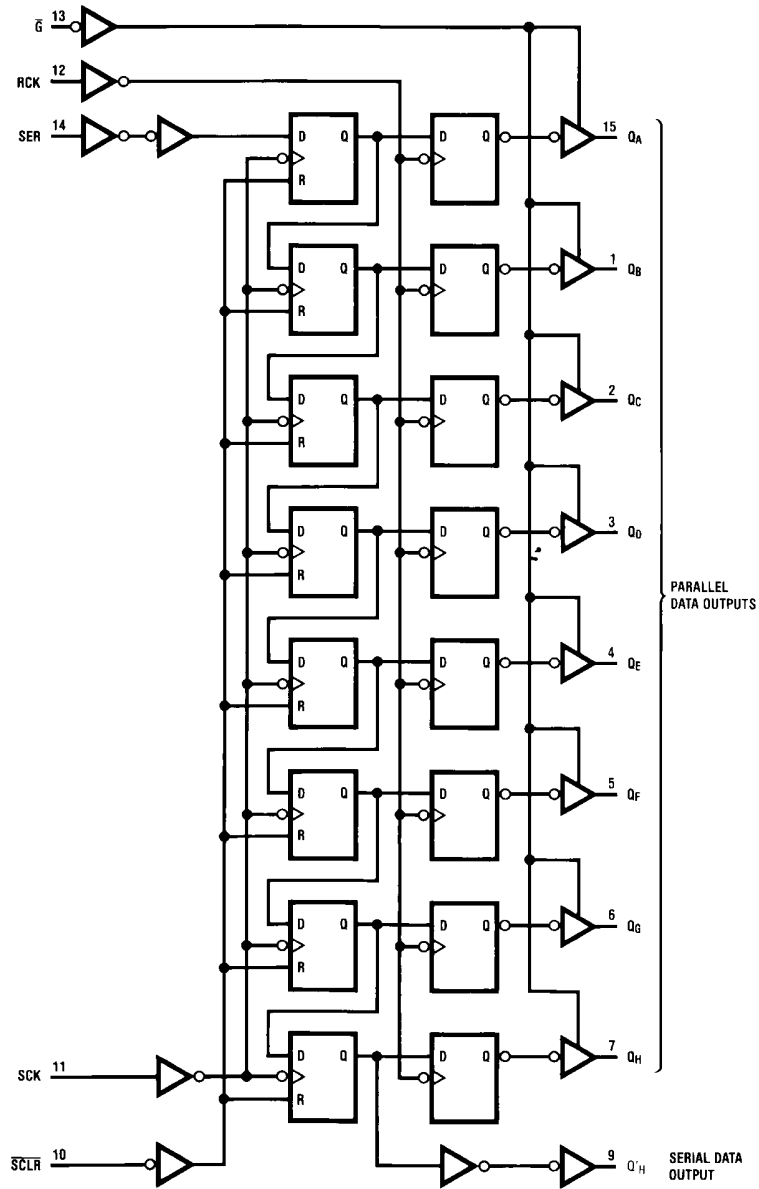


Truth Table

RCK	SCK	$\overline{\text{SCLR}}$	$\overline{\text{G}}$	Function
X	X	X	H	Q_A thru $Q_H = 3\text{-STATE}$
X	X	L	L	Shift Register cleared $Q_H = 0$
X	\uparrow	H	L	Shift Register clocked $Q_N = Q_{n-1}, Q_0 = \text{SER}$
\uparrow	X	H	L	Contents of Shift Register transferred to output latches

Logic Diagram

(positive logic)



AC Electrical Characteristics

 $V_{CC} = 5V, T_A = 25^\circ C, t_r = t_f = 6 \text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency of SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SCK to Q_H	$C_L = 45 \text{ pF}$	12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, RCK to Q_A thru Q_H	$C_L = 45 \text{ pF}$	18	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time from \bar{G} to Q_A thru Q_H	$R_L = 1 \text{ k}\Omega$ $C_L = 45 \text{ pF}$	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from \bar{G} to Q_A thru Q_H	$R_L = \text{k}\Omega$ $C_L = 5 \text{ pF}$	15	25	ns
t_S	Minimum Setup Time from SER to SCK			20	ns
t_S	Minimum Setup Time from SCLR to SCK			20	ns
t_S	Minimum Setup Time from SCK to RCK (Note 5)			40	ns
t_H	Minimum Hold Time from SER to SCK			0	ns
t_W	Minimum Pulse Width of SCK or RCK			16	ns

Note 5: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

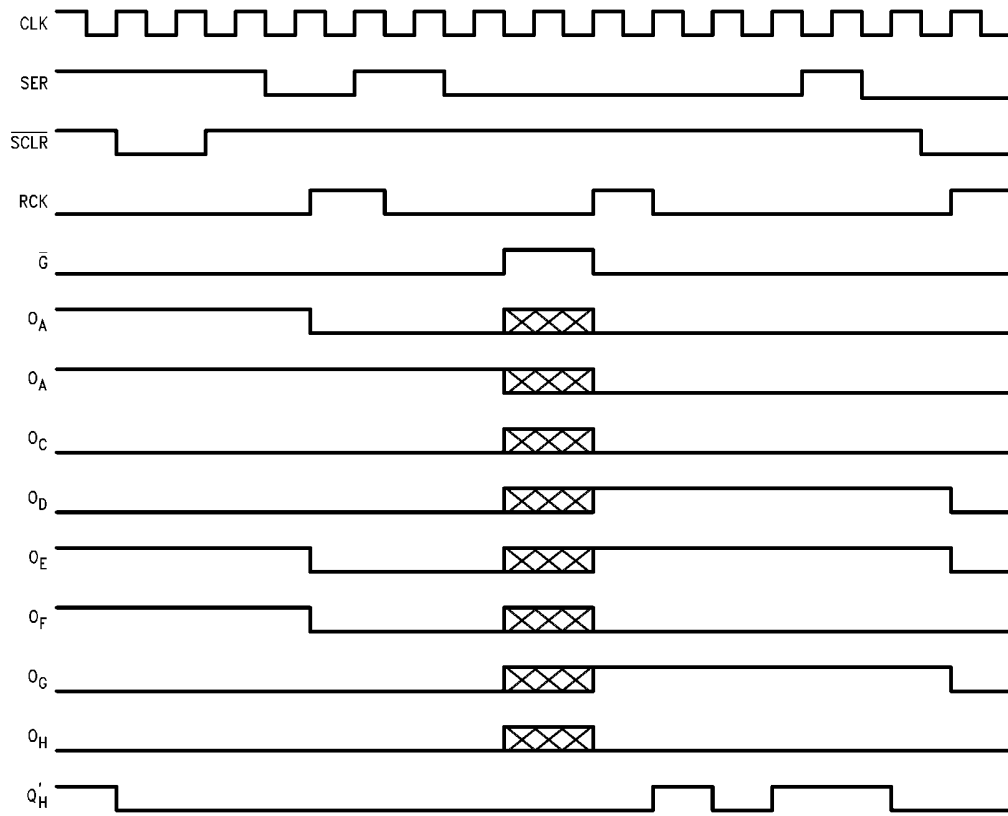
AC Electrical Characteristics


 $V_{CC} = 2.0\text{--}6.0V, C_L = 50 \text{ pF}, t_r = t_f = 6 \text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$				Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	$C_L = 50 \text{ pF}$	2.0V	10	6	4.8	4.0	MHz
			4.5V	45	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to Q_H	$C_L = 50 \text{ pF}$	2.0V	58	210	265	315	ns
			$C_L = 150 \text{ pF}$	2.0V	83	294	367	441
		$C_L = 50 \text{ pF}$	4.5V	14	42	53	63	ns
			$C_L = 150 \text{ pF}$	4.5V	17	58	74	88
		$C_L = 50 \text{ pF}$	6.0V	10	36	45	54	ns
			$C_L = 150 \text{ pF}$	6.0V	14	50	63	76
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_A thru Q_H	$C_L = 50 \text{ pF}$	2.0V	70	175	220	265	ns
			$C_L = 150 \text{ pF}$	2.0V	105	245	306	368
		$C_L = 50 \text{ pF}$	4.5V	21	35	44	53	ns
			$C_L = 150 \text{ pF}$	4.5V	28	49	61	74
		$C_L = 50 \text{ pF}$	6.0V	18	30	37	45	ns
			$C_L = 150 \text{ pF}$	6.0V	26	42	53	63
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCLR to Q_H		2.0V		175	221	261	ns
			4.5V		35	44	52	ns
			6.0V		30	37	44	ns

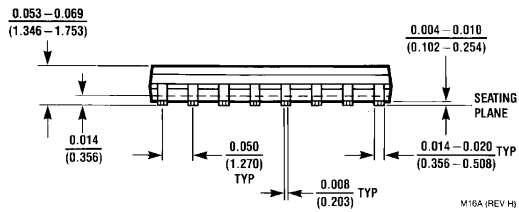
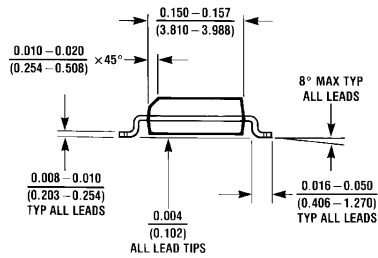
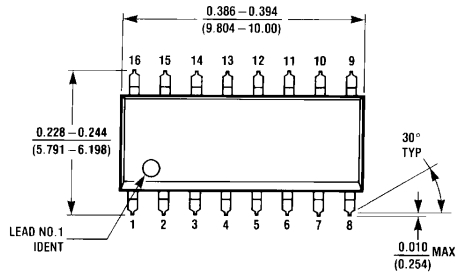
AC Electrical Characteristics (Continued)								
Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C	T _A = -40 to 85°C	T _A = -55 to 125°C	Units	
				Typ	Guaranteed Limits			
t _{PZH} , t _{PZL}	Maximum Output Enable from \overline{G} to Q _A thru Q _H	R _L = 1 kΩ	2.0V	75	175	220	265	ns
		C _L = 50 pF	2.0V	100	245	306	368	ns
		C _L = 150 pF	4.5V	15	35	44	53	ns
		C _L = 150 pF	4.5V	20	49	61	74	ns
		C _L = 50 pF	6.0V	13	30	37	45	ns
		C _L = 150 pF	6.0V	17	42	53	63	ns
t _{PHZ} , t _{PLZ}	Maximum Output Disable Time from \overline{G} to Q _A thru Q _H	R _L = 1 kΩ	2.0V	75	175	220	265	ns
		C _L = 50 pF	4.5V	15	35	44	53	ns
			6.0V	13	30	37	45	ns
t _S	Minimum Setup Time from SER to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t _R	Minimum Removal Time from \overline{SCLR} to SCK		2.0V		50	63	75	ns
			4.5V		10	13	15	ns
			6.0V		9	11	13	ns
t _S	Minimum Setup Time from SCK to RCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	26	ns
t _H	Minimum Hold Time SER to SCK		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t _W	Minimum Pulse Width of SCK or \overline{SCLR}		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	22	ns
t _r , t _f	Maximum Input Rise and Fall Time, Clock		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time Q _A -Q _H		2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t _{THL} , t _{TLH}	Maximum Output Rise & Fall Time Q _H		2.0V		75	95	110	ns
			4.5V		15	19	22	ns
			6.0V		13	16	19	ns
C _{PD}	Power Dissipation Capacitance, Outputs Enabled (Note 6)	$\overline{G} = V_{CC}$		90				pF
		$\overline{G} = GND$		150				pF
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF
C _{OUT}	Maximum Output Capacitance			15	20	20	20	pF
<p>Note 6: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC}.</p>								

Timing Diagram

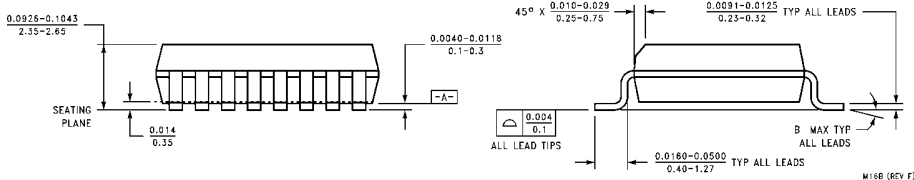
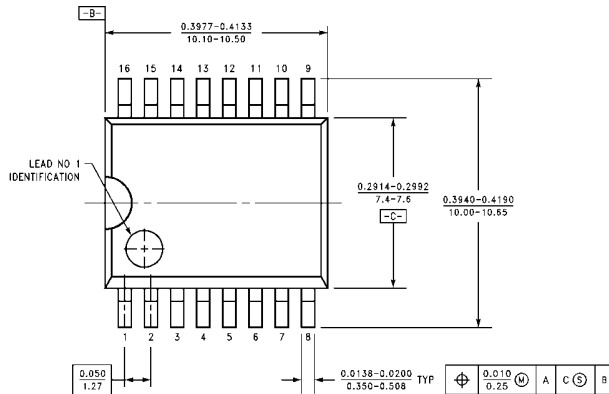


NOTE:  Implies that the output is in 3-STATE mode.

Physical Dimensions inches (millimeters) unless otherwise noted

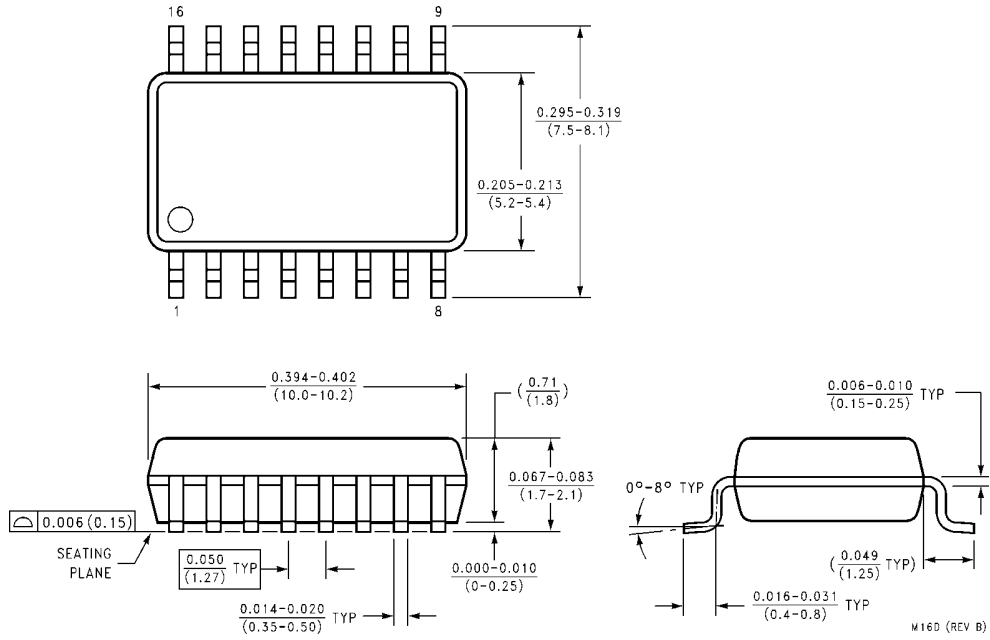


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A



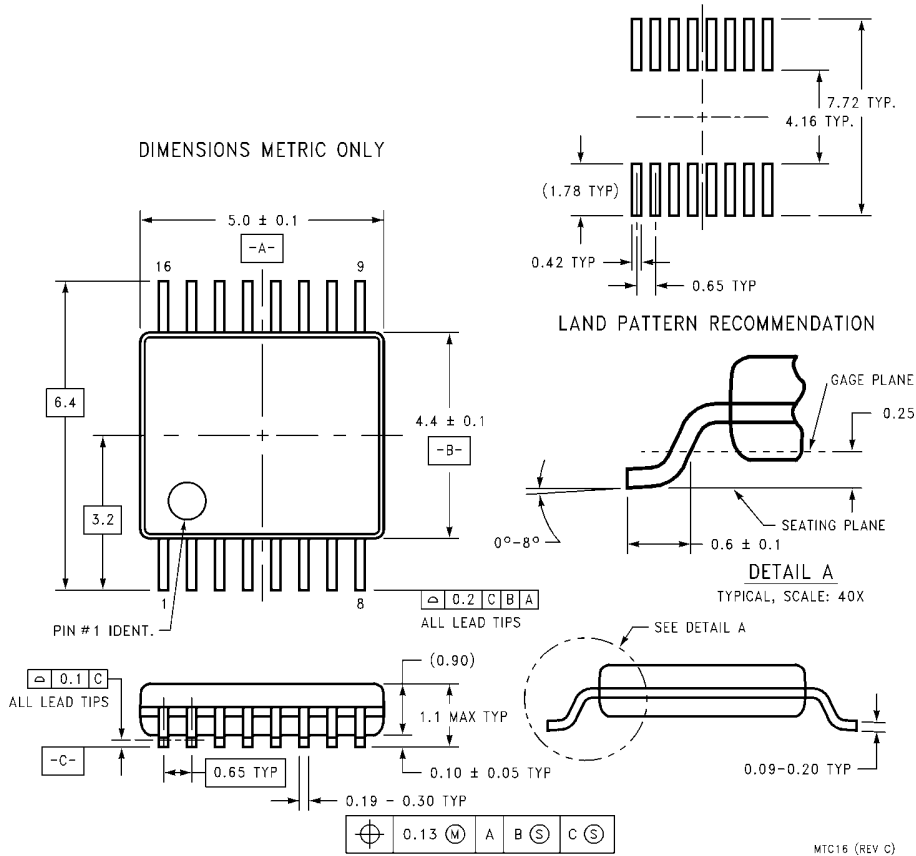
16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M16B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

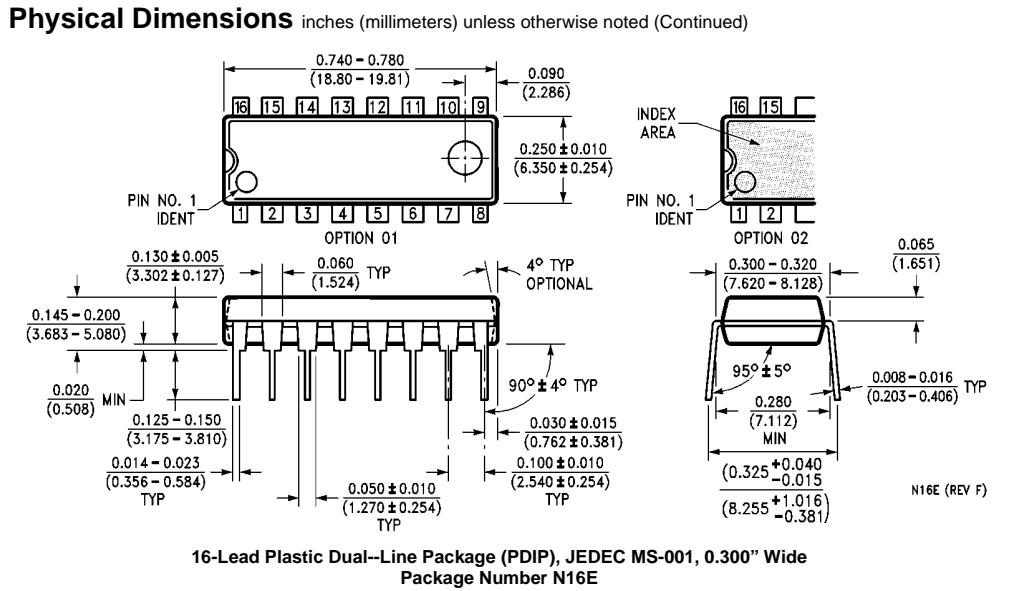


**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**



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