

MM74HCT540 • MM74HCT541 Inverting Octal 3-STATE Buffer • Octal 3-STATE Buffer

General Description

The MM74HCT540 and MM74HCT541 3-STATE buffers utilize advanced silicon-gate CMOS technology and are general purpose high speed inverting and non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the low power consumption of CMOS. Both devices are TTL input compatible and have a fanout of 15 LS-TTL equivalent inputs.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

The MM74HCT540 is an inverting buffer and the MM74HCT541 is a non-inverting buffer. The 3-STATE control gate operates as a two-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are HIGH, all eight outputs are in the high-impedance state.

In order to enhance PC board layout, the MM74HCT540 and MM74HCT541 offers a pinout having inputs and outputs on opposite sides of the package. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delay: 12 ns
- 3-STATE outputs for connection to system buses
- Low quiescent current: 80 μ A
- Output current: 6 mA (min.)

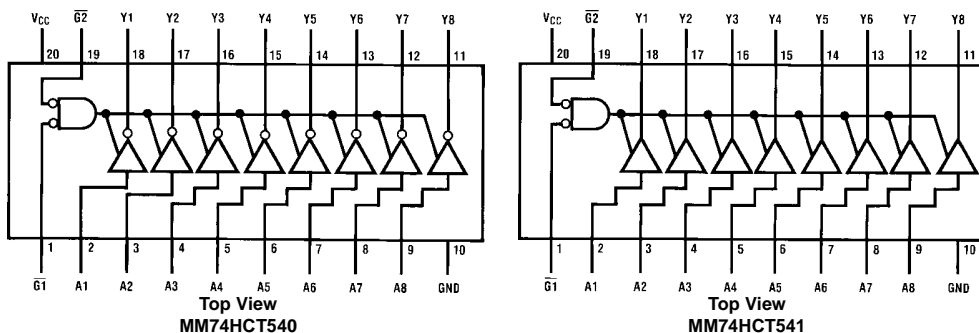
Ordering Code:

Order Number	Package Number	Package Description
MM74HCT540WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HCT540SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT540MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT540N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HCT541WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HCT541SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT541N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

Pin Assignments for DIP, SOIC, SOP and TSSOP



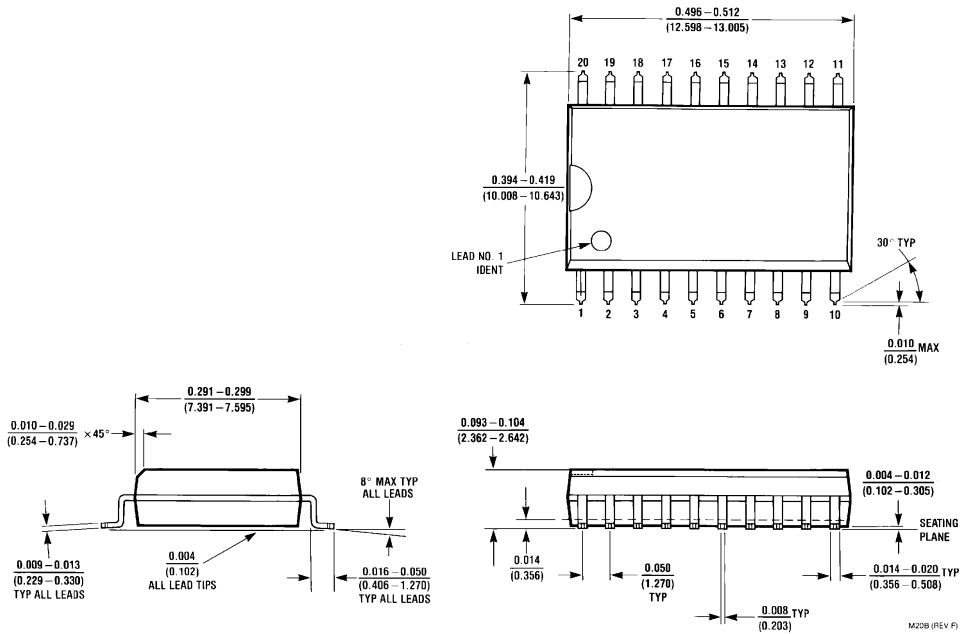
AC Electrical Characteristics						
MM74HCT540: $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $T_A = 25^\circ C$, (unless otherwise specified)						
Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units	
t_{PHL} , t_{PLH}	Maximum Output Propagation Delay	$C_L = 45$ pF	12	18	ns	
t_{PZL} , t_{PZH}	Maximum Output Enable Time	$C_L = 45$ pF $R_L = 1$ k Ω	14	28	ns	
t_{PLZ} , t_{PHZ}	Maximum Output Disable Time	$C_L = 5$ pF $R_L = 1$ k Ω	13	25	ns	

AC Electrical Characteristics							
MM74HCT540: $V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6$ ns (unless otherwise specified)							
Symbol	Parameter	Conditions	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	Units
			Typ	Guaranteed Limits			
t_{PHL} , t_{PLH}	Maximum Output Propagation Delay	$C_L = 50$ pF	12	20	25	30	ns
		$C_L = 150$ pF	22	30	38	45	ns
t_{PZH} , t_{PZL}	Maximum Output Enable Time	$R_L = 1$ k Ω , $C_L = 50$ pF	15	30	38	45	ns
		$C_L = 150$ pF	20	40	50	60	ns
t_{PHZ} , t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ k Ω , $C_L = 50$ pF	15	30	38	45	ns
t_{THL} , t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50$ pF	6	12	15	18	ns
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance		15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output) $\bar{Q} = V_{CC}$	12				pF
		$\bar{Q} = GND$	50				pF

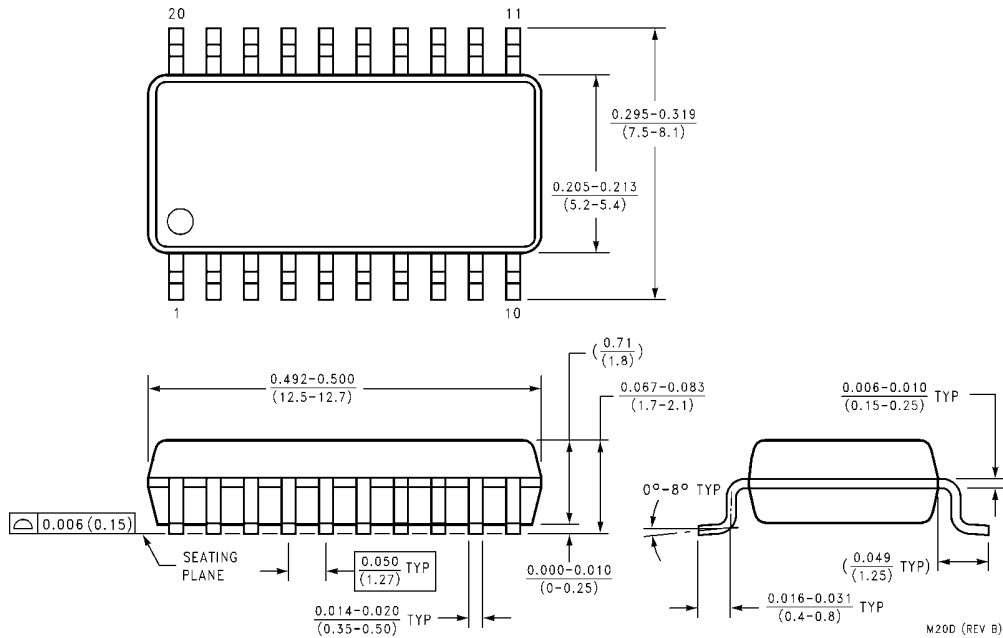
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

AC Electrical Characteristics							
MM74HCT541: $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $T_A = 25^\circ C$, (unless otherwise specified)							
Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units		
t_{PHL} , t_{PLH}	Maximum Output Propagation Delay	$C_L = 45$ pF	13	20	ns		
t_{PZL} , t_{PZH}	Maximum Output Enable Time	$C_L = 45$ pF $R_L = 1$ k Ω	17	28	ns		
t_{PLZ} , t_{PHZ}	Maximum Output Disable Time	$C_L = 5$ pF $R_L = 1$ k Ω	15	25	ns		
AC Electrical Characteristics							
MM74HCT541: $V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6$ ns (unless otherwise specified)							
Symbol	Parameter	Conditions	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	Units
			Typ	Guaranteed Limits			
t_{PHL} , t_{PLH}	Maximum Output Propagation Delay	$C_L = 50$ pF	14	23	29	34	ns
		$C_L = 150$ pF	17	33	42	49	ns
t_{PZH} , t_{PZL}	Maximum Output Enable Time	$R_L = 1$ k Ω $C_L = 50$ pF	17	30	38	45	ns
		$C_L = 150$ pF	22	40	50	60	ns
t_{PHZ} , t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ k Ω $C_L = 50$ pF	17	30	38	45	ns
t_{THL} , t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50$ pF	6	12	15	18	ns
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance		15	20	20	20	pF
C_{PD}	Power Dissipation	(per output) $\bar{G} = V_{CC}$	12				pF
	Capacitance (Note 6)	$\bar{G} = GND$	45				pF
<p>Note 6: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.</p>							

Physical Dimensions inches (millimeters) unless otherwise noted

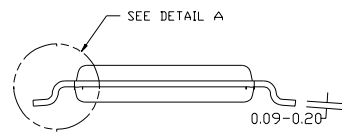
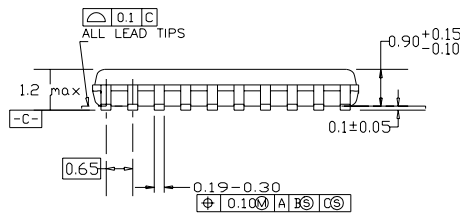
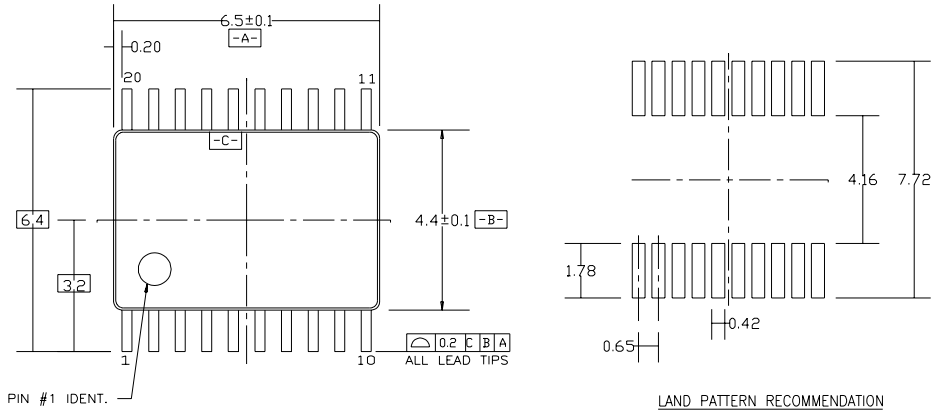


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B



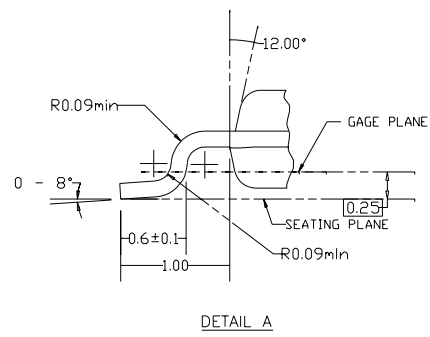
20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



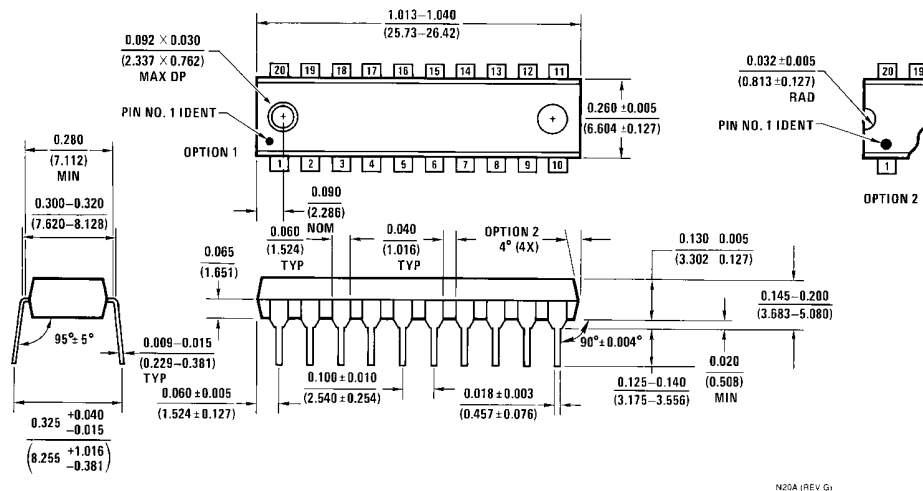
DIMENSIONS ARE IN MILLIMETERS

- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
 - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.



**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N20A

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