September 1996

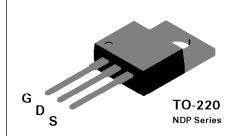


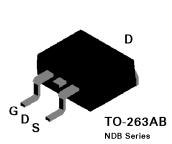
NDP7051L / NDB7051L N-Channel Logic Level Enhancement Mode Field Effect Transistor

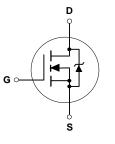
General Description

Features

- These logic level N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.
- 67 A, 50 V. $R_{DS(ON)} = 0.0145 \Omega @ V_{GS} = 5 V$ $R_{DS(ON)} = 0.0115 \Omega @ V_{GS} = 10 V.$
- Low drive requirements allowing operation directly from logic drivers. V_{GS(TH)} < 2.0V.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low R_{DS(ON)}.
- TO-220 and TO-263 (D²PAK) package for both through hole and surface mount applications.







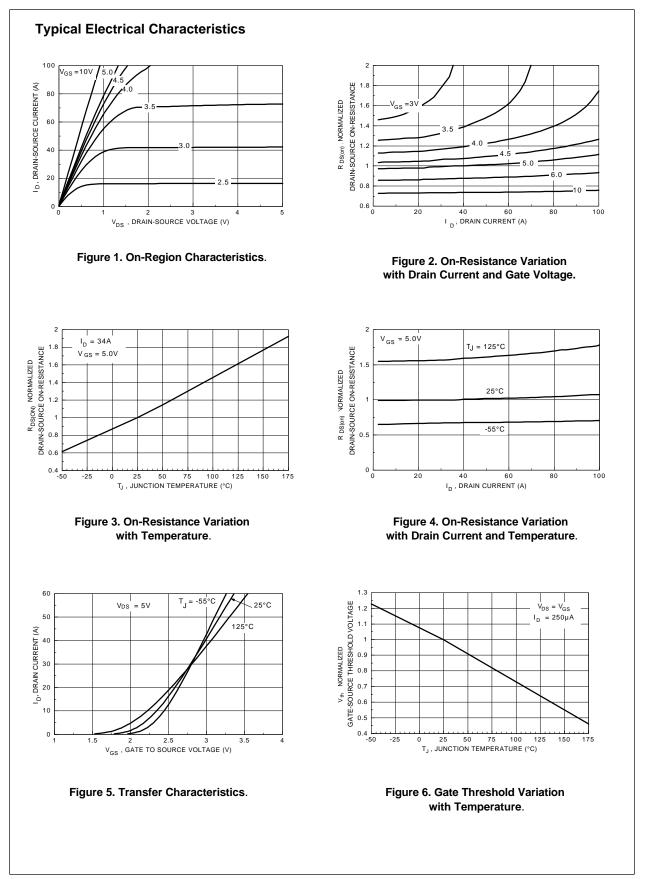
Absolute Maximum Ratings T_o = 25°C unless otherwise noted

Symbol	Parameter	NDP7051L	NDB7051L	Units
V _{DSS}	Drain-Source Voltage	50		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \le 1 M\Omega$)	50		V
V _{GSS}	Gate-Source Voltage - Continuous	±16		V
	- Nonrepetitive ($t_p < 50 \ \mu s$)	±2	25	
I _D	Drain Current - Continuous	6	7	А
	- Pulsed	20	00	
P _D	Maximum Power Dissipation @ $T_c = 25^{\circ}C$	13	W	
	Derate above 25°C	0.8	W/°C	
T_,,T _{stg}	Operating and Storage Temperature Range		o 175	°C

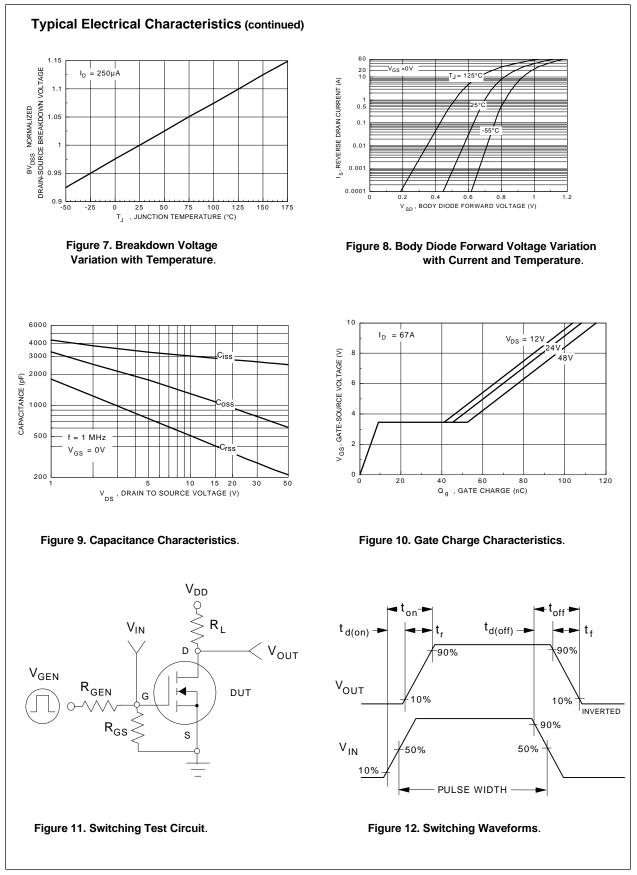
Symbol	Parameter	Conditions		Min	Тур	Max	Units
DRAIN-S	OURCE AVALANCHE RATINGS (Note 1)				-		
W _{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 25 \text{ V}, \text{ I}_{D} = 67 \text{ A}$				430	mJ
I _{AR}	Maximum Drain-Source Avalanche Cur	rent				67	Α
OFF CH/	ARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		50			V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{\rm DS} = 40 \text{ V}, V_{\rm GS} = 0 \text{ V}$				10	μA
			T _J = 125°C			1	mA
I _{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 16 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
	Gate - Body Leakage, Reverse	$V_{GS} = -16 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$				100	nA
ON CHAI	RACTERISTICS (Note 1)				-		
V _{GS(th)}	Gate Threshold Voltage	$V_{\rm DS} = V_{\rm GS}, I_{\rm D} = 250 \mu {\rm A}$		1	1.24	2	V
			T _J = 125°C	0.65	0.84	1.5	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 5 \text{ V}, \text{ I}_{D} = 34 \text{ A}$			0.013	0.0145	Ω
			T _J = 125°C		0.018	0.026	
		$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 34 \text{ A}$			0.01	0.0115	
l _{D(on)}	On-State Drain Current	$V_{GS} = 5 \text{ V}, V_{DS} = 10 \text{ V}$		60			А
9 _{FS}	Forward Transconductance	$V_{\rm DS} = 5 \text{ V}, \text{ I}_{\rm D} = 34 \text{ A}$			50		S
DYNAMI	C CHARACTERISTICS				-		
C _{iss}	Input Capacitance	$V_{DS} = 25 V, V_{GS} = 0 V,$ f = 1.0 MHz			2700		pF
C _{oss}	Output Capacitance				850		pF
C _{rss}	Reverse Transfer Capacitance				300		pF
SWITCHI	NG CHARACTERISTICS (Note 1)						
t _{D(on)}	Turn - On Delay Time	$V_{DD} = 25 \text{ V}, I_{D} = 34 \text{ A},$			17	30	nS
t,	Turn - On Rise Time	$V_{GS} = 5 \text{ V}, \text{ R}_{GEN} = 10 \Omega$ $\text{ R}_{GS} = 10 \Omega$			182	300	nS
t _{D(off)}	Turn - Off Delay Time				82	150	nS
t,	Turn - Off Fall Time				157	250	nS
Q _g	Total Gate Charge	V _{DS} = 12 V			56	80	nC
Q _{gs}	Gate-Source Charge	$I_{\rm D} = 67 \text{A} , V_{\rm GS} = 5 \text{V}$			9		nC
Q _{gd}	Gate-Drain Charge				32		nC

Symbol	Parameter	Conditions		Min	Тур	Max	Units
DRAIN-S	OURCE DIODE CHARACTERISTICS	·			•	•	
I _s	Maximum Continuos Drain-Source Diode Forward Current				67	Α	
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				200	Α	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 34 \text{ A} \text{ (Note 1)}$			0.92	1.3	V
			T _J = 125°C		0.83	1.2	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0 V, I_F = 67 A,$ $dI_F/dt = 100 A/\mu s$		40	75	150	ns
l _m	Reverse Recovery Current			2	3.6	10	A
THERMA	L CHARACTERISTICS	•			•		
R _{θJC}	Thermal Resistance, Junction-to-Case				1.15	°C/W	
R _{eja}	Thermal Resistance, Junction-to-Ambient				62.5	°C/W	

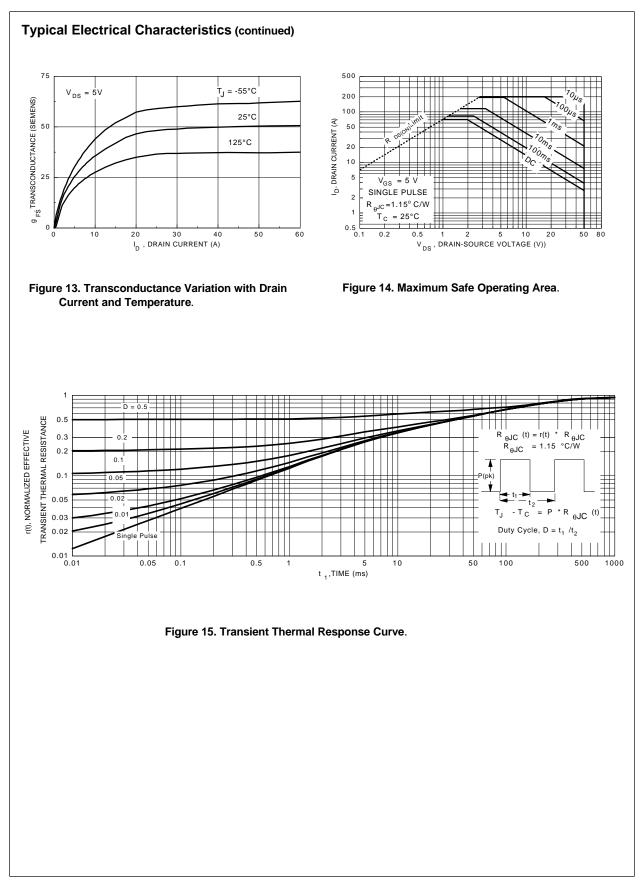
1. Pulse Test: Pulse Width \leq 300 µs, Duty Cycle \leq 2.0%.



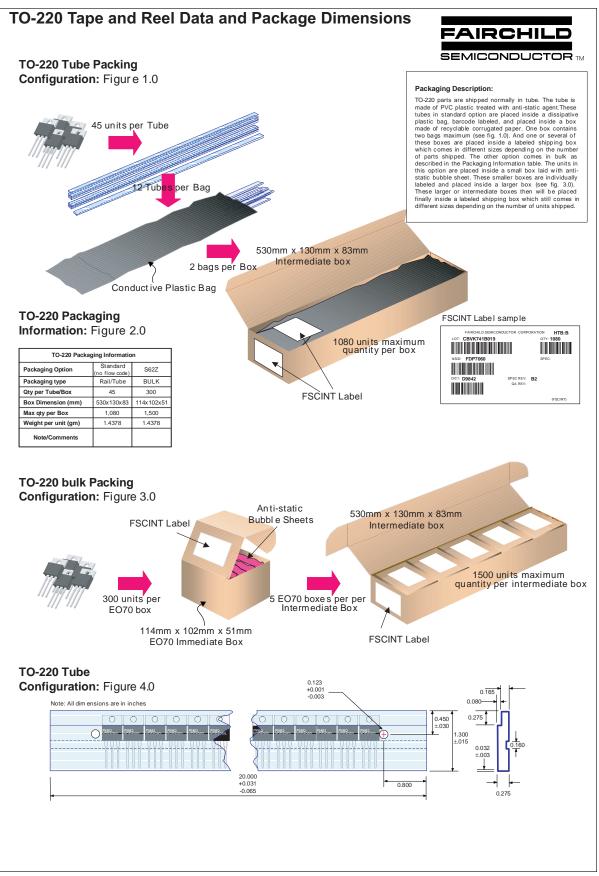
NDP7051L Rev.D/NDB7051L Rev.E



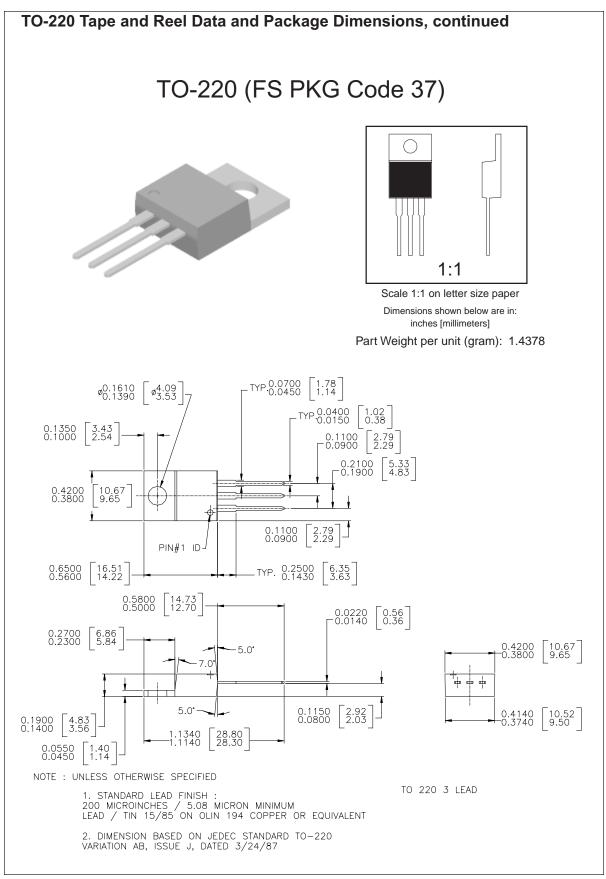
NDP7051L Rev.D/NDB7051L Rev.E



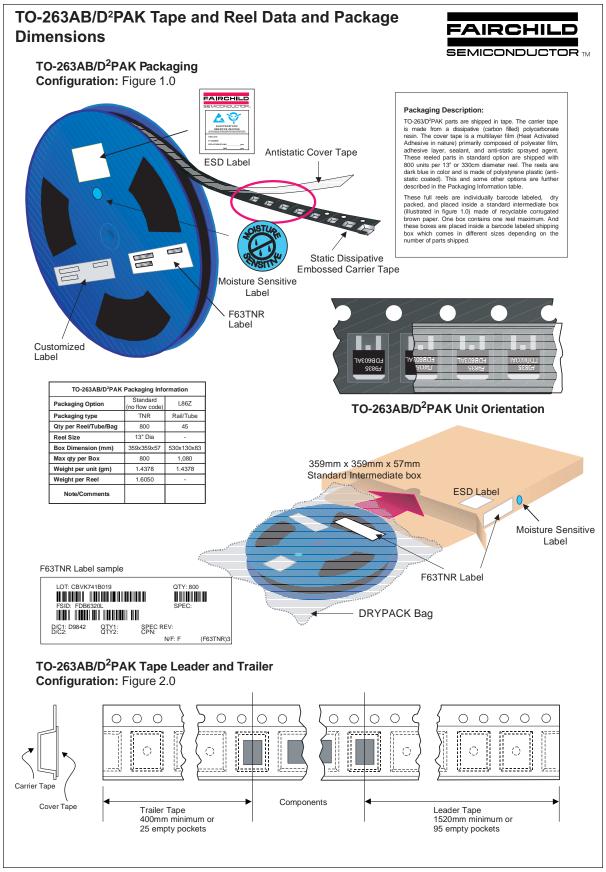
NDP7051L Rev.D/NDB7051L Rev.E



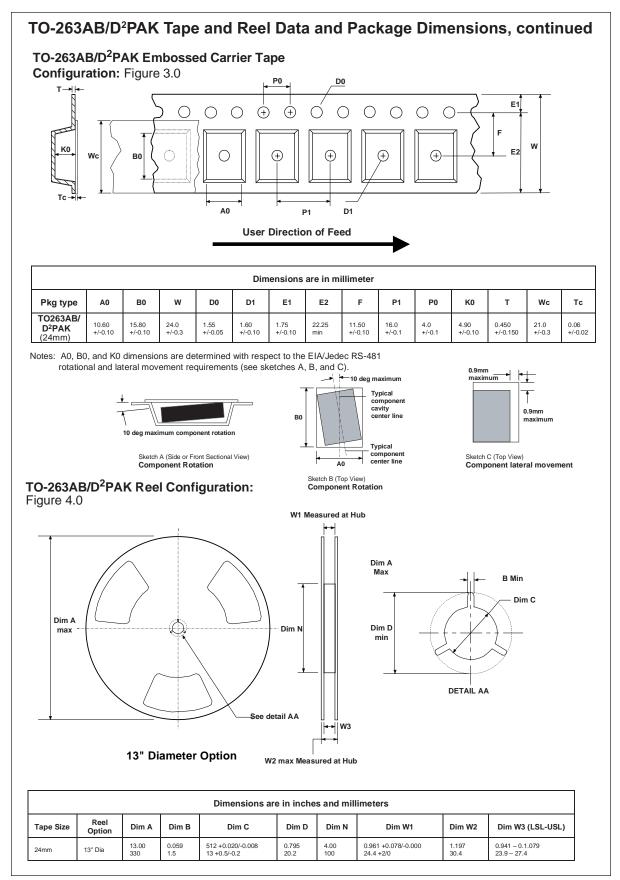
August 1999, Rev. B

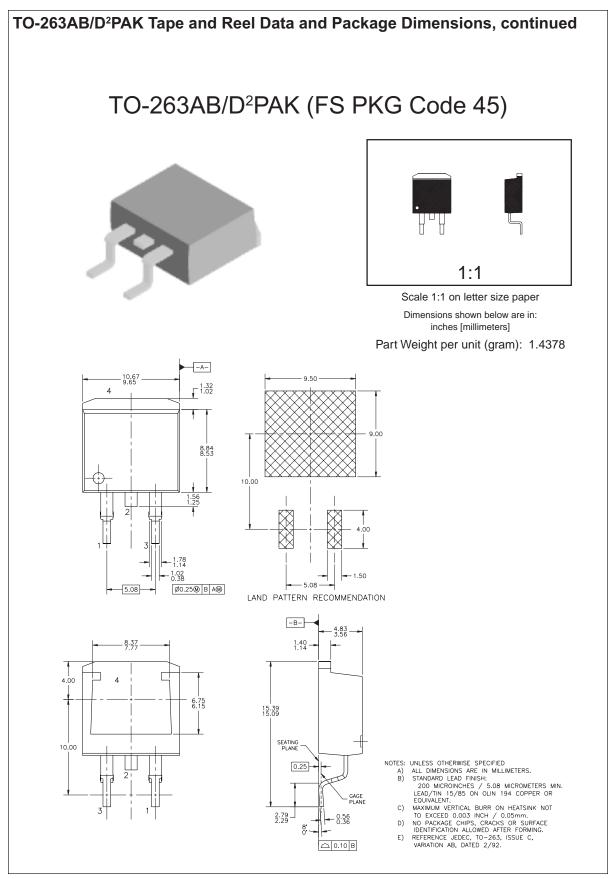


September 1998, Rev. A



September 1999, Rev. B





August 1998, Rev. A

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACExTM CoolFETTM CROSSVOLTTM E²CMOSTM FACTTM FACT Quiet SeriesTM FAST[®] FAST[®] FASTrTM GTOTM HiSeCTM ISOPLANAR™ MICROWIRE™ POP™ PowerTrench® QFET™ QS™ Quiet Series™ SuperSOT™-3 SuperSOT™-6 SuperSOT™-8 SyncFET™ TinyLogic™ UHC™ VCX™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user. 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.