September 1996

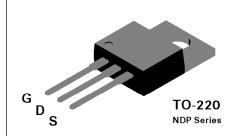


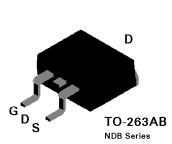
# NDP7051L / NDB7051L N-Channel Logic Level Enhancement Mode Field Effect Transistor

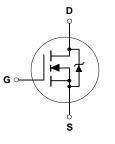
#### **General Description**

Features

- These logic level N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.
- 67 A, 50 V.  $R_{DS(ON)} = 0.0145 \Omega @ V_{GS} = 5 V$  $R_{DS(ON)} = 0.0115 \Omega @ V_{GS} = 10 V.$
- Low drive requirements allowing operation directly from logic drivers. V<sub>GS(TH)</sub> < 2.0V.</li>
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low R<sub>DS(ON)</sub>.
- TO-220 and TO-263 (D<sup>2</sup>PAK) package for both through hole and surface mount applications.







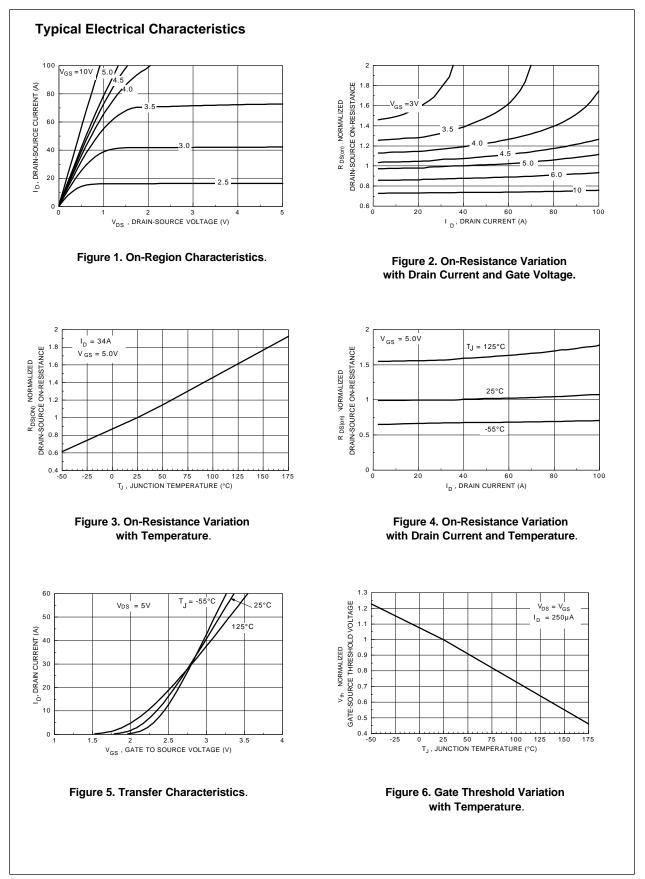
## **Absolute Maximum Ratings** T<sub>o</sub> = 25°C unless otherwise noted

Symbol	Parameter	NDP7051L	NDB7051L	Units
V <sub>DSS</sub>	Drain-Source Voltage	50		V
$V_{\text{DGR}}$	Drain-Gate Voltage ( $R_{GS} \le 1 M\Omega$ )	50		V
V <sub>GSS</sub>	Gate-Source Voltage - Continuous	±16		V
	- Nonrepetitive ( $t_p < 50 \ \mu s$ )	±2	25	
I <sub>D</sub>	Drain Current - Continuous	6	7	А
	- Pulsed	20	00	
P <sub>D</sub>	Maximum Power Dissipation @ $T_c = 25^{\circ}C$	13	W	
	Derate above 25°C	0.8	W/°C	
T_,,T <sub>stg</sub>	Operating and Storage Temperature Range		o 175	°C

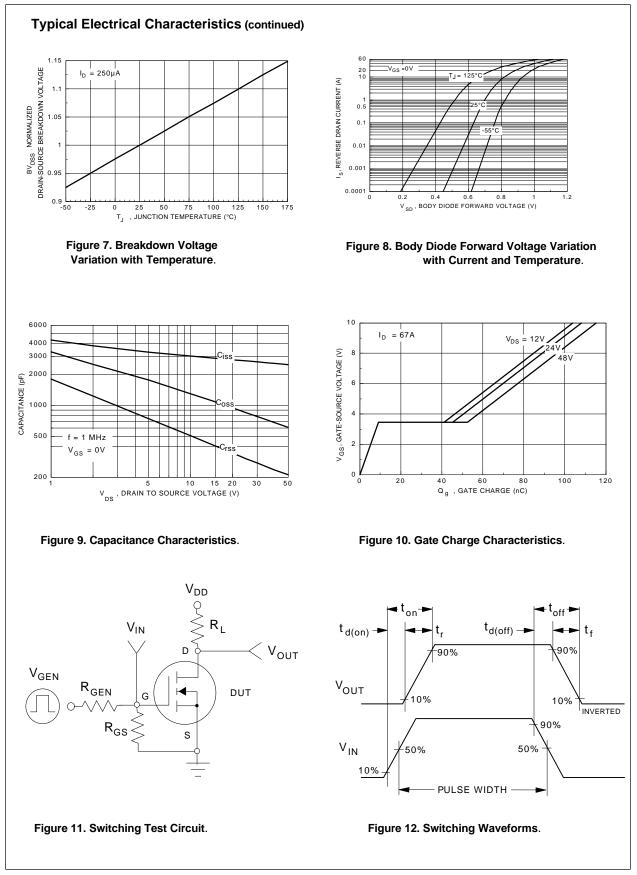
Symbol	Parameter	Conditions		Min	Тур	Max	Units
DRAIN-S	OURCE AVALANCHE RATINGS (Note 1)				-		
W <sub>DSS</sub>	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 25 \text{ V}, \text{ I}_{D} = 67 \text{ A}$				430	mJ
I <sub>AR</sub>	Maximum Drain-Source Avalanche Cur	rent				67	Α
OFF CH/	ARACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		50			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{\rm DS} = 40 \text{ V}, V_{\rm GS} = 0 \text{ V}$				10	μA
			T <sub>J</sub> = 125°C			1	mA
I <sub>GSSF</sub>	Gate - Body Leakage, Forward	$V_{GS} = 16 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
	Gate - Body Leakage, Reverse	$V_{GS} = -16 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$				100	nA
ON CHAI	RACTERISTICS (Note 1)				-		
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{\rm DS} = V_{\rm GS}, I_{\rm D} = 250 \mu {\rm A}$		1	1.24	2	V
			T <sub>J</sub> = 125°C	0.65	0.84	1.5	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 5 \text{ V}, \text{ I}_{D} = 34 \text{ A}$			0.013	0.0145	Ω
			T <sub>J</sub> = 125°C		0.018	0.026	
		$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 34 \text{ A}$			0.01	0.0115	
l <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 5 \text{ V}, V_{DS} = 10 \text{ V}$		60			А
9 <sub>FS</sub>	Forward Transconductance	$V_{\rm DS} = 5 \text{ V}, \text{ I}_{\rm D} = 34 \text{ A}$			50		S
DYNAMI	C CHARACTERISTICS				-		
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25 V, V_{GS} = 0 V,$ f = 1.0 MHz			2700		pF
C <sub>oss</sub>	Output Capacitance				850		pF
C <sub>rss</sub>	Reverse Transfer Capacitance				300		pF
SWITCHI	NG CHARACTERISTICS (Note 1)						
t <sub>D(on)</sub>	Turn - On Delay Time	$V_{DD} = 25 \text{ V}, I_{D} = 34 \text{ A},$			17	30	nS
t,	Turn - On Rise Time	$V_{GS} = 5 \text{ V}, \text{ R}_{GEN} = 10 \Omega$ $\text{ R}_{GS} = 10 \Omega$			182	300	nS
t <sub>D(off)</sub>	Turn - Off Delay Time				82	150	nS
t,	Turn - Off Fall Time				157	250	nS
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 12 V			56	80	nC
Q <sub>gs</sub>	Gate-Source Charge	$I_{\rm D} = 67  \text{A}  ,  V_{\rm GS} = 5  \text{V}$			9		nC
Q <sub>gd</sub>	Gate-Drain Charge				32		nC

Symbol	Parameter	Conditions		Min	Тур	Max	Units
DRAIN-S	OURCE DIODE CHARACTERISTICS	·			•	•	
I <sub>s</sub>	Maximum Continuos Drain-Source Diode Forward Current				67	Α	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				200	Α	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 34 \text{ A} \text{ (Note 1)}$			0.92	1.3	V
			T <sub>J</sub> = 125°C		0.83	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 V, I_F = 67 A,$ $dI_F/dt = 100 A/\mu s$		40	75	150	ns
l <sub>m</sub>	Reverse Recovery Current			2	3.6	10	A
THERMA	L CHARACTERISTICS	•			•		
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case				1.15	°C/W	
R <sub>eja</sub>	Thermal Resistance, Junction-to-Ambient				62.5	°C/W	

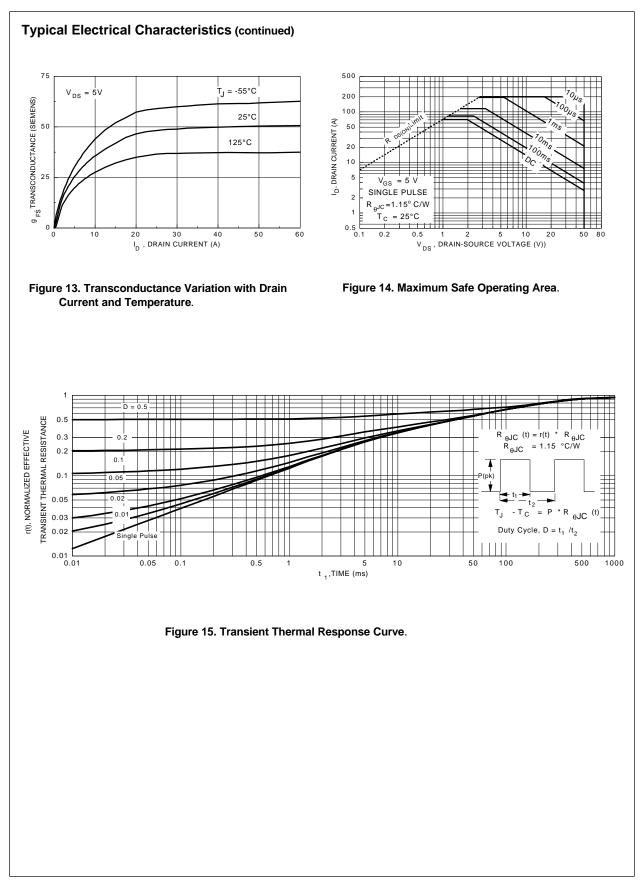
1. Pulse Test: Pulse Width  $\leq$  300 µs, Duty Cycle  $\leq$  2.0%.



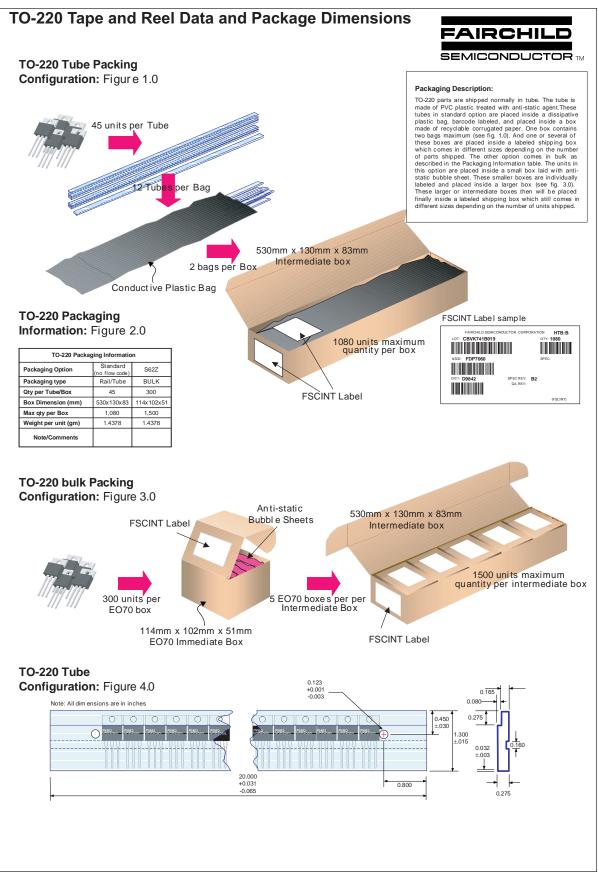
NDP7051L Rev.D/NDB7051L Rev.E



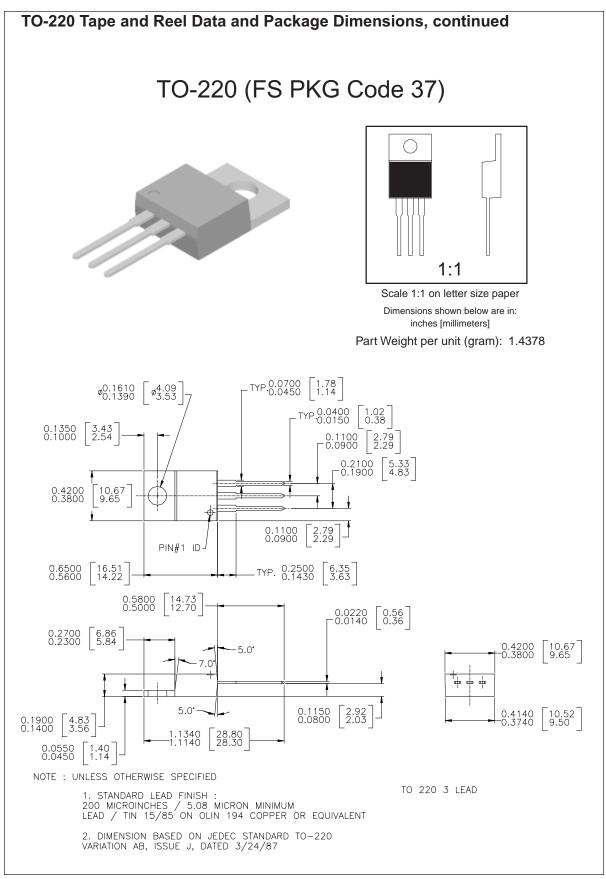
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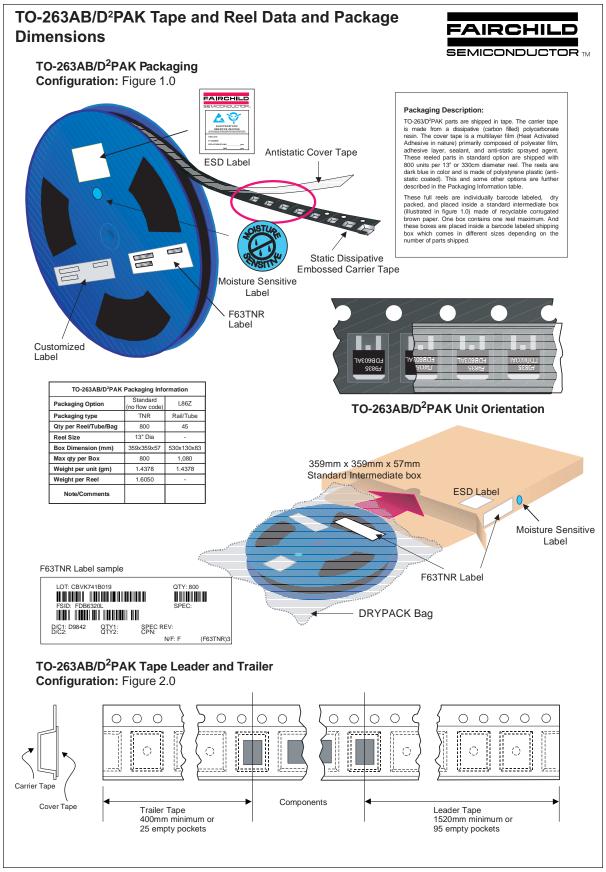
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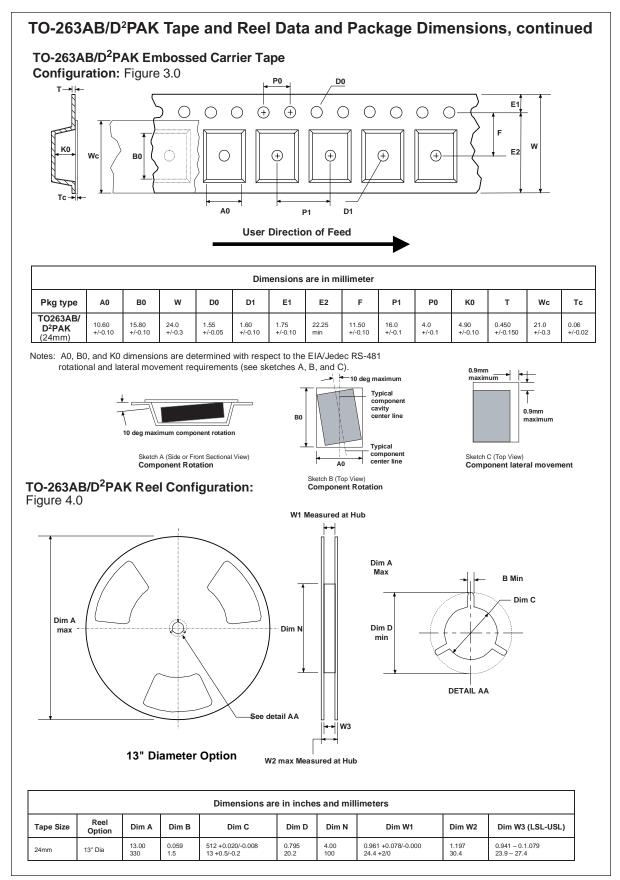
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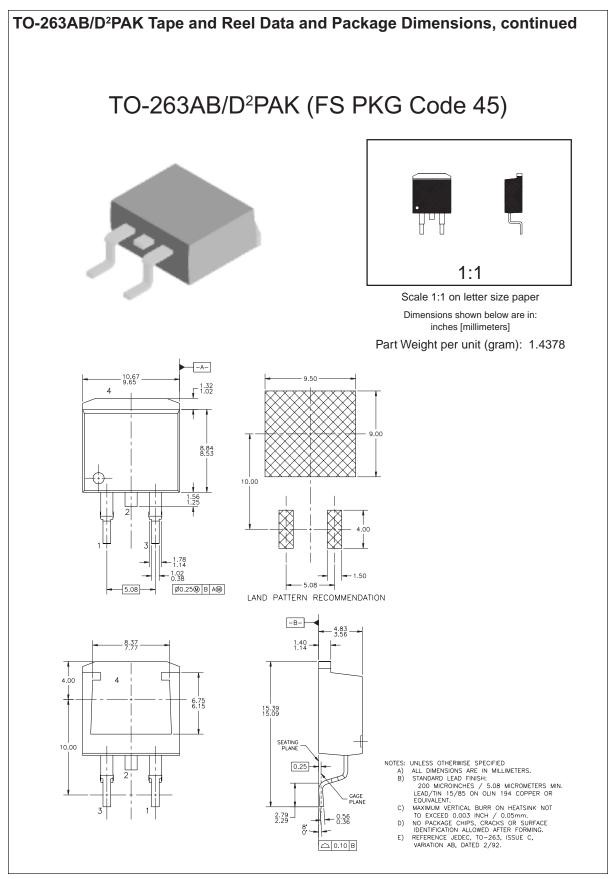


September 1998, Rev. A



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