# May 2000 ADVANCE INFORMATION

# **FDS7064A**

# 30V N-Channel PowerTrench MOSFET

### **General Description**

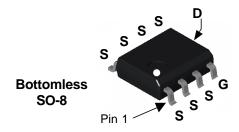
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for "low side" synchronous rectifier operation, providing an extremely low  $R_{\text{DS}(\text{ON})}$  in a small package.

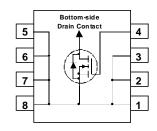
## **Applications**

- · Synchronous rectifier
- DC/DC converter

#### **Features**

- 19 A, 30 V  $R_{DS(ON)} = 6.5 \text{ m}\Omega$  @  $V_{GS} = 4.5 \text{ V}$
- High performance trench technology for extremely low  $R_{\mbox{\scriptsize DS(ON)}}$
- High power and current handling capability
- · Fast switching
- Bottomless™ SO-8 package: Enhanced thermal performance in industry-standard package size





Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	bol Parameter		Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage		30	V
V <sub>GSS</sub>	Gate-Source Voltage		±12	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	19	А
	- Pulsed		60	
P <sub>D</sub>	Power Dissipation for Single Operation	(Note 1a)	3.9	W
$T_J$ , $T_{STG}$	Operating and Storage Junction Temperature Range		-55 to +175	°C

## **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	38	°C/W
R <sub>eJC</sub>	Thermal Resistance, Junction-to-Case		1	°C/W

## **Package Marking and Ordering Information**

Device Marking	Device	Reel Size	Tape width	Quantity
FDS7064A	FDS7064A	13"	12mm	2500 units

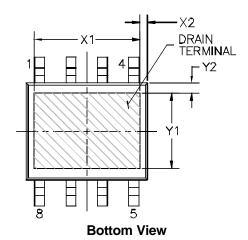
Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics			I	l	ı
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250  \mu\text{A}$	30			V
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, Referenced to 25°C		20		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			1	μΑ
GSSF	Gate-Body Leakage, Forward	V <sub>GS</sub> = 12 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	$V_{GS} = -12 \text{ V}$ , $V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.8	1.2	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		-4		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 19 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 21 \text{ A}$			6.5 5.5	mΩ
D(on)	On-State Drain Current	$V_{GS} = 4.5 \text{ V}, V_{DS} = 5 \text{ V}$	50			Α
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, \qquad I_{D} = 19 \text{ A}$		75		S
Dynamio	Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$		5070		pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		550		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			230		pF
Switchir	ng Characteristics (Note 2)					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 10 \text{ V},  I_D = 1 \text{ A},$		17	25	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$		18	25	ns
d(off)	Turn-Off Delay Time			69	100	ns
t <sub>f</sub>	Turn-Off Fall Time	7		29	42	ns
$Q_g$	Total Gate Charge	$V_{DS} = 15 \text{ V}, I_{D} = 19 \text{ A},$		33	46	nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = 4.5 \text{ V}$		7.5		nC
$Q_{gd}$	Gate-Drain Charge			6.8		nC
Drain-S	ource Diode Characteristics	and Maximum Ratings				
l <sub>s</sub>	Maximum Continuous Drain-Source				3.2	Α
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_S = 3.2 \text{ A}  \text{(Note 2)}$			1.2	V

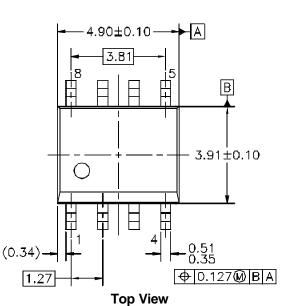
#### Notes

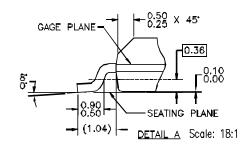
 $<sup>\</sup>textbf{1.}\,\,R_{\theta JA}\,\text{is the junction-to-ambient thermal resistance.}\,\,R_{\theta JA}\,\text{depends on the user's board design}.$ 

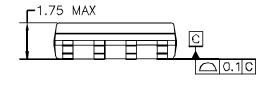
a) 38°C/W when mounted on a 1in² pad of 2 oz copper

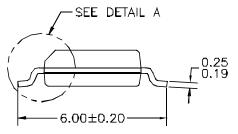
## **Dimensional Outline and Pad Layout**

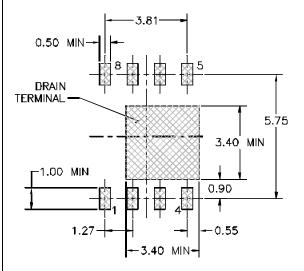












## **Minimum Recommended Landing Pattern**

Notes Unless otherwise Specified

- a) All dimensions in mm
- b) Standard lead finish:  $20-80~\mu$  inches nickel /  $6~\mu$  inches palladium
- c) Chip Size Dimensional Table

Chip	Size		
X1	Y1	X2	Y2
2.36	2.36	0.75	0.67

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