

FEATURES

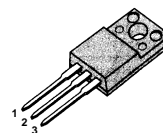
- Advanced New Design
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Very Low Intrinsic Capacitances
- Excellent Switching Characteristics
- Unrivalled Gate Charge: 6.0nC (Typ.)
- Extended Safe Operating Area
- Lower $R_{DS(ON)}$: 2.06 Ω (Typ.)

$$BV_{DSS} = -200V$$

$$R_{DS(ON)} = 2.7\Omega$$

$$I_D = -2.2A$$

TO-220F



1. Gate 2. Drain 3. Source

ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Value	Units
V_{DSS}	Drain-to-Source Voltage	-200	V
I_D	Continuous Drain Current ($T_C = 25^\circ C$)	-2.2	A
	Continuous Drain Current ($T_C = 100^\circ C$)	-1.39	
I_{DM}	Drain Current-Pulsed ①	-8.8	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy ②	150	mJ
I_{AR}	Avalanche Current ①	-2.2	A
E_{AR}	Repetitive Avalanche Energy ①	3.2	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
P_D	Total Power Dissipation ($T_C = 25^\circ C$)	32	W
	Linear Derating Factor	0.26	
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ C$
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

THERMAL RESISTANCE

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	-	3.9	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient	-	62.5	

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristics	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	-200	-	-	V	$V_{GS}=0V, I_D=-250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	-	-0.18	-	V/ $^\circ\text{C}$	$I_D=-250\mu A$, See Fig 7
$V_{GS(th)}$	Gate Threshold Voltage	-3.0	-	-5.0	V	$V_{DS}=-5V, I_D=-250\mu A$
I_{GSS}	Gate-Source Leakage, Forward	-	-	-100	nA	$V_{GS}=-30V$
	Gate-Source Leakage, Reverse	-	-	100		$V_{GS}=30V$
I_{DSS}	Drain-to-Source Leakage Current	-	-	-1	μA	$V_{DS}=-200V$
		-	-	-10		$V_{DS}=-160V, T_C=125^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	-	2.06	2.7	Ω	$V_{GS}=-10V, I_D=-1.1A$ ④
g_{fs}	Forward Transconductance	-	1.15	-	S	$V_{DS}=-40V, I_D=-1.1A$ ④
C_{iss}	Input Capacitance	-	190	250	pF	$V_{GS}=0V, V_{DS}=-25V$ $f=1\text{MHz}$ See Fig 5
C_{oss}	Output Capacitance	-	45	60		
C_{rss}	Reverse Transfer Capacitance	-	7.5	10		
$t_{d(on)}$	Turn-On Delay Time	-	8.5	25	ns	$V_{DD}=-100V, I_D=-2.8A$ $R_G=50\Omega$ See Fig 13 ④ ⑤
t_r	Rise Time	-	35	80		
$t_{d(off)}$	Turn-Off Delay Time	-	12	35		
t_f	Fall Time	-	25	60		
Q_g	Total Gate Charge	-	6.0	8.0	nC	$V_{DS}=-160V, V_{GS}=-10V$ $I_D=-2.8A$ See Fig 6 & Fig 12 ④ ⑤
Q_{gs}	Gate-Source Charge	-	1.7	-		
Q_{gd}	Gate-Drain (Miller) Charge	-	2.9	-		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristics	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current	-	-	-2.2	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	-	-	-8.8		
V_{SD}	Diode Forward Voltage ④	-	-	-5.0	V	$T_J=25^\circ\text{C}, I_S=-2.2A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	-	100	-	ns	$T_J=25^\circ\text{C}, I_F=-2.8A, V_{DD}=-160V$
Q_{rr}	Reverse Recovery Charge	-	0.34	-	μC	$di_F/dt=100A/\mu\text{s}$ ④

Notes:

- ① Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- ② $L=46.5\text{mH}, I_{AS}=-2.2A, V_{DD}=-50V, R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
- ③ $I_{SD} \leq -2.8A, di/dt \leq 300A/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$
- ④ Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
- ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

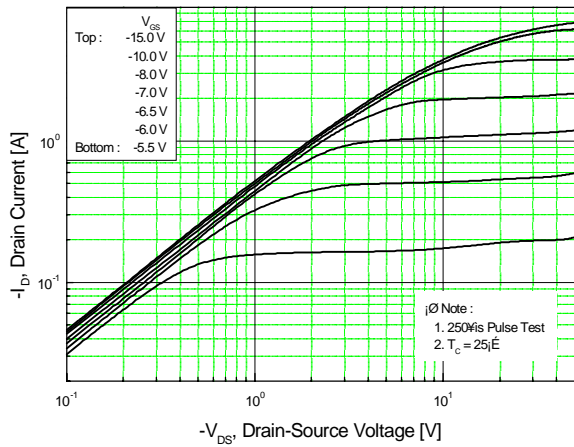


Fig 2. Transfer Characteristics

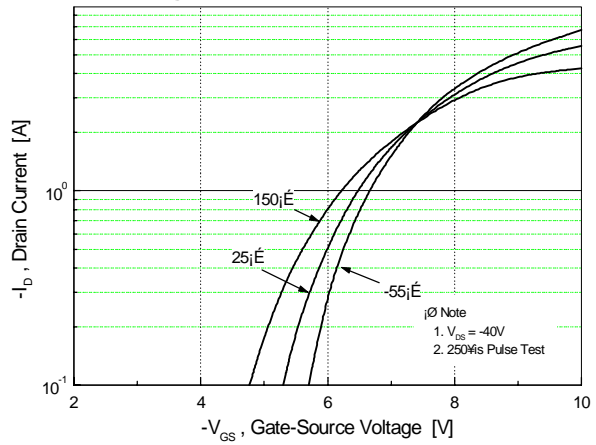


Fig 3. On-Resistance vs. Drain Current

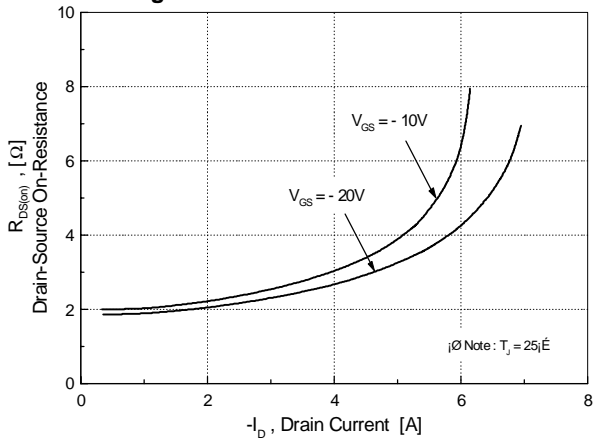


Fig 4. Source-Drain Diode Forward Voltage

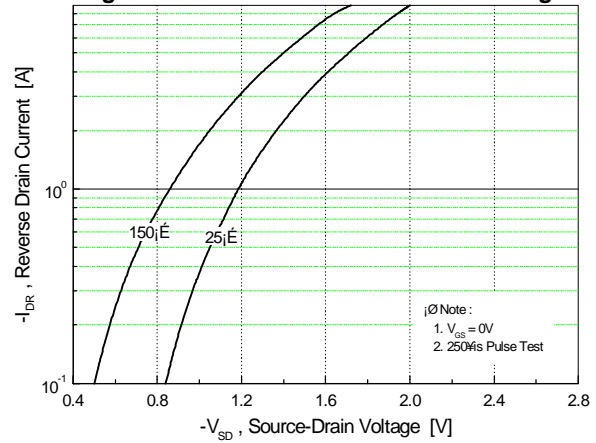


Fig 5. Capacitance vs. Drain-Source Voltage

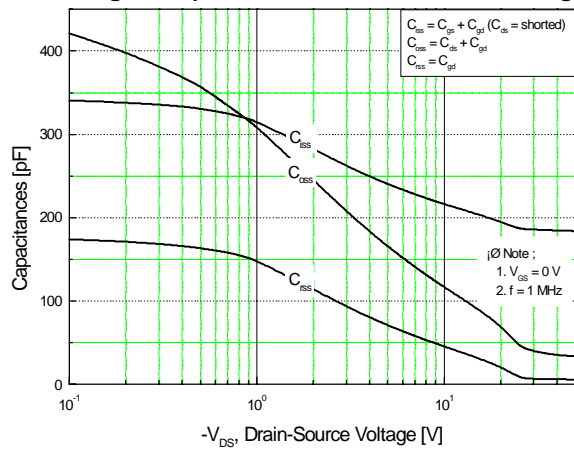


Fig 6. Gate Charge vs. Gate-Source Voltage

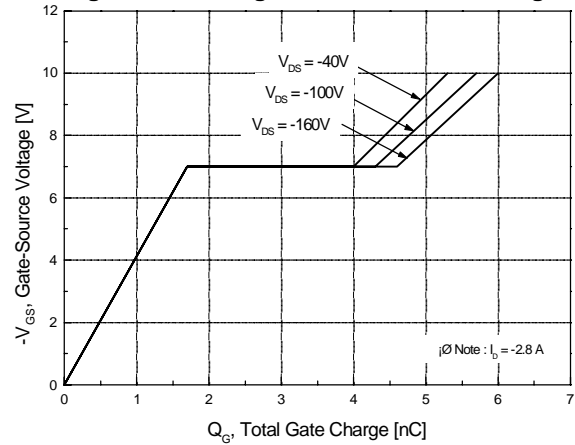


Fig 7. Breakdown Voltage vs. Temperature

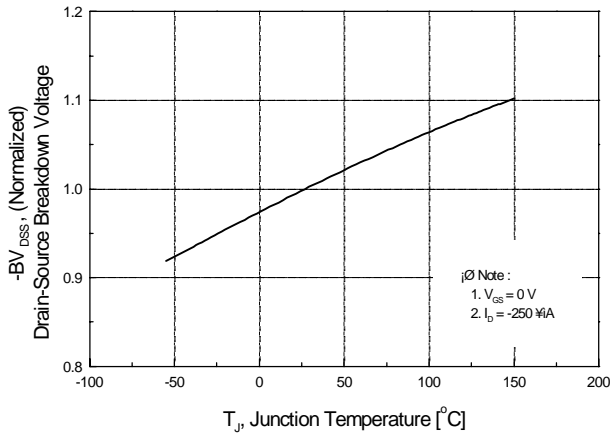


Fig 8. On-Resistance vs. Temperature

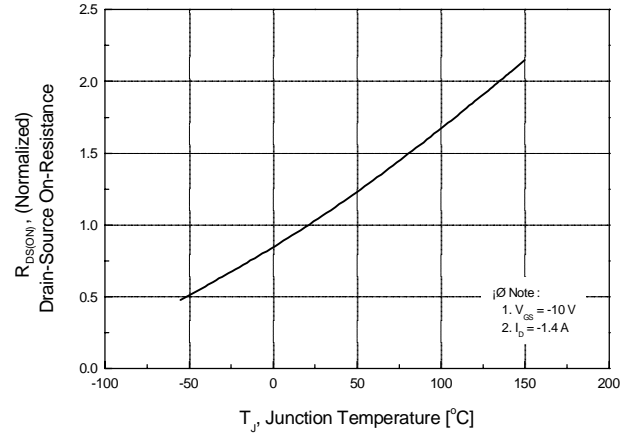


Fig 9. Max. Safe Operating Area

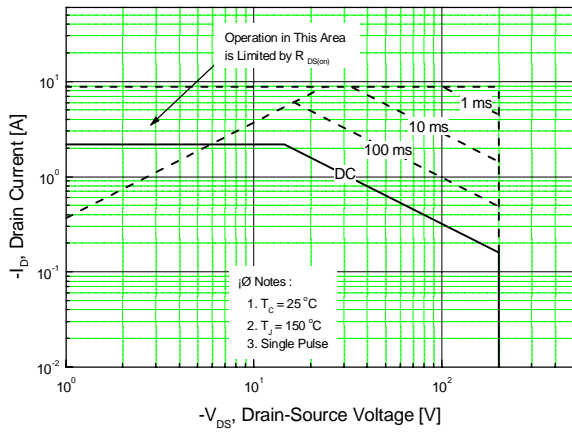


Fig 10. Max. Drain Current vs. Case Temperature

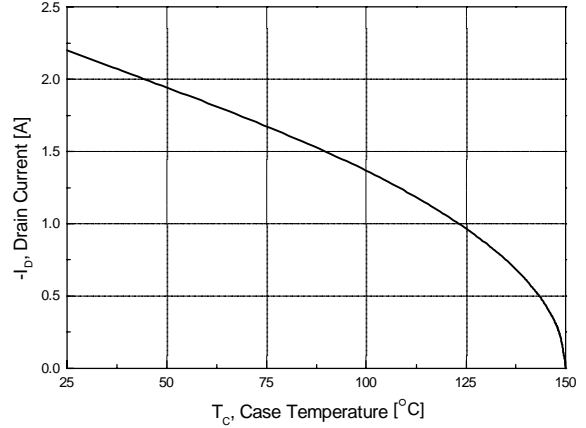


Fig 11. Thermal Response

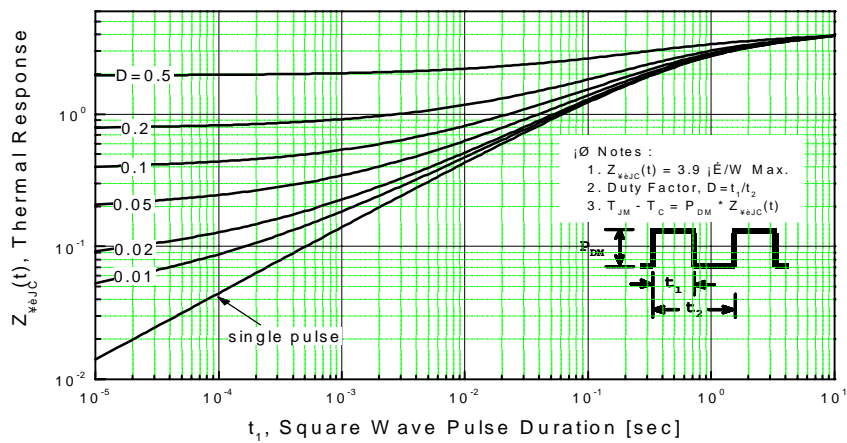


Fig 12. Gate Charge Test Circuit & Waveform

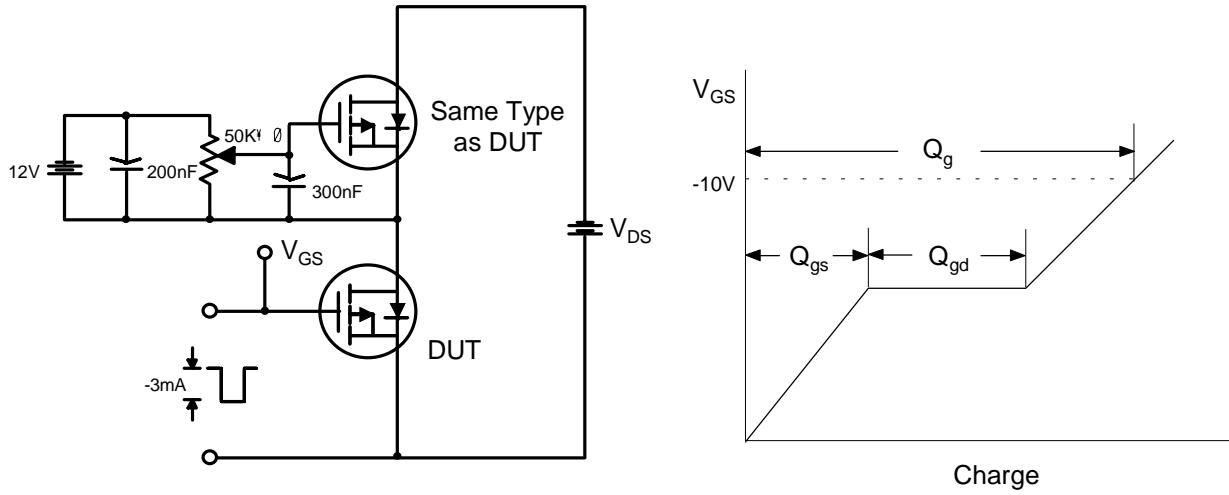


Fig 13. Resistive Switching Test Circuit & Waveforms

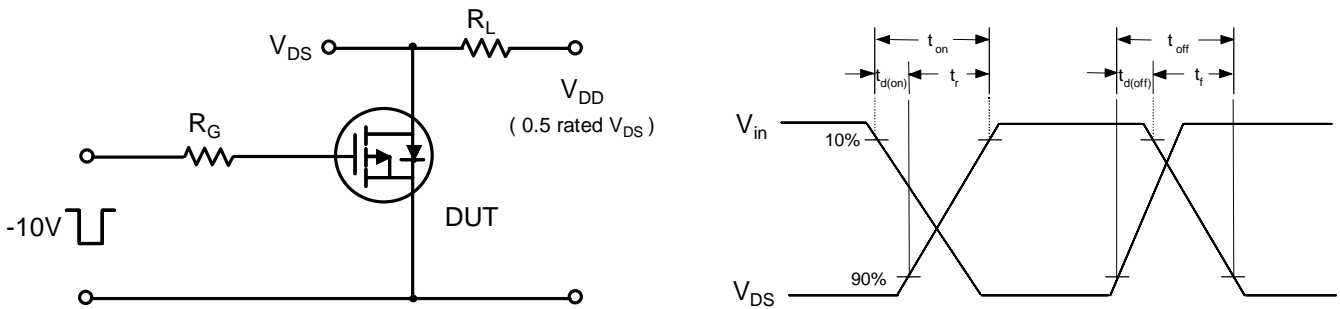


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

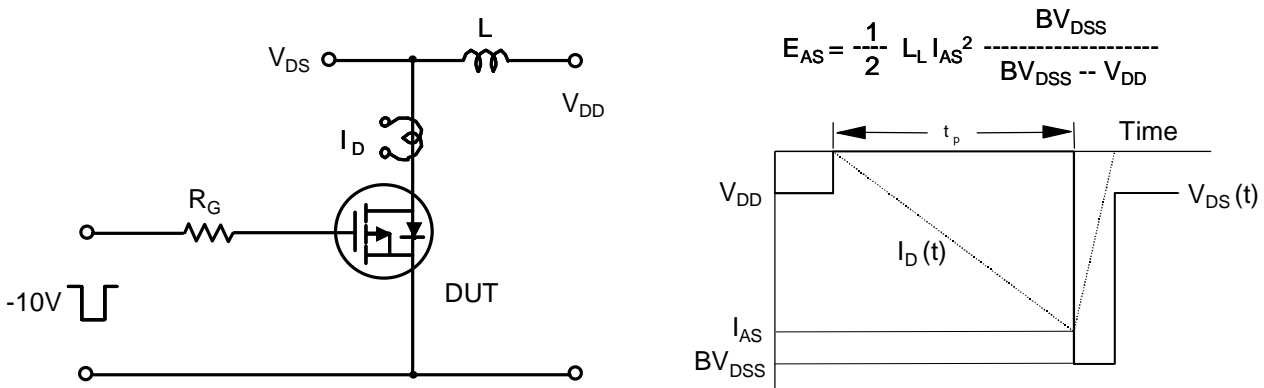
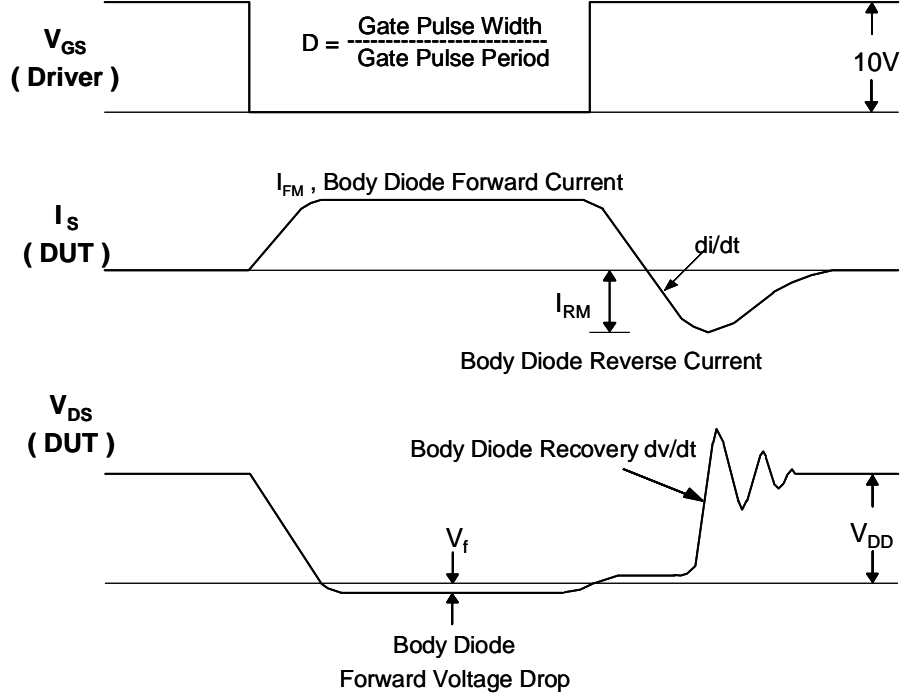
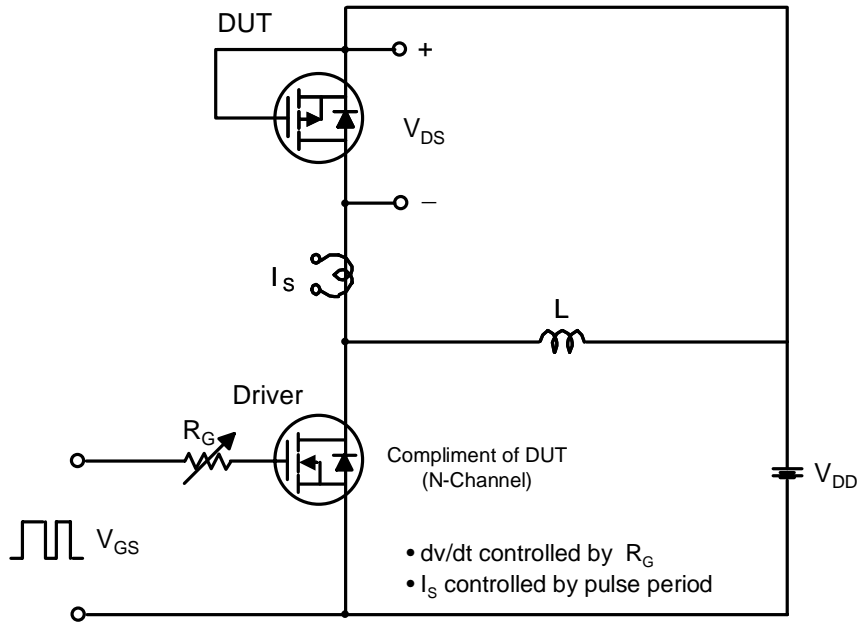
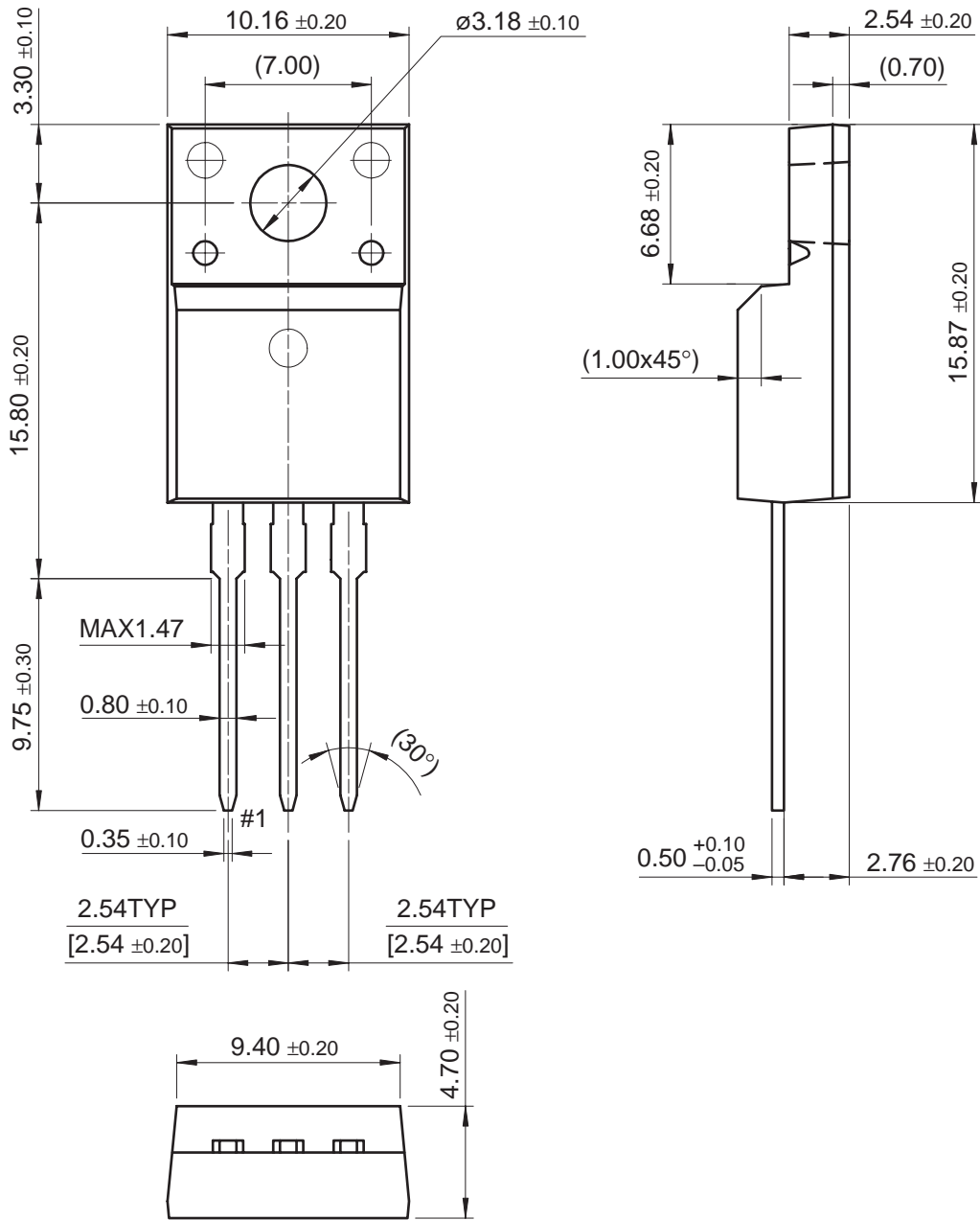


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



TO-220F Package Dimensions

TO-220F (FS PKG CODE AQ)



Dimensions in Millimeters

September 1999, Rev B

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