

# ML2021

## Telephone Line Equalizer

### Features

- Slope, height, and bandwidth adjustable
- Optimized group delays (500 Hz to 6.4 kHz)
- On chip anti-alias filter
- Bypass mode
- Low supply current 6 mA typical from  $\pm 5V$  supplies
- TTL / CMOS compatible interface
- Double buffered data latch
- Selectable master clock 1.544 or 1.536 MHz
- Synchronous or asynchronous data loading capability
- Compatible with ML2003 and ML2004 logarithmic gain/attenuator

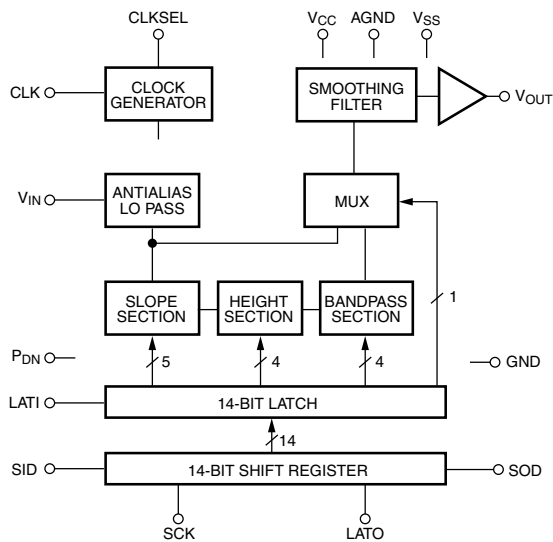
### General Description

The ML2021 is a monolithic analog line equalizer for telephone applications. The ML2021 consists of a switched capacitor filter that realizes a family of frequency response curves optimized for telephone line equalization while minimizing group delay.

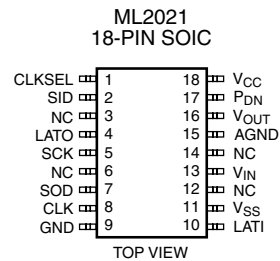
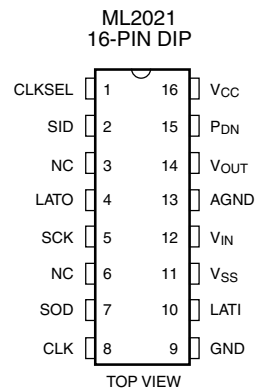
The ML2021 consists of a continuous anti-aliasing filter, three programmable switched capacitor equalization filters, an output smoothing filter, a  $600\Omega$  driver, and a digital section for the serial interface.

The equalization filters adjust the slope, height, and bandwidth of the frequency response. The desired frequency response is programmed by a digital 14-bit serial input data stream.

### Block Diagram



### Pin Connections



## Pin Description

Name	Function
CLKSEL	<b>Clock select input.</b> This pin selects the frequency of the CLK input. If CLK is 1.536 MHz, set CLKSEL = 1. If CLK is 1.544 MHz, set CLKSEL = 0. Pin has an internal pullup resistor to VCC.
SID	<b>Serial input data.</b> Digital input that contains serial data word which controls the filter frequency response setting.
LATO	<b>Output latch clock.</b> Digital input which loads the data word back into the shift register from the latch.
SCK	<b>Shift clock.</b> Digital input which shifts the serial data on SID into the shift register on rising edges and out onto SOD on falling edges.
SOD	<b>Serial output data.</b> Digital output of the shift register.
CLK	<b>Master clock input.</b> Digital input which generates clocks for the switched capacitor filters. Frequency can be either 1.544 MHz or 1.536 MHz.
GND	<b>Digital ground.</b> 0 volts. All digital inputs and output are referenced to this ground.
LATI	<b>Input latch clock.</b> Digital input which loads data from the shift register into the latch.
VSS	<b>Negative supply.</b> -5volts $\pm 10\%$ .
VIN	<b>Analog input.</b>
AGND	<b>Analog ground.</b> 0 volts. Analog input and output are referenced to this ground.
VOUT	<b>Analog output.</b>
PDN	<b>Powerdown input.</b> When P <sub>DN</sub> = 1, device is in powerdown mode. When P <sub>DN</sub> = 0, device is in normal operation. This pin has an internal pulldown resistor to GND.
VCC	<b>Positive supply.</b> 5 volts $\pm 10\%$

## Absolute Maximum Ratings<sup>1</sup>

Parameter	Min.	Max.	Units
Supply Voltage			
VCC		+6.5	V
VSS		-6.5	V
AGND with respect to GND		$\pm 0.5$	V
Analog Input and Output	VSS -0.3	VCC +0.3	V
Digital Input and Outputs	GND -0.3	VCC +0.3	V
Input Current Per Pin		$\pm 25$	mA
Power Dissipation		750	mW
Storage Temperature Range	-65	+150	°C
Lead Temperature (Soldering, 10 sec)		300	°C

## Operating Conditions

Parameter	Min.	Max.	Units
Temperature Range <sup>2</sup>			
ML2021CX	0	70	°C
ML2021IX	-40	85	°C
Supply Voltage			
VCC	4	6	V
VSS	-4	-6	V

### Electrical Characteristics

Unless otherwise specified  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = -5V \pm 10\%$ , Data Word:  $\overline{BP} = 1$ , Other Bits = 0,  $C_L = 100pF$ ,  $R_L = 600\Omega$ , dBm measurements use  $600\Omega$  as reference load,  $V_{IN} = -7dBm$ , 1kHz sinusoid  $CLK = 1.544 MHz \pm 300 Hz$  and digital time measured at 1.4 V

Symbol	Parameter	Notes	Conditions	Min	Typ. <sup>3</sup>	Max.	Units
<b>Analog</b>							
SR	Response, Slope Section	4	1 kHz response				
			<u>NL/L</u> <u>S3</u> <u>S2</u> <u>S1</u> <u>S0</u>				
			0 0 0 0 1			1.4 ±0.1	dB
			0 0 0 1 0			2.6 ±0.2	dB
			0 0 1 0 0			4.7 ±0.2	dB
			0 1 0 0 0			7.8 ±0.2	dB
			0 1 1 1 1			11.4 ±0.25	dB
			1 0 0 0 0			0 ±0.1	dB
			1 0 0 0 1			0.4 ±0.1	dB
			1 0 0 1 0			0.9 ±0.2	dB
			1 0 1 0 0			1.8 ±0.2	dB
			1 1 0 0 0			3.7 ±0.2	dB
			1 1 1 1 1			6.6 ±0.25	dB
			Referenced to				
			0 0 0 0 0				
HR	Response, Height Section	4	3250 Hz response referenced to 1 kHz response with $\overline{BP} = 1$ , other bits = 0				
			<u>NL/L</u> <u>H3</u> <u>H2</u> <u>H1</u> <u>H0</u>				
			0 0 0 0 0			0 ±0.15	dB
			0 0 0 0 1			0.5 ±0.2	dB
			0 0 0 1 0			1.1 ±0.2	dB
			0 0 1 0 0			2.3 ±0.2	dB
			0 1 0 0 0			5.7 ±0.3	dB
0 1 1 1 1			11.1 ±0.3	dB			
BR	Response, Bandwidth Section (Q)	4	<u>NL/L</u> <u>B3</u> <u>B2</u> <u>B1</u> <u>B0</u> <u>H3</u> <u>H2</u> <u>H1</u> <u>H0</u>				
			0 0 0 0 0 1 1 1 1			16.1 ±2.0	
			0 0 0 0 1 1 1 1 1			14.2 ±1.5	
			0 0 0 1 0 1 1 1 1			12.6 ±1.5	
			0 0 1 0 0 1 1 1 1			9.1 ±1.0	
			0 1 0 0 0 1 1 1 1			3.6 ±0.5	
			0 1 1 1 1 1 1 1 1			1.2 ±0.35	
PK	BW Peak Frequency	4	H3 thru H0 = 1	3230	3250	3270	Hz
AG	Absolute Gain, Flat Response	4	0.5 kHz to 4 kHz	-0.1	+0.1	+0.3	dB
AGB	Absolute Gain, Bypass Mode	4	0.3 kHz to 4 kHz, $\overline{BP} = 0$	-0.1	+0.1	+0.3	dB
ICN	Idle Channel Noise	4	$V_{IN} = 0$		3	8	dBrc
			$V_{IN} = 0$ , All Data Bits = 1		9		dBrc
HD	Harmonic Distortion	4	$V_{IN} = 5 dBm$ , 1 kHz Measure 2nd, 3rd, harmonic relative to fundamental			-48	dB
SD	Signal to Distortion	4	$V_{IN} = -12dBm$ , 1 kHz C msg weighted	+48			dB
SFN	Signal Frequency Noise	5	$V_{IN} = 0$ , 4 kHz ≤ frequency ≤ 150 kHz			-50	dBm
PSRR	Power Supply Rejection	4	200mVp-p, 1 kHz sine, $V_{IN} = 0$ on $V_{CC}$			-40	dB
			on $V_{SS}$			-40	dB

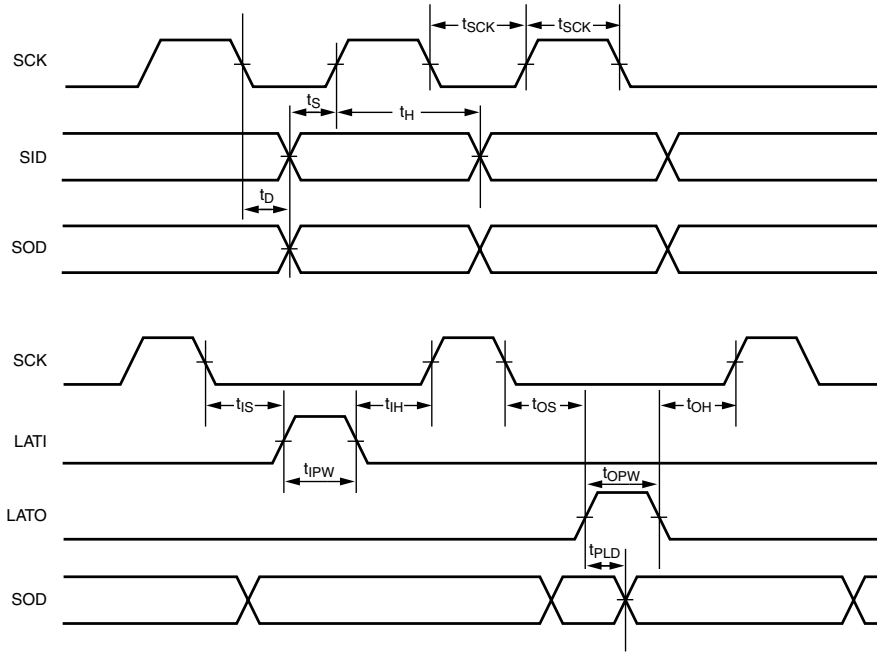
**Electrical Characteristics** (continued)

Unless otherwise specified  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = -5V \pm 10\%$ , Data Word:  $\overline{BP} = 1$ , Other Bits = 0,  $C_L = 100pF$ ,  $R_L = 600\Omega$ , dBm measurements use  $600\Omega$  as reference load,  $V_{IN} = -7dBm$ , 1kHz sinusoid CLK =  $1.544 MHz \pm 300 Hz$  and digital time measured at 1.4 V

Symbol	Parameter	Notes	Conditions	Min	Typ. <sup>3</sup>	Max.	Units
Z <sub>IN</sub>	Input Impedance, V <sub>IN</sub>	4		100			k $\Omega$
V <sub>OS</sub>	Output Offset Voltage	4	V <sub>IN</sub> = 0			±50	mV
V <sub>INR</sub>	Input Voltage Range	4		±2.0			V
V <sub>OSW</sub>	Output Voltage Swing	4	R <sub>L</sub> = 600 $\Omega$	±2.0			V
<b>Digital and DC</b>							
V <sub>IL</sub>	Digital Input Low Voltage	4				0.8	V
V <sub>IH</sub>	Digital Input High Voltage	4		2.0			V
V <sub>OL</sub>	Digital Output Low Voltage	4	I <sub>OL</sub> = 2mA			0.4	V
V <sub>OH</sub>	Digital Output High Voltage	4	I <sub>OH</sub> = -1mA	4.0			V
I <sub>LCLK</sub>	Input Current, CLK SEL	4	V <sub>IN</sub> = 0	5		100	$\mu A$
I <sub>LPDN</sub>	Input Current, PDN	4	V <sub>IN</sub> = V <sub>CC</sub>	-3		-100	$\mu A$
I <sub>L</sub>	Input Current, All Other Inputs	4	V <sub>IN</sub> = 0 to V <sub>CC</sub>			±10	$\mu A$
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	4	No output load, V <sub>IL</sub> = GND, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IN</sub> = 0			10	mA
I <sub>SS</sub>	V <sub>SS</sub> Supply Current	4	No output load, V <sub>IL</sub> = GND, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IN</sub> = 0			-10	mA
I <sub>CCP</sub>	V <sub>CC</sub> Supply Current, Powerdown Mode	4	No output load, V <sub>IL</sub> = GND, V <sub>IH</sub> = V <sub>CC</sub>			1.2	mA
I <sub>SSP</sub>	V <sub>SS</sub> Supply Current, Powerdown Mode	4	No output load, V <sub>IL</sub> = GND, V <sub>IH</sub> = V <sub>CC</sub>			-1.2	mA
<b>AC Characteristics</b>							
t <sub>DC</sub>	Clock Duty Cycle	5		40		60	%
t <sub>SCK</sub>	SCK On/Off Period	4		250			ns
t <sub>S</sub>	SID Data Setup Time	4		50			ns
t <sub>H</sub>	SID Data Hold Time	4		50			ns
t <sub>D</sub>	SOD Data Delay	4		0		125	ns
t <sub>IPW</sub>	LATI Pulse Width	4		50			ns
t <sub>OPW</sub>	LATO Pulse Width	4		50			ns
t <sub>IS</sub> , t <sub>OS</sub>	LATI, LATO Setup Time	4		50			ns
t <sub>IH</sub> , t <sub>OH</sub>	LATI, LATO Hold Time	5		50			ns
t <sub>PLD</sub>	SOD Parallel Load Delay	4		0		125	ns

**Notes**

1. Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
2. 0°C to +70°C and -40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.
3. Typicals are parametric norm at 25°C.
4. Parameter guaranteed and 100% production tested.
5. Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.



TIMING PARAMETERS ARE REFERENCED TO THE 1.4 VOLT MIDPOINT.

Figure 1. Serial Timing Diagram

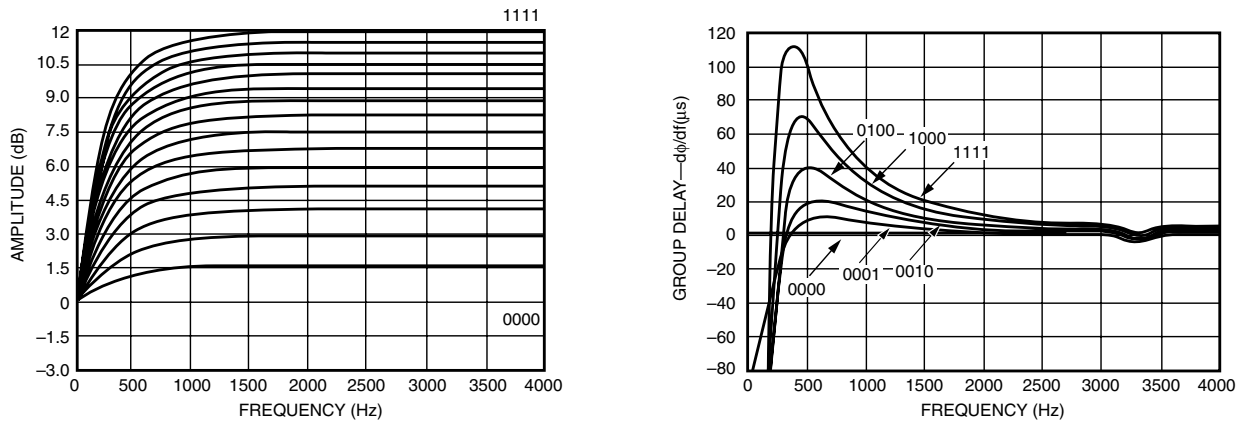
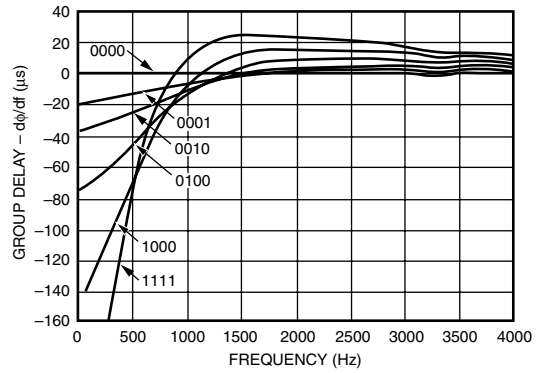
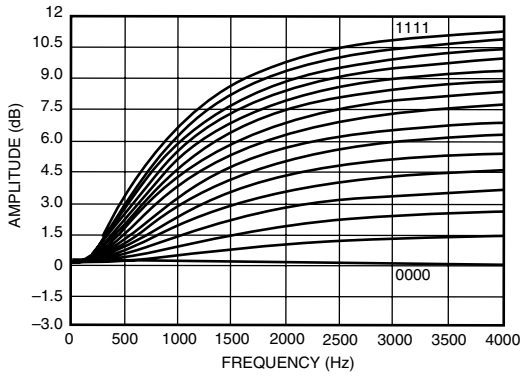
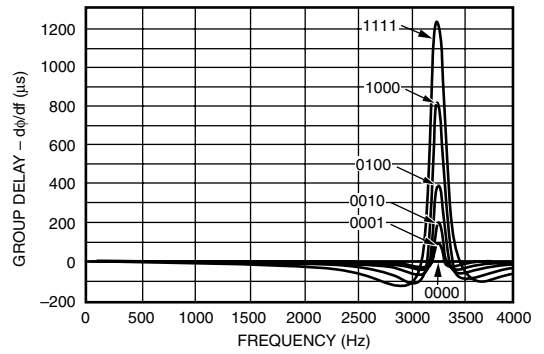
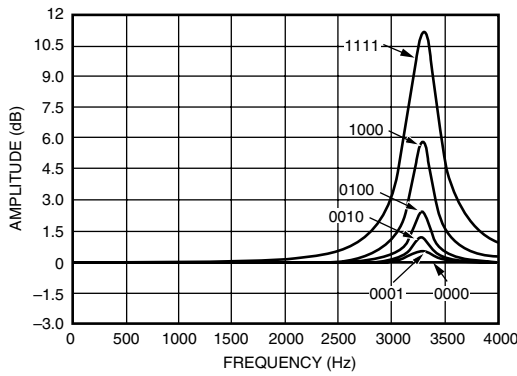


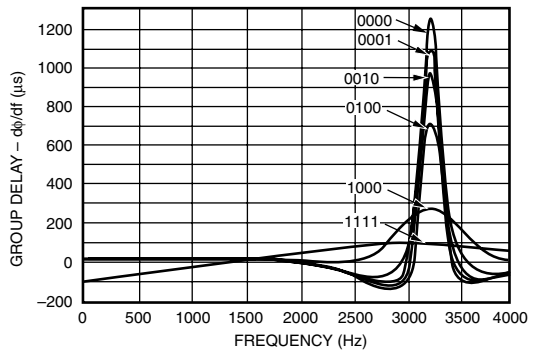
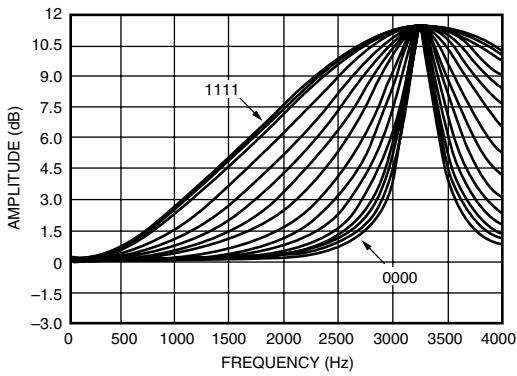
Figure 2. Typical Slope Filter Response—NL/L = 0  
B3-B0, H3-H0 = 0000, S3-S0 = 0000 to 1111.



**Figure 3. Typical Slope Filter Response—NL/L = 1  
B3-B0, H3-H0 = 0000, S3-S0 = 0000 to 1111.**



**Figure 4. Typical Height Filter Response—NL/L = 0  
B3-B0, S3-S0 = 0000, H3-H0 = 0000 to 1111.**



**Figure 5. Typical Bandwidth Filter Response—NL/L = 0  
H3-H0 = 1111; S3-S0 = 0000; B3-B0 = 0000 to 1111.**

## Functional Description

The ML2021 consists of a continuous anti-alias filter, three programmable switched capacitor equalization filters, an output smoothing filter, an output driver, and a digital section for the serial interface.

### Anti-Alias Filter

The first section is a continuous anti-alias filter. This filter is needed to prevent aliasing of high frequency signal present on the input into the passband by the sampling action of the switched capacitor filters. This section is a continuous second order lowpass filter with a typical 3 dB frequency at 20 kHz and 30 dB of rejection at 124 kHz.

### Equalization Filters

The programmable filters implement a family of frequency response curves intended to compensate for the response of telephone lines.

This filter is composed of three distinct sections: slope, height, and bandwidth.

### Response of Slope, Height, and Bandwidth

The family of response curves generated by the slope section are shown in Figures 2 and 3. There are 4 slope select bits, S3-S0. These bits alter the slope of the highpass response under 1000Hz, and as a result, the absolute gain above 1000 Hz will be unique for each setting. Table 1 gives typical 1 kHz gain values for all slope settings.

Table 1. Typ. 1kHz Gain for Slope Settings

Slope Setting	Rel 1kHz Gain (dB)	
	NL/L = 1	NL/L = 0
0	0.0	REL
1	0.4	1.4
2	0.9	2.6
3	1.4	3.7
4	1.8	4.7
5	2.3	5.5
6	2.8	6.3
7	3.4	7.2
8	3.7	7.8
9	4.2	8.4
10	4.6	9.0
11	5.0	9.5
12	5.4	10.0
13	5.8	10.5
14	6.2	11.0
15	6.6	11.4

HT, BW Bits = 0

There is an additional bit, NL/L, that also affects the high-pass response of the slope filter. The slope response curves in Figure 2 are with NL/L = 0. These same response curves are shown in Figure 3 with NL/L = 1. Notice that the NL/L bit adds more droop in the highpass response below 2500 Hz.

The family of response curves generated by the height section are shown in Figure 4. There are 4 height select bits, H3-H0. This section creates a peak in the response at 3250 Hz and this filter controls the amount of peaking. Table 2 gives typical 1 kHz gain values for all height and bandwidth settings.

Table 2. Typ. 1kHz Gain for HT and BW Settings

		Relative 1kHz Gain (dB)															
		HT Setting															
BW Setting		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0	0	Rel	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0.1
5		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0.1	0.1
6		0	0	0	0	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.1
7		0	0	0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.1	0.2	0.2
8		0	0	0	0	0	0	0.1	0.1	0.1	0.1	0.1	0.1	0.2	0.2	0.3	0.3
9		0	0	0	0	0	0.1	0.1	0.1	0.1	0.2	0.2	0.3	0.3	0.4	0.5	0.6
10		0	0	0	0	0.1	0.1	0.1	0.1	0.2	0.3	0.3	0.4	0.5	0.6	0.7	0.8
11		0	0	0	0.1	0.1	0.1	0.1	0.2	0.2	0.3	0.4	0.4	0.5	0.7	0.8	0.9
12		0	0	0.1	0.1	0.1	0.2	0.2	0.3	0.4	0.5	0.7	0.8	1.0	1.1	1.4	1.6
13		0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.6	0.8	0.9	1.1	1.4	1.6	1.9	2.3
14		0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.7	0.8	1.0	1.2	1.5	1.7	2.0	2.4
15		0	0	0.1	0.1	0.2	0.3	0.4	0.5	0.7	0.9	1.1	1.3	1.6	1.8	2.1	2.5

Slope Bits = 0

The family of response curves generated by the bandwidth section is shown in Figure 5. There are 4 bandwidth select bits, B3-B0. This section causes the response of the 3250 Hz peak to be widened, and as a result, this filter controls the bandwidth of the 3250 Hz peaked region.

### Transfer Function

The transfer function for the ML2021 is shown below. This transfer function is valid for magnitude response only. The actual magnitude response from an individual device may deviate from the computed response from the transfer function by typically 0–0.2 dB.

$$H(s) = \frac{c(s+b)}{b(s+c)} \times \frac{[s^2 + h(\omega_o/Q)s + \omega_o^2]}{[s^2 + (\omega_o/Q)s + \omega_o^2]} \times \frac{[\sin(\pi f/fc)]}{(\pi f/fc)}$$

$$s = j \times 256000 \times \tan(\pi f/128000)$$

$$\omega_o = 20463.77$$

$$fc = 128000$$

$$b, c : \text{ See Table 3. (slope)}$$

$$Q : \text{ See Table 4. (bandwidth)}$$

$$h : \text{ See Table 5. (height)}$$

Table 3. Slope Response Factors (b,c)

S3-0	b NL/L = 0	b NL/L = 1
0000	2.371759E +03	1.116280E + 04
0001	1.985920E + 03	9.345141E + 03
0010	1.701779E + 03	8.007156E + 03
0011	1.493571E + 03	7.026999E + 03
0100	1.326721E + 03	6.241681E + 03
0101	1.196668E + 03	5.629636E + 03
0110	1.087277E + 03	5.114881E + 03
0111	9.983588E + 02	4.696487E + 03
1000	9.179889E + 02	4.318339E + 03
1001	8.537864E + 02	4.016273E + 03
1010	7.966049E + 02	3.747249E + 03
1011	7.478074E + 02	3.517676E + 03
1100	7.035099E + 02	3.309279E + 03
1101	6.651771E + 02	3.128945E + 03
1110	6.299477E + 02	2.963214E + 03
1111	5.990361E + 02	2.817797E + 03
S3-0	c NL/L = 0	c NL/L = 1
XXXX	2.371759E + 03	1.116280E + 04

Table 4. Slope Response factors (b,c)

B3-0	Q
0000	17.444906
0001	15.386148
0010	13.652451
0011	11.593677
0100	9.859960
0101	8.017864
0110	6.392453
0111	5.092080
1000	3.900003
1001	3.141338
1010	2.599369
1011	2.165724
1100	1.731965
1101	1.406509
1110	1.352248
1111	1.297981

Table 5. Height Response Factors (h)

Code	h
0000	1.000000
0001	1.071519
0010	1.148154
0011	1.230269
0100	1.318257
0101	1.445438
0110	1.603245
0111	1.757924
1000	1.949845
1001	2.137962
1010	2.317395
1011	2.540973
1100	2.786121
1101	3.019951
1110	3.311311
1111	3.672823

### Group Delay

The difference between the ML2020 and ML2021 is the elimination of a 60 Hz highpass filter in order to eliminate positive group delay at low frequency.

The group delay through the ML2021 can be minimized such that less than 50 $\mu$ s of group delay can be achieved in both unloaded and cable loaded conditions relative to 1804 Hz in the frequency range of 504 to 3004Hz. Minimum group delays are dependant upon using the proper setting for slope, height, and bandwidth for a give equalization requirement.

### Smoothing Filter

The equalizer filters are followed by a continuous second order smoothing filter that removes the high frequency sample information generated by the action of the switched capacitor filters. This filter provides a continuous analog signal at the output, VOUT.

### Output Buffer

The final stage in the ML2021 is the output buffer. This amplifier has internal gain of 1 and is capable of driving 600 $\Omega$ , 100pF loads. Thus, it is suitable for driving telephone hybrids directly without any external amplifier.

### Bypass Mode

The filter sections can be bypassed by setting the bypass data bit, BP, to 0. Since the switched capacitor filters are bypassed in this mode, frequency response effects of the switched capacitor filters are eliminated. Thus, this mode offers very flat response and low noise over the 300-4000 Hz frequency range.

### Filter Clock

The master clock, CLK, is used to generate the internal clocks for the switched capacitor filters. The frequency of CLK can be either 1.544 MHz or 1.536 MHz. However, the internal clock frequency must be kept at 1.536 MHz to guarantee accurate frequency response. The CLKSEL pin enables a bit swallower circuit to keep the internal clock frequency set to 1.536 MHz. When 1.544 MHz clock is used, CLKSEL should be set to logic level 0, and one bit out of every 193 bits is removed (swallowed) to reduce the internal frequency to 1.536 MHz. When 1.536 MHz clock is used, CLKSEL should be set to logic level 1, and the internal clock rate is the same as the external clock rate.

### Serial Interface

The architecture of the digital section is shown in the preceding block diagram.

A timing diagram for the serial interface is shown in Figure 6. The serial input data, SID, is loaded into a shift register on rising edges of the shift clock, SCK. The data word is parallel loaded into a latch when the input latch signal, LATI, is



high. The LATI pulse must occur when SCK is low. A new data word can be loaded into the shift register without disturbing the existing data word in the latch.

The parallel outputs of the latch control the filter response curves. The order of the data word bits in the latch is shown in Figure 7.

Note that bit 0 is the first bit of the data word clocked into the shift register.

The device has the capability to read out the data word stored in the latch. This is done by parallel loading the data from the latch back into the shift register when the latch signal, LATO, is high. The LATO pulse must occur when SCK is low. Then, the data word can be shifted out of the register

serially to the output, SOD, on falling edges of the shift clock, SCK.

The loading and reading of the data word can be done continuously or in bursts. Since the shift register and latch circuitry inside the device is static, there are no minimum frequency requirements on the clocks or data pulses. However, there is some coupling of the digital signals in the analog section. If this coupling is undesirable, the data can be clocked in bursts during non critical intervals, or the data rate can be done at a frequency outside the analog frequency range.

The clocks used to shift and latch data (SCK, LATI, LATO) are not related internally to the master clock and can occur asynchronous to CLK.

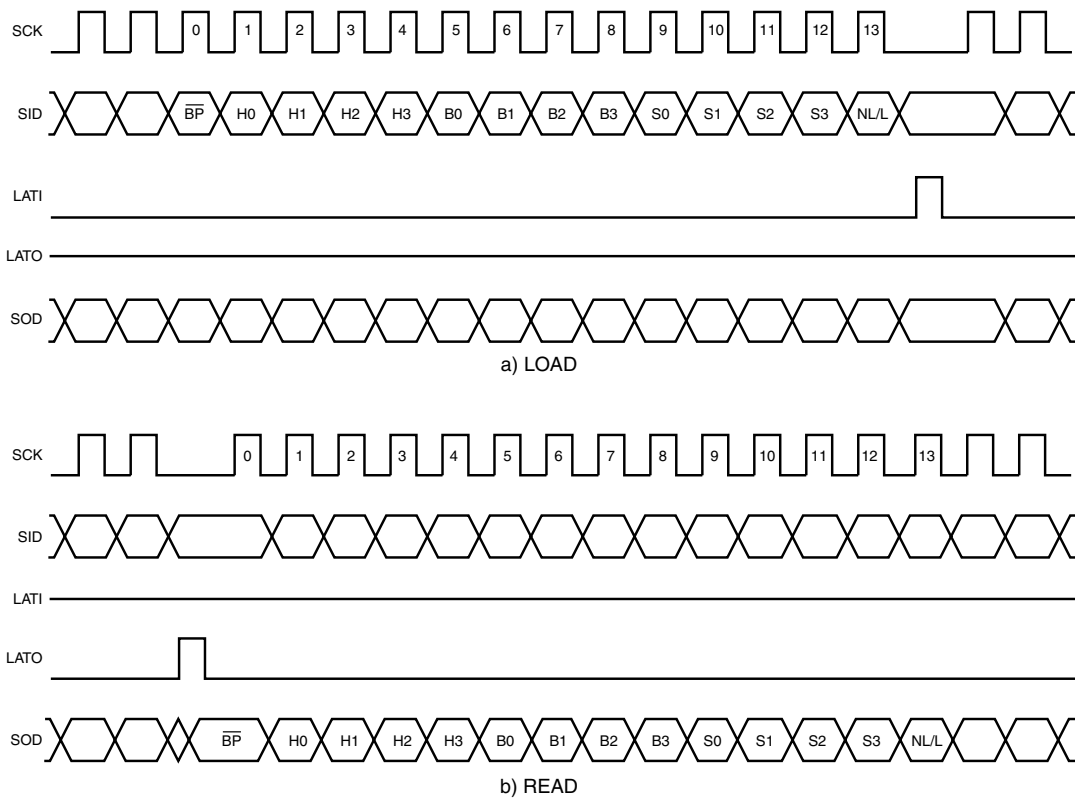


Figure 6. Serial Timing

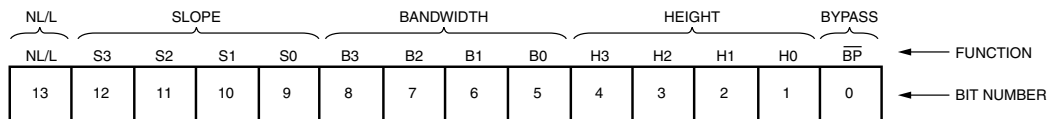


Figure 7. 14-Bit Latch

### Powerdown Mode

A powerdown mode can be selected with pin PDN. When PDN = 1, the device is powered down. In this state, the power consumption is reduced by removing power from the analog section and forcing the analog output, VOUT, to a high impedance state. While the device is in power down mode, the digital section is still functional and the current data word remains stored in the latch. The master clock, CLK, can be left active or removed during powerdown mode. When PDN = 0, the device is in normal operation.

### Power Supplies

The digital section inside the device is powered between VCC and GND, or 5 volts. The analog section is powered between VCC and VSS, or ±5 volts. The analog section uses AGND as the reference point.

GND and AGND are totally isolated inside the device to minimize coupling from the digital section into the analog section. Typically this is less than 100 μV. However, ANGD and GND should be tied together physically near the device and close to the common power supply ground connection.

The power supply rejection of VCC and VSS to the analog output is greater than -60dB at 1 kHz, typically. If decoupling of the power supplies is still necessary in a system, VCC and VSS should be decoupled with respect to AGND.

## Applications

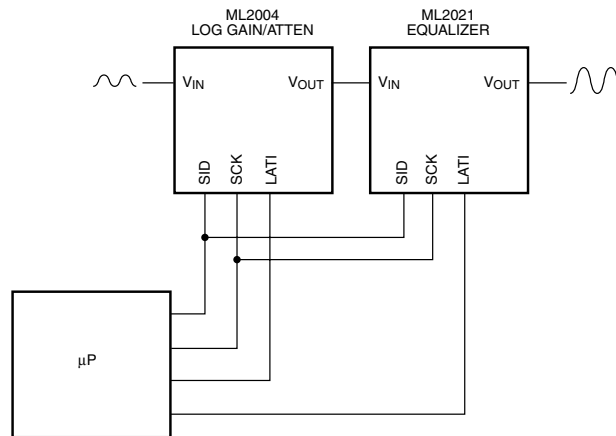


Figure 8. Typical Serial Interface

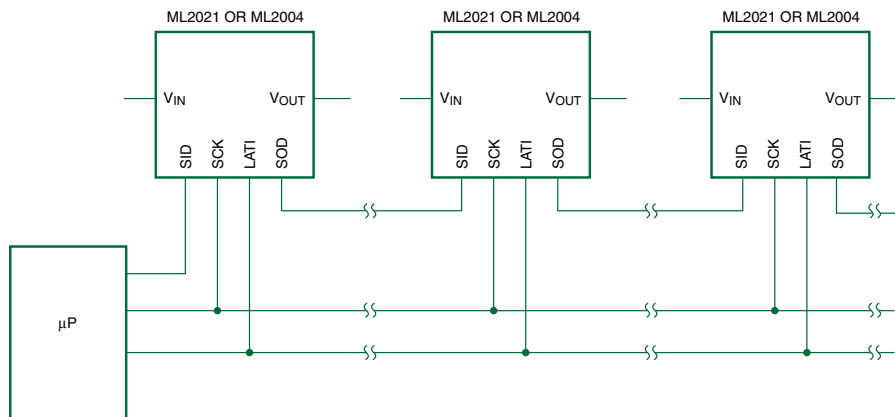


Figure 9. Controlling Multiple ML2021 and ML2024 With Only 3 Digital Lines Using One Long Data Word

## Ordering Information

Part Number	Temperature Range	Package
ML2021CP	0°C to 70°C	Molded DIP (P16)
ML2021CS	0°C to 70°C	Molded SOIC (S18)
ML2021IP	-40°C to 85°C	Molded DIP (P16)
ML2021IS	-40°C to 85°C	Molded SOIC (S18)

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