

# ML4827

## Fault-Protected PFC and PWM Controller Combo

### Features

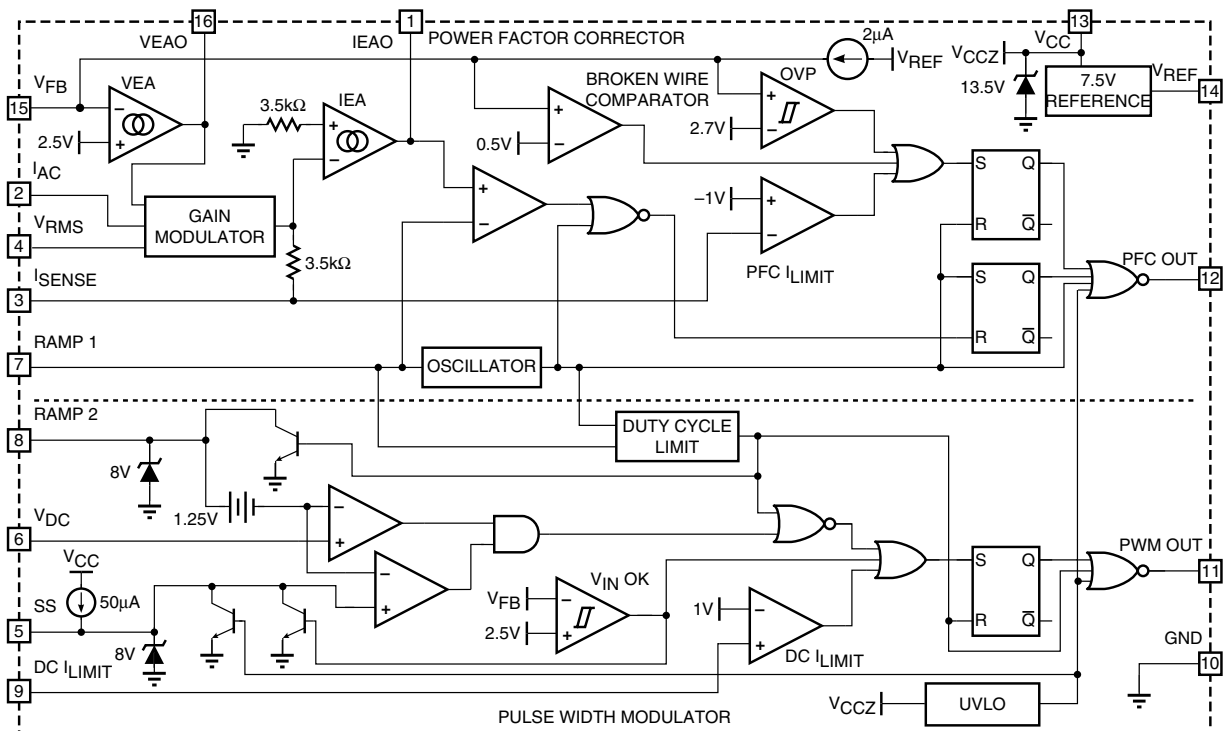
- Pin-compatible with industry-standard ML4824-1
- TriFault Detect™ to conform to UL1950™ requirements
- Available in 50% or 74% max duty cycle versions
- Low total harmonic distortion
- Reduces ripple current in the storage capacitor between the PFC and PWM sections
- Average current, continuous boost leading edge PFC
- High efficiency trailing-edge PWM can be configured for current mode or voltage mode operation
- Average line voltage compensation with brown-out control
- PFC overvoltage comparator eliminates output “runaway” due to load removal
- Current fed gain modulator for improved noise immunity
- Overvoltage protection, UVLO, and soft start

### General Description

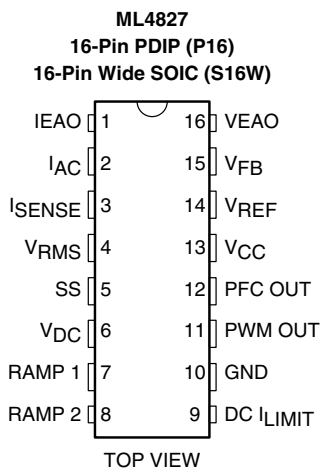
The ML4827 is a controller for power factor corrected, switched mode power supplies, that includes circuitry

necessary for conformance to the safety requirements of UL1950. A direct descendent of the industry-standard ML4824-1, the ML4827 adds a TriFault Detect™ function to guarantee that no unsafe conditions may result from single component failure in the PFC. Power Factor Correction (PFC) allows the use of smaller, lower cost bulk capacitors, reduces power line loading and stress on the switching FETs, and results in a power supply that fully complies with IEC1000-3-2 specification. The ML4827 includes circuits for the implementation of a leading edge, average current, “boost” type power factor correction and a trailing edge, pulse width modulator (PWM). The device is available in two versions; the ML4827-1 (Duty Cycle<sub>MAX</sub> = 50%) and the ML4827-2 (Duty Cycle<sub>MAX</sub> = 74%). The higher maximum duty cycle of the -2 allows enhanced utilization of a given transformer core’s power handling capacity. An overvoltage comparator shuts down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting and input voltage brown-out protection. The PWM section can be operated in current or voltage mode, and includes a duty cycle limit to prevent transformer saturation.

### Block Diagram



## Pin Configuration



## Pin Description

PIN	NAME	FUNCTION
1	IEAO	PFC transconductance current error amplifier output
2	IAC	PFC gain control reference input
3	ISENSE	Current sense input to the PFC current limit comparator
4	VRMS	Input for PFC RMS line voltage compensation
5	SS	Connection point for the PWM soft start capacitor
6	VDC	PWM voltage feedback input
7	RAMP 1	PFC (master) oscillator input; fOSC set by RTCT
8	RAMP 2	When in current mode, this pin functions as as the current sense input; when in voltage mode, it is the PWM (slave) oscillator input.
9	DC ILIMIT	PWM current limit comparator input
10	GND	Ground
11	PWM OUT	PWM driver output
12	PFC OUT	PFC driver output
13	VCC	Positive supply (connected to an internal shunt regulator)
14	VREF	Buffered output for the internal 7.5V reference
15	VFB	PFC transconductance voltage error amplifier input, and TriFault Detect input
16	VEAO	PFC transconductance voltage error amplifier output

## Absolute Maximum Ratings

Absolute Maximum Ratings are those values, beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Parameter	Min.	Max.	Units
VCC Shunt Regulator Current		55	mA
ISENSE Voltage	-3	5	V
Voltage on any other Pin	GND-0.3	VCCZ +0.3	V
IREF		20	mA
IAC Input Current		10	mA

Peak PFC OUT Current, Source or Sink		500	mA
Peak PWM OUT Current, Source or Sink		500	mA
PFC OUT, PWM OUT Energy Per Cycle		1.5	μJ
Junction Temperature		150	°C
Storage Temperature Range	-65	150	°C
Lead Temperature (soldering, 10s)		260	°C
Thermal Resistance (θ <sub>JA</sub> )			
Plastic DIP		80	°C/W
Plastic SOIC		105	°C/W

## Operating Conditions

Parameter	Min.	Max.	Units
Temperature Range			
ML4827CP, CS	0	70	°C
ML4827IP, IS	-40	85	°C

## Electrical Characteristics

Unless otherwise specified, I<sub>CC</sub> = 25mA, R<sub>T</sub> = 21.8kΩ, C<sub>T</sub> = 1000pF, T<sub>A</sub> = Operating Temperature Range (Note 1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Voltage Error Amplifier</b>						
	Input Voltage Range		0		7	V
	Transconductance	V <sub>NON INV</sub> = V <sub>INV</sub> , V <sub>EAO</sub> = 3.75V	50	85	120	μΩ
	Feedback Reference Voltage		2.48	2.55	2.62	V
	Input Bias Current	Note 2		-1	-2	μA
	Output High Voltage		6.0	6.7		V
	Output Low Voltage			0.6	1.0	V
	Source Current	ΔV <sub>IN</sub> = ±0.5V, V <sub>OUT</sub> = 6V	-40	-80		μA
	Sink Current	ΔV <sub>IN</sub> = ±0.5V, V <sub>OUT</sub> = 1.5V	40	80		μA
	Open Loop Gain		60	75		dB
	Power Supply Rejection Ratio	V <sub>CCZ</sub> - 3V < V <sub>CC</sub> < V <sub>CCZ</sub> - 0.5V	60	75		dB
<b>Current Error Amplifier</b>						
	Input Voltage Range		-1.5		2	V
	Transconductance	V <sub>NON INV</sub> = V <sub>INV</sub> , V <sub>EAO</sub> = 3.75V	130	195	310	μΩ
	Input Offset Voltage		2	10	17	mV
	Input Bias Current			-0.5	-1.0	μA
	Output High Voltage		6.0	6.7		V
	Output Low Voltage			0.6	1.0	V
	Source Current	ΔV <sub>IN</sub> = ±0.5V, V <sub>OUT</sub> = 6V	-40	-90		μA
	Sink Current	ΔV <sub>IN</sub> = ±0.5V, V <sub>OUT</sub> = 1.5V	40	90		μA
	Open Loop Gain		60	75		dB
	Power Supply Rejection Ratio	V <sub>CCZ</sub> - 3V < V <sub>CC</sub> < V <sub>CCZ</sub> - 0.5V	60	75		dB
<b>OVP Comparator</b>						
	Threshold Voltage		2.6	2.7	2.8	V
	Hysteresis		80	115	150	mV

**Electrical Characteristics** (Continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Tri-Fault Detect</b>						
	Fault Detect HIGH		2.6	2.7	2.8	V
	Time to Fault Detect HIGH	$V_{FB} = V_{FAULT\ DETECT\ LOW}$ to $V_{FB} = OPEN$ 1nF from $V_{FB}$ to GND		1	2	ms
	Fault Detect LOW		0.4	0.5	0.6	V
<b>PFC I<sub>LIMIT</sub> Comparator</b>						
	Threshold Voltage		-0.8	-1.0	-1.15	V
	$\Delta(PFC\ I_{LIMIT}\ V_{TH} - \text{Gain Modulator Output})$		100	190		mV
	Delay to Output			150	300	ns
<b>DC I<sub>LIMIT</sub> Comparator</b>						
	Threshold Voltage		0.9	1.0	1.1	V
	Input Bias Current			$\pm 0.3$	$\pm 1$	$\mu A$
	Delay to Output			150	300	ns
<b>V<sub>IN</sub> OK Comparator</b>						
	Threshold Voltage		2.45	2.55	2.65	V
	Hysteresis		0.8	1.0	1.2	V
<b>Gain Modulator</b>						
	Gain (Note 3)	$I_{AC} = 100\mu A, V_{RMS} = V_{FB} = 0V$	0.36	0.55	0.66	
		$I_{AC} = 50\mu A, V_{RMS} = 1.2V, V_{FB} = 0V$	1.20	1.80	2.24	
		$I_{AC} = 50\mu A, V_{RMS} = 1.8V, V_{FB} = 0V$	0.55	0.80	1.01	
		$I_{AC} = 100\mu A, V_{RMS} = 3.3V, V_{FB} = 0V$	0.14	0.20	0.26	
	Bandwidth	$I_{AC} = 100\mu A$		10		MHz
	Output Voltage	$I_{AC} = 250\mu A, V_{RMS} = 1.15V, V_{FB} = 0V$	0.74	0.82	0.90	V
<b>Oscillator</b>						
	Initial Accuracy	$T_A = 25^\circ C$	75	80	85	kHz
	Voltage Stability	$V_{CCZ} - 3V < V_{CC} < V_{CCZ} - 0.5V$		1		%
	Temperature Stability			2		%
	Total Variation	Line, Temp	72		88	kHz
	Ramp Valley to Peak Voltage			2.5		V
	Dead Time	PFC Only	450	600	750	ns
	C <sub>T</sub> Discharge Current	$V_{RAMP\ 2} = 0V, V_{RAMP\ 1} = 2.5V$	4.5	7.5	9.5	mA
<b>Reference</b>						
	Output Voltage	$T_A = 25^\circ C, I(V_{REF}) = 1mA$	7.4	7.5	7.6	V
	Line Regulation	$V_{CCZ} - 3V < V_{CC} < V_{CCZ} - 0.5V$		2	10	mV
	Load Regulation	$1mA < I(V_{REF}) < 20mA$		2	15	mV
	Temperature Stability			0.4		%
	Total Variation	Line, Load, Temp	7.35		7.65	V
	Long Term Stability	$T_J = 125^\circ C, 1000\ \text{Hours}$		5	25	mV

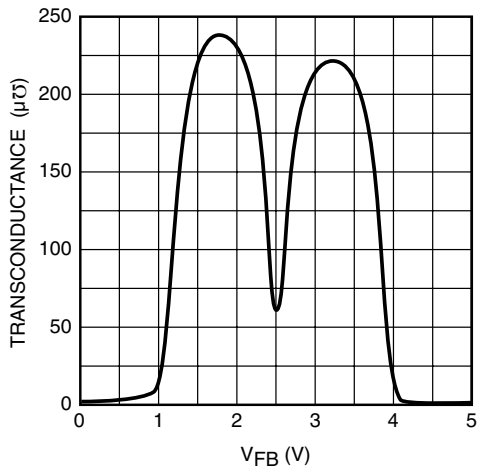
**Electrical Characteristics** (Continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>PFC</b>						
	Minimum Duty Cycle	VIEAO > 4.0V			0	%
	Maximum Duty Cycle	VIEAO < 1.2V	90	95		%
	Output Low Voltage	IOUT = -20mA		0.4	0.8	V
		IOUT = -100mA		0.8	2.0	V
		IOUT = 10mA, VCC = 8V		0.7	1.5	V
	Output High Voltage	IOUT = 20mA	10	10.5		V
		IOUT = 100mA	9.5	10		V
	Rise/Fall Time	CL = 1000pF		50		ns
<b>PWM</b>						
	Duty Cycle Range	ML4827-1	0-44	0-47	0-50	%
		ML4827-2	0-64	0-70	0-74	%
	Output Low Voltage	IOUT = -20mA		0.4	0.8	V
		IOUT = -100mA		0.8	2.0	V
		IOUT = 10mA, VCC = 8V		0.7	1.5	V
	Output High Voltage	IOUT = 20mA	10	10.5		V
		IOUT = 100mA	9.5	10		V
	Rise/Fall Time	CL = 1000pF		50		ns
<b>Supply</b>						
	Shunt Regulator Voltage (VCCZ)		12.8	13.5	14.2	V
	VCCZ Load Regulation	25mA < ICC < 55mA		±100	±300	mV
	VCCZ Total Variation	Load, Temp	12.4		14.6	V
	Start-up Current	VCC = 11.8V, CL = 0		0.7	1.0	mA
	Operating Current	VCC < VCCZ - 0.5V, CL = 0		16	19	mA
	Undervoltage Lockout Threshold		12	13	14	V
	Undervoltage Lockout Hysteresis		2.7	3.0	3.3	V

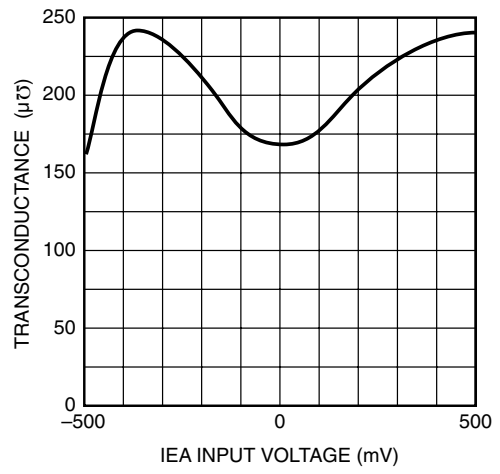
**Notes:**

- Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
- Includes all bias currents to other circuits connected to the VFB pin.
- Gain =  $K \times 5.3V$ ;  $K = (I_{GAINMOD} - I_{OFFSET}) \times I_{AC} \times (V_{EAO} - 1.5V)^{-1}$ .

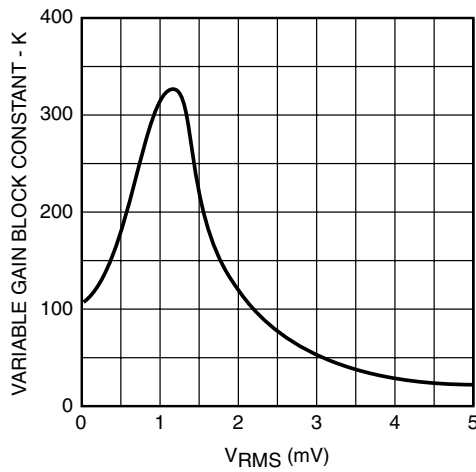
### Typical Performance



Voltage Error Amplifier (VEA) Transconductance ( $g_m$ )



Current Error Amplifier (IEA) Transconductance ( $g_m$ )



Gain Modulator Transfer Characteristic (K)

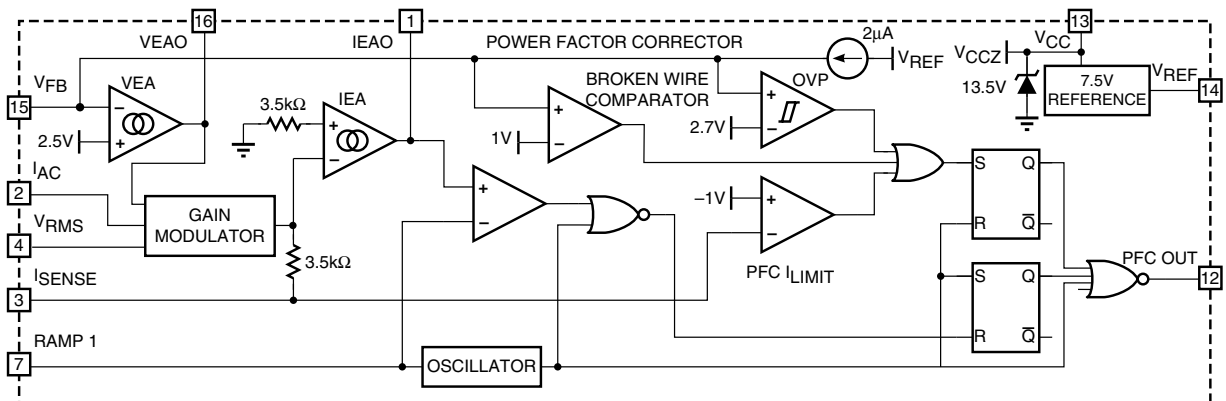


Figure 1. PFC Section Block Diagram

## Functional Description

The ML4827 consists of an average current controlled, continuous boost Power Factor Corrector (PFC) front end and a synchronized Pulse Width Modulator (PWM) back end. The PWM can be used in either current or voltage mode. In voltage mode, feedforward from the PFC output buss can be used to improve the PWM's line regulation. In either mode, the PWM stage uses conventional trailing-edge duty cycle modulation, while the PFC uses leading-edge modulation. This patented leading/trailing edge modulation technique results in a higher useable PFC error amplifier bandwidth, and can significantly reduce the size of the PFC DC buss capacitor.

The synchronization of the PWM with the PFC simplifies the PWM compensation due to the controlled ripple on the PFC output capacitor (the PWM input capacitor). The PWM section of both the ML4827-1 and the ML4827-2 run at the same frequency as the PFC.

A number of protection features have been built into the ML4827 to insure the final power supply will be as reliable as possible. These include TriFault Detect, soft-start, PFC over-voltage protection, peak current limiting, brown-out protection, duty cycle limit, and under-voltage lockout.

### Tri-Fault Detect protection

Many power supplies manufactured for sale in the US must meet Underwriter's Laboratories (UL) standards. UL's specification UL1950 requires that no unsafe condition may result from the failure of any single circuit component. Typical system designs include external active and passive circuitry to meet this requirement. TriFault Detect is an on-chip feature of the ML4827 that monitors the  $V_{FB}$  pin for overvoltage, undervoltage, or floating conditions which indicate that a component of the feedback path may have failed. In such an event, the PFC supply output will be disabled. These integrated redundant protections assure system compliance with UL1950 requirements.

### Power Factor Correction

Power factor correction makes a nonlinear load look like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with and proportional to the line voltage, so the power factor is unity (one). A common class of nonlinear load is the input of most power supplies, which use a bridge rectifier and capacitive input filter fed from the line. The peak-charging effect which occurs on the input filter capacitor in these supplies causes brief high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such supplies present a power factor to the line of less than one (i.e. they cause significant current harmonics of the power line frequency to appear at their input). If the input current drawn by such a supply (or any other nonlinear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the AC line and a unity power factor will be achieved.

To hold the input current draw of a device drawing power from the AC line in phase with and proportional to the input voltage, a way must be found to prevent that device from loading the line except in proportion to the instantaneous line voltage. The PFC section of the ML4827 uses a boost-mode DC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage. No bulk filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice line frequency) from zero volts to the peak value of the AC input and back to zero. By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current which the converter draws from the power line agrees with the instantaneous line voltage. One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is 385VDC, to allow for a high line of 270VAC<sub>rms</sub>. The other condition is that the current which the converter is allowed to draw from the line at any given instant must be proportional to the line voltage. The first of these requirements is satisfied by establishing a suitable voltage control loop for the converter, which in turn drives a current error amplifier and switching output driver. The second requirement is met by using the rectified AC line voltage to modulate the output of the voltage control loop. Such modulation causes the current error amplifier to command a power stage current which varies directly with the input voltage. In order to prevent ripple which will necessarily appear at the output of the boost circuit (typically about 10VAC on a 385V DC level) from introducing distortion back through the voltage error amplifier, the bandwidth of the voltage loop is deliberately kept low. A final refinement is to adjust the overall gain of the PFC such to be proportional to  $1/V_{IN}^2$ , which linearizes the transfer function of the system as the AC input voltage varies.

Since the boost converter topology in the ML4827 PFC is of the current-averaging type, no slope compensation is required.

### PFC Section

#### Gain Modulator

Figure 1 shows a block diagram of the PFC section of the ML4827. The gain modulator is the heart of the PFC, as it is this circuit block which controls the response of the current loop to line voltage waveform and frequency, RMS line voltage, and PFC output voltage. There are three inputs to the gain modulator. These are:

1. A current representing the instantaneous input voltage (amplitude and waveshape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is then fed into the gain modulator at  $I_{AC}$ . Sampling current in this way minimizes ground noise, as is required in high power switching power conversion environments. The gain modulator responds linearly to this current.

2. A voltage proportional to the long-term RMS AC line voltage, derived from the rectified line voltage after scaling and filtering. This signal is presented to the gain modulator at  $V_{RMS}$ . The gain modulator's output is inversely proportional to  $V_{RMS}^2$  (except at unusually low values of  $V_{RMS}$  where special gain contouring takes over, to limit power dissipation of the circuit components under heavy brownout conditions). The relationship between  $V_{RMS}$  and gain is termed  $K$ , and is illustrated in the Typical Performance Characteristics.
3. The output of the voltage error amplifier,  $VEAO$ . The gain modulator responds linearly to variations in this voltage.

The output of the gain modulator is a current signal, in the form of a full wave rectified sinusoid at twice the line frequency. This current is applied to the virtual-ground (negative) input of the current error amplifier. In this way the gain modulator forms the reference for the current error loop, and ultimately controls the instantaneous current draw of the PFC from the power line. The general form for the output of the gain modulator is:

$$I_{GAINMOD} = \frac{I_{AC} \times VEAO}{V_{RMS}^2} \times 1V \quad (1)$$

More exactly, the output current of the gain modulator is given by:

$$I_{GAINMOD} = K \times (VEAO - 1.5V) \times I_{AC}$$

where  $K$  is in units of  $V^{-1}$ .

Note that the output current of the gain modulator is limited to  $\cong 200\mu A$ .

### Current Error Amplifier

The current error amplifier's output controls the PFC duty cycle to keep the average current through the boost inductor a linear function of the line voltage. At the inverting input to the current error amplifier, the output current of the gain modulator is summed with a current which results from a negative voltage being impressed upon the  $I_{SENSE}$  pin (current into  $I_{SENSE} \cong V_{SENSE}/3.5k\Omega$ ). The negative voltage on  $I_{SENSE}$  represents the sum of all currents flowing in the PFC circuit, and is typically derived from a current sense resistor in series with the negative terminal of the input bridge rectifier. In higher power applications, two current transformers are sometimes used, one to monitor the  $I_D$  of the boost MOS-

FET(s) and one to monitor the  $I_F$  of the boost diode. As stated above, the inverting input of the current error amplifier is a virtual ground. Given this fact, and the arrangement of the duty cycle modulator polarities internal to the PFC, an increase in positive current from the gain modulator will cause the output stage to increase its duty cycle until the voltage on  $I_{SENSE}$  is adequately negative to cancel this increased current. Similarly, if the gain modulator's output decreases, the output duty cycle will decrease, to achieve a less negative voltage on the  $I_{SENSE}$  pin.

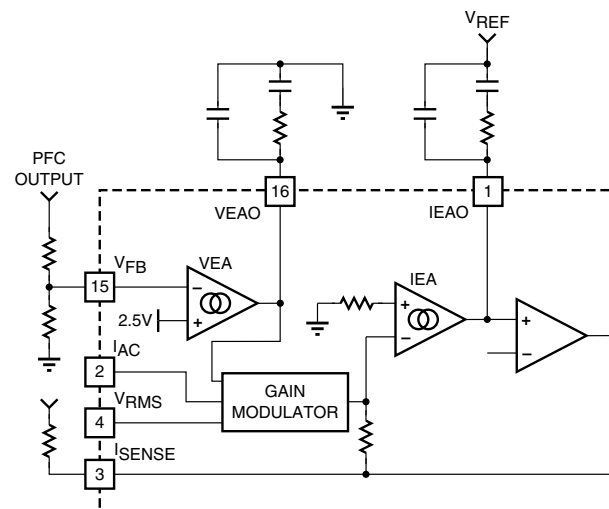


Figure 2. Compensation Network Connections for the Voltage and Current Error Amplifiers

### Cycle-By-Cycle Current Limiter

The  $I_{SENSE}$  pin, as well as being a part of the current feedback loop, is a direct input to the cycle-by-cycle current limiter for the PFC section. Should the input voltage at this pin ever be more negative than  $-1V$ , the output of the PFC will be disabled until the protection flip-flop is reset by the clock pulse at the start of the next PFC power cycle.

### Overvoltage Protection

The OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load should suddenly change. A resistor divider from the high voltage DC output of the PFC is fed to  $V_{FB}$ . When the voltage on  $V_{FB}$  exceeds  $2.7V$ , the PFC output driver is shut down. The PWM section will continue to operate. The OVP comparator has  $125mV$  of hysteresis, and the PFC will not restart until the voltage at  $V_{FB}$  drops below  $2.58V$ . The  $V_{FB}$  should be set at a level where the active and passive external power components and the ML4827 are within their safe operating voltages, but not so low as to interfere with the boost voltage regulation loop.



### Error Amplifier Compensation

The PWM loading of the PFC can be modeled as a negative resistor; an increase in input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers. Figure 2 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with their respective return points. The current loop compensation is returned to  $V_{REF}$  to produce a soft-start characteristic on the PFC: as the reference voltage comes up from zero volts, it creates a differentiated voltage on IEAO which prevents the PFC from immediately demanding a full duty cycle on its boost converter.

There are two major concerns when compensating the voltage loop error amplifier; stability and transient response. Optimizing interaction between transient response and stability requires that the error amplifier's open-loop crossover frequency should be 1/2 that of the line frequency, or 23Hz for a 47Hz line (lowest anticipated international power frequency). The gain vs. input voltage of the ML4827's voltage error amplifier has a specially shaped nonlinearity such that under steady-state operating conditions the transconductance of the error amplifier is at a local minimum. Rapid perturbations in line or load conditions will cause the input to the voltage error amplifier ( $V_{FB}$ ) to deviate from its 2.5V (nominal) value. If this happens, the transconductance of the voltage error amplifier will increase significantly, as shown in the Typical Performance Characteristics. This raises the gain-bandwidth product of the voltage loop, resulting in a much more rapid voltage loop response to such perturbations than would occur with a conventional linear gain characteristic.

The current amplifier compensation is similar to that of the voltage error amplifier with the exception of the choice of crossover frequency. The crossover frequency of the current amplifier should be at least 10 times that of the voltage amplifier, to prevent interaction with the voltage loop. It should also be limited to less than 1/6th that of the switching frequency, e.g. 16.7kHz for a 100kHz switching frequency.

There is a modest degree of gain contouring applied to the transfer characteristic of the current error amplifier, to increase its speed of response to current-loop perturbations. However, the boost inductor will usually be the dominant factor in overall current loop response. Therefore, this contouring is significantly less marked than that of the voltage error amplifier.

For more information on compensating the current and voltage control loops, see Application Notes 33 and 34. Application Note 16 also contains valuable information for the design of this class of PFC.

### Oscillator (RAMP 1)

The oscillator frequency is determined by the values of  $R_T$  and  $C_T$ , which determine the ramp and off-time of the oscillator output clock:

$$f_{OSC} = \frac{1}{t_{RAMP} + t_{DEADTIME}} \quad (2)$$

The deadtime of the oscillator is derived from the following equation:

$$t_{RAMP} = C_T \times R_T \times \ln\left(\frac{V_{REF} - 1.25}{V_{REF} - 3.75}\right) \quad (3)$$

at  $V_{REF} = 7.5V$ :

$$t_{RAMP} = C_T \times R_T \times 0.51$$

The deadtime of the oscillator may be determined using:

$$t_{DEADTIME} = \frac{2.5V}{5.1mA} \times C_T = 490 \times C_T \quad (4)$$

The deadtime is so small ( $t_{RAMP} \gg t_{DEADTIME}$ ) that the operating frequency can typically be approximated by:

$$f_{OSC} = \frac{1}{t_{RAMP}} \quad (5)$$

#### EXAMPLE:

For the application circuit shown in the data sheet, with the oscillator running at:

$$f_{OSC} = 100kHz = \frac{1}{t_{RAMP}}$$

$$t_{RAMP} = C_T \times R_T \times 0.51 = 1 \times 10^{-5}$$

Solving for  $R_T \times C_T$  yields  $2 \times 10^{-4}$ . Selecting standard components values,  $C_T = 470pF$ , and  $R_T = 41.2k\Omega$ .

The deadtime of the oscillator adds to the Maximum PWM Duty Cycle (it is an input to the Duty Cycle Limiter). With zero oscillator deadtime, the Maximum PWM Duty Cycle is typically 45% for the ML4827-1. In many applications of the ML4827-1, care should be taken that  $C_T$  not be made so large as to extend the Maximum Duty Cycle beyond 50%. This can be accomplished by using a stable 470pF capacitor for  $C_T$ .

## PWM SECTION

### Pulse Width Modulator

The PWM section of the ML4827 is straightforward, but there are several points which should be noted. Foremost among these is its inherent synchronization to the PFC section of the device, from which it also derives its basic timing. The PWM is capable of current-mode or voltage mode operation. In current-mode applications, the PWM ramp (RAMP 2) is usually derived directly from a current sensing resistor or current transformer in the primary of the output stage, and is thereby representative of the current flowing in the converter's output stage. DC I<sub>LIMIT</sub>, which provides cycle-by-cycle current limiting, is typically connected to RAMP 2 in such applications. For voltage-mode operation or certain specialized applications, RAMP 2 can be connected to a separate RC timing network to generate a voltage ramp against which V<sub>DC</sub> will be compared. Under these conditions, the use of voltage feedforward from the PFC buss can assist in line regulation accuracy and response. As in current mode operation, the DC I<sub>LIMIT</sub> input would be used for output stage overcurrent protection.

No voltage error amplifier is included in the PWM stage of the ML4827, as this function is generally performed on the output side of the PWM's isolation boundary. To facilitate the design of optocoupler feedback circuitry, an offset has been built into the PWM's RAMP 2 input which allows V<sub>DC</sub> to command a zero percent duty cycle for input voltages below 1.25V.

### Maximum Duty Cycle

In the ML4827-1, the maximum duty cycle of the PWM section is limited to 50% for ease of use and design. In the case of the ML4827-2, the maximum duty cycle of the PWM section is extended to 70% (typical) for enhanced utilization of the inductor. Operation at 70% duty cycle requires special care in circuit design to avoid volt-second imbalances, and/or high-voltage damage to the PWM switch transistor(s).

### Using the ML4827-2

The ML4827-2's higher PWM duty cycle offers several design advantages that skilled power supply and magnetics engineers can take advantage of, including:

- Reduced RMS and peak PWM switch currents
- Reduced RMS and peak PWM transformer currents
- Easier RFI/EMI filtering due to lower peak currents

These reduced currents can result in cost savings by allowing smaller PWM transformer primary windings and fewer turns on forward converter reset windings. Long duty cycles, by allowing greater utilization of the PFC's stored charge, can also lower the cost of PFC bus capacitors while still offering long "hold-up" times.

NOTE: during the time when the PWM switch is off (the reset or flyback periods), increasing duty cycles will result in rapidly increasing peak voltages across the switch. This result of high PWM duty cycles requires greater care be used in circuit design. Relevant design issues include:

- Higher voltage (>1000V) PWM switches
- More carefully designed and tested PWM transformers
- Clamps and/or snubbers when needed

Also, slope compensation will be required in most current mode PWM designs.

For those who want to approach the limits of attainable performance (most commonly high-volume, low-cost supplies), the ML4827-2's 70% maximum PWM duty cycle offers several desirable design capabilities. Using a 70% duty cycle makes it essential to perform a careful magnetics design and component stress analysis before finalizing designs with the ML4827-2.

### The ML4827-2: Special Considerations for High Duty Cycles

The use of the ML4827-1, especially with the type of PWM output stage shown in the Application Circuit of Figure 6, is straightforward due to the limitation of the PWM duty cycle to 50% maximum. In fact, one of the advantages of the "two-transistor single-ended forward converter" shown in Figure 6 is that it will necessarily reset the core, with no additional winding required, as long as the core does not go into saturation during the topology's maximum permissible 50% duty cycle.

For the "-2" version of the ML4827, the maximum duty cycle ( $\delta$ ) of the PWM is nominally 70%. As the two-transistor single-ended forward converter cannot be used at duty cycles greater than 50%, high- $\delta$  applications require the use of either a single-transistor forward converter (with a transformer reset winding), or a flyback output stage. In either case, special concerns arise regarding the peak voltage appearing on the PWM switch transistor, the PWM output transformer, and associated power components as the duty cycle increases. For any output stage topology, the available on-time (core "set" time) is  $(1/f_{PWM}) \times \delta$ , while the reset time for the core of the PWM output transformer is  $(1/f_{PWM}) \times (1-\delta)$ . This means that the magnetizing inductance of the core charges for a period of  $(1/f_{PWM}) \times \delta$ , and must be completely discharged during a period of  $(1/f_{PWM}) \times (1-\delta)$ . The ratio of these two periods, multiplied by the maximum value of the PFC's V<sub>BUSS</sub>, yields the minimum voltage for which the PWM output transistor must be rated. Frequently, the design of the transformer's reset winding, and/or of the output transistor's snubbers or clamps, require an additional voltage margin of 100V to 200V.

To put some numbers into the discussion, with a given  $V_{BUSS(MAX)}$  of 400V:

1. For  $\delta = 50\%$ :  $V_{RESET} = \{[(1/f_{PWM}) \times \delta] / [(1/f_{PWM}) \times (1-\delta)]\} \times 400V = 0.50/0.50 \times 400V = 400V$
2. For  $\delta = 55\%$ :  $V_{RESET} = 0.55/0.45 \times 400V = 489V$
3. For  $\delta = 60\%$ :  $V_{RESET} = 0.60/0.40 \times 400V = 600V$
4. For  $\delta = 64\%$  (Data Sheet Lower Limit Value):  $V_{RESET} = 0.64/0.36 \times 400V = 711V$
5. For  $\delta = 70\%$ :  $V_{RESET} = 0.70/0.30 \times 400V = 933V$
6. For  $\delta = 74\%$  (Data Sheet Upper Limit Value):  $V_{RESET} = 0.74/0.26 \times 400V = 1138V$

It is economically desirable to design for the lowest meaningful voltage on the output MOSFET. It is simultaneously necessary to design the circuit to operate at the lowest guaranteed value for  $\delta$ , to ensure that the magnetics will deliver full output power with any individual ML4827. In actual operation, the choice of  $\delta_{MIN} = 60\%$  will allow some toler-

ance for the timing capacitors and resistors. A tolerance on  $(R_{RAMP2} \times C_{RAMP2})$  of  $\pm 2\%$  is the simplest “brute force” way to achieve the desired result. This should be combined with an external duty cycle clamp. This protects the PWM circuitry against the condition in which the output has been shorted, and the error amplifier output ( $V_{DC}$ ) would otherwise be driven to its upper rail. One method which works well when the PWM is used in voltage mode is to limit the maximum input to the PWM feedback voltage ( $V_{DC}$ ). If the voltage available to this pin is derived from the ML4827’s 7.5V  $V_{REF}$ , it will be in close ratio to the charging time of the RAMP2 capacitor. This will be true whether the RAMP2 capacitor is charged from  $V_{REF}$ , or, as is more commonly done in voltage-mode applications, from the output of the PFC Stage (the “feedforward” configuration). Figure 3 shows such a duty cycle clamp.

If the ML4827-2’s PWM is to be used in a current-mode design, the PWM stage will require slope compensation. This can be done by any of the standard industry techniques. Note that the ramp to use for this slope compensation is the voltage on RAMP1.

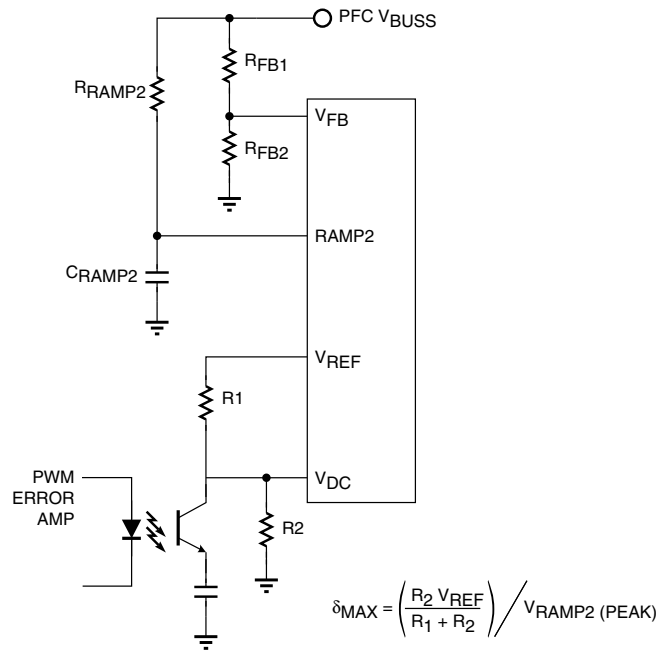


Figure 3. ML4827-PWM Duty Cycle Clamp for Voltage-Made Operation

Using the recommended values of  $\delta_{\text{MIN}} = 60\%$  and  $\delta_{\text{MAX}} = 64\%$  for a high- $\delta$  application, a MOSFET switch with a Drain-Source breakdown voltage of 900V, or in some cases as low as 800V, can reliably be used. Such parts are readily and inexpensively available from a number of vendors.

### V<sub>IN</sub> OK Comparator

The V<sub>IN</sub> OK comparator monitors the DC output of the PFC and inhibits the PWM if this voltage on V<sub>FB</sub> is less than its nominal 2.5V. Once this voltage reaches 2.5V, which corresponds to the PFC output capacitor being charged to its rated boost voltage, the soft-start begins.

### PWM Control (RAMP 2)

When the PWM section is used in current mode, RAMP 2 is generally used as the sampling point for a voltage representing the current in the primary of the PWM's output transformer, derived either by a current sensing resistor or a current transformer. In voltage mode, it is the input for a ramp voltage generated by a second set of timing components (R<sub>RAMP2</sub>, C<sub>RAMP2</sub>), which will have a minimum value of zero volts and should have a peak value of approximately 5V. In voltage mode operation, feedforward from the PFC output buss is an excellent way to derive the timing ramp for the PWM stage.

### Soft Start

Start-up of the PWM is controlled by the selection of the external capacitor at SS. A current source of 50 $\mu$ A supplies the charging current for the capacitor, and start-up of the PWM begins at 1.25V. Start-up delay can be programmed by the following equation:

$$C_{\text{SS}} = t_{\text{DELAY}} \times \frac{50\mu\text{A}}{1.25\text{V}} \quad (6)$$

where C<sub>SS</sub> is the required soft start capacitance, and t<sub>DELAY</sub> is the desired start-up delay.

It is important that the time constant of the PWM soft-start allow the PFC time to generate sufficient output power for the

PWM section. The PWM start-up delay should be at least 5ms.

Solving for the minimum value of C<sub>SS</sub>:

$$C_{\text{SS}} = 5\text{ms} \times \frac{50\mu\text{A}}{1.25\text{V}} \cong 220\text{nF}$$

### Generating V<sub>CC</sub>

The ML4827 is a current-fed part. It has an internal shunt voltage regulator, which is designed to regulate the voltage internal to the part at 13.5V. This allows a low power dissipation while at the same time delivering 10V of gate drive at the PWM OUT and PFC OUT outputs. It is important to limit the current through the part to avoid overheating or destroying it. This can be easily done with a single resistor in series with the V<sub>CC</sub> pin, returned to a bias supply of typically 18V to 20V. The resistor's value must be chosen to meet the operating current requirement of the ML4827 itself (19mA max) plus the current required by the two gate driver outputs.

#### EXAMPLE:

With a V<sub>BIAS</sub> of 20V, a V<sub>CC</sub> limit of 14.6V (max) and the ML4827 driving a total gate charge of 110nC at 100kHz (e.g., 1 IRF840 MOSFET and 2 IRF830 MOSFETs), the gate driver current required is:

$$I_{\text{GATEDRIVE}} = 100\text{kHz} \times 100\text{nC} = 11\text{mA} \quad (7)$$

$$R_{\text{BIAS}} = \frac{20\text{V} - 14.6\text{V}}{19\text{mA} + 11\text{mA}} = 180\Omega \quad (8)$$

To check the maximum dissipation in the ML4827, find the current at the minimum V<sub>CC</sub> (12.4V):

$$I_{\text{CC}} = \frac{20\text{V} - 12.4\text{V}}{180\Omega} = 42.2\text{mA} \quad (9)$$

The maximum allowable I<sub>CC</sub> is 55mA, so this is an acceptable design.

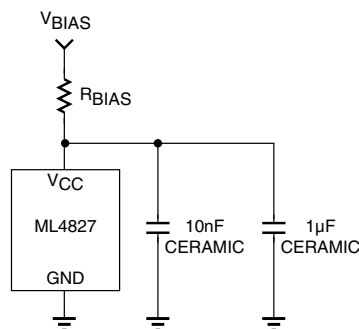


Figure 4. External Component Connections to V<sub>CC</sub>

The ML4827 should be locally bypassed with a 10nF and a 1μF ceramic capacitor. In most applications, an electrolytic capacitor of between 100μF and 330μF is also required across the part, both for filtering and as part of the start-up bootstrap circuitry.

### Leading/Trailing Modulation

Conventional Pulse Width Modulation (PWM) techniques employ trailing edge modulation in which the switch will turn on right after the trailing edge of the system clock. The error amplifier output voltage is then compared with the modulating ramp. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned OFF. When the switch is ON, the inductor current will ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 5 shows a typical trailing edge control scheme.

In the case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during the OFF time of the switch. Figure 6 shows a leading edge control scheme.

One of the advantages of this control technique is that it requires only one system clock. Switch 1 (SW1) turns off and switch 2 (SW2) turns on at the same instant to minimize the momentary “no-load” period, thus lowering ripple voltage generated by the switching action. With such

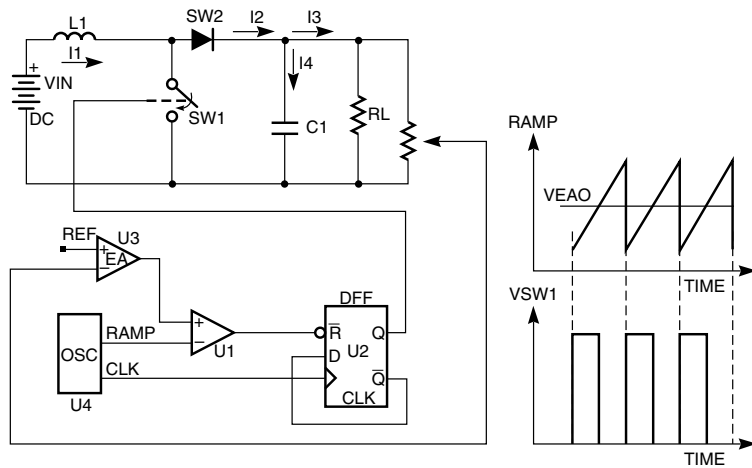


Figure 5. Typical Trailing Edge Control Scheme

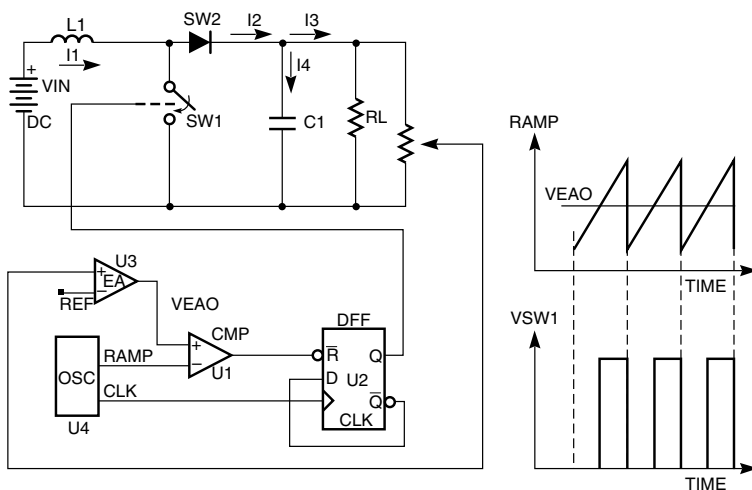


Figure 6. Typical Leading Edge Control Scheme

synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC's output ripple voltage can be reduced by as much as 30% using this method.

### Typical Applications

Figure 7 is the application circuit for a complete 100W power factor corrected power supply. This circuit was designed using the methods and topology detailed in Application Note 33.

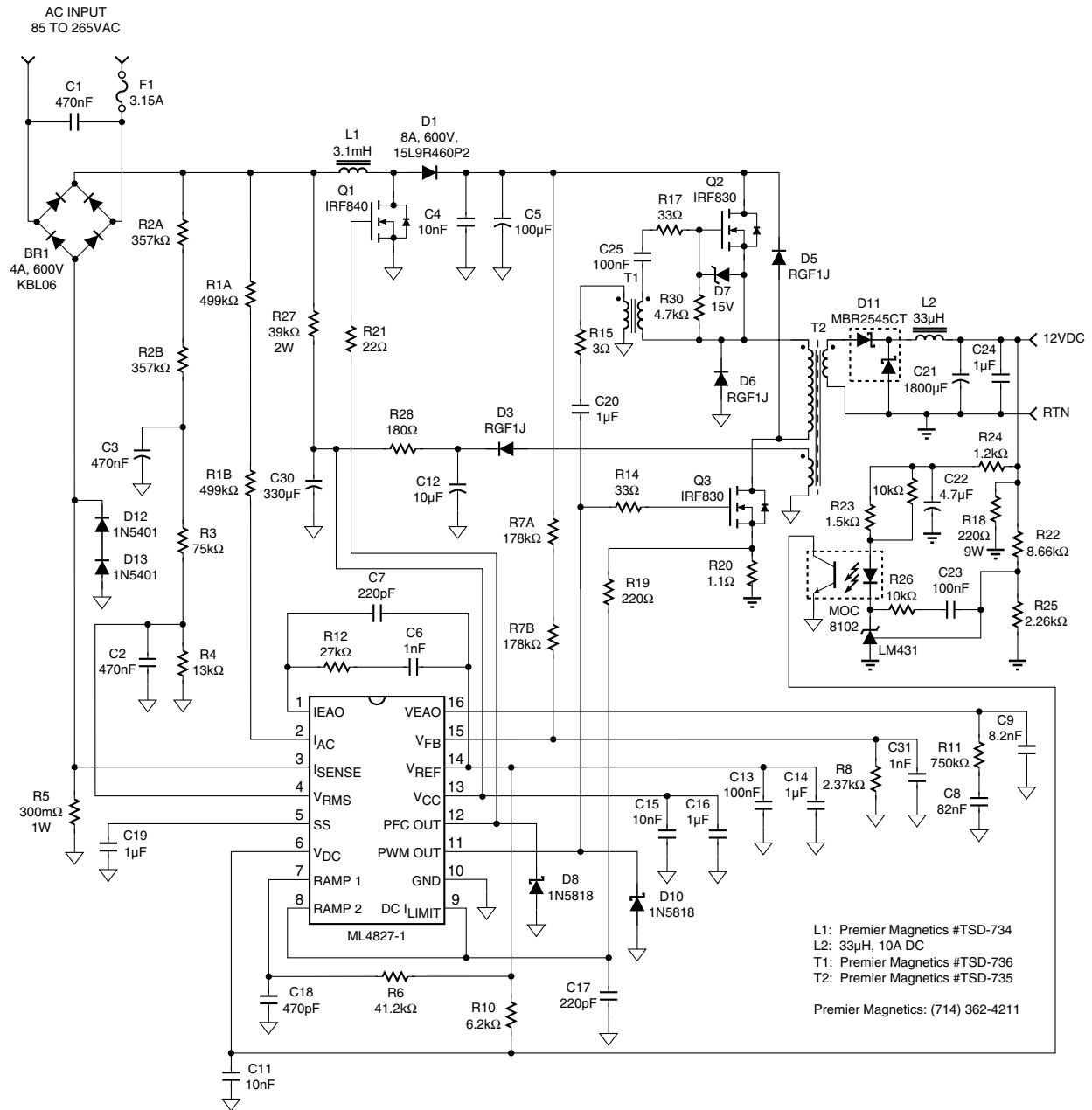
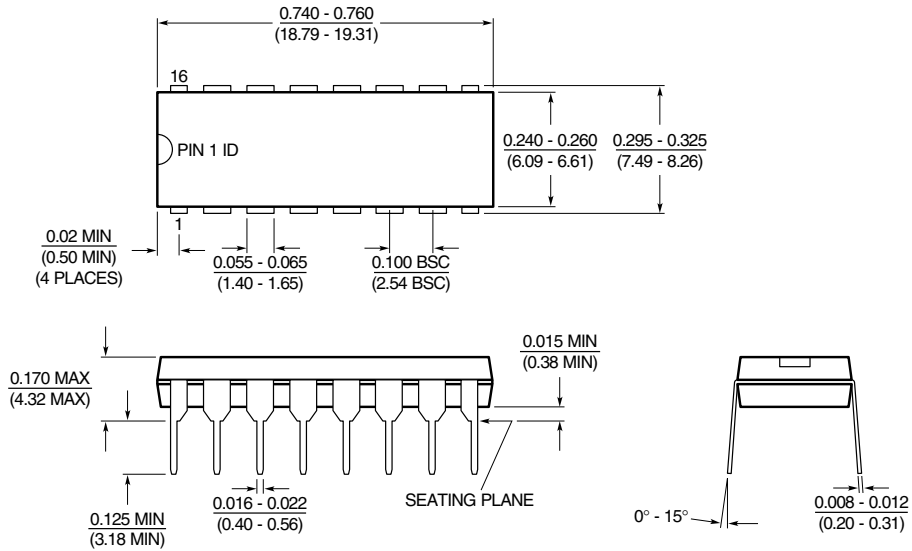


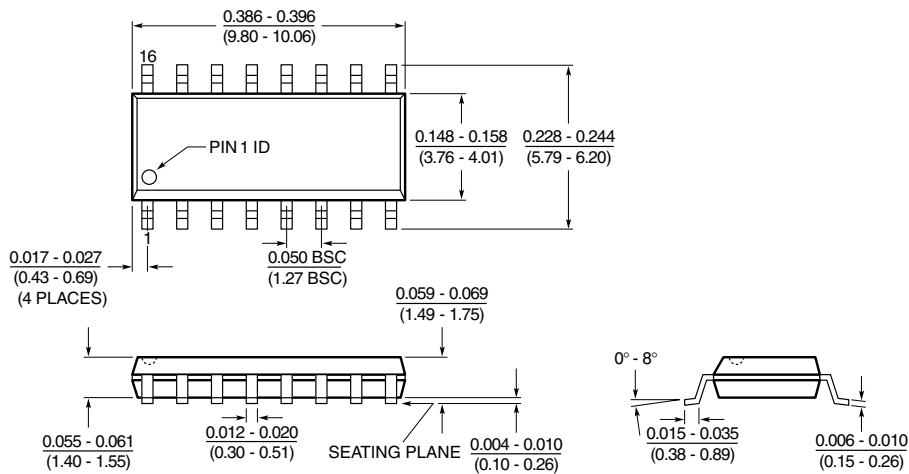
Figure 7. 100W Power Factor Corrected Power Supply, Designed Using Micro Linear Application Note 33

**Mechanical Dimensions** inches (millimeters)

**Package: P16**  
**16-Pin PDIP**



**Package: S16N**  
**16-Pin Narrow SOIC**



## Ordering Information

Part Number	Max Duty Cycle	Temperature Range	Package
ML4827CP-1	50%	0°C to 70°C	16-Pin PDIP (P16)
ML4827CP-2	74%	0°C to 70°C	16-Pin PDIP (P16)
ML4827CS-1	50%	0°C to 70°C	16-Pin Narrow SOIC (S16N)
ML4827CS-2	74%	0°C to 70°C	16-Pin Narrow SOIC (S16N)
ML4827IP-2	74%	-40°C to 85°C	16-Pin PDIP (P16)
ML4827IS-2	74%	-40°C to 85°C	16-Pin Narrow SOIC (S16N)

### DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.