FAIRCHILD
SEMICONDUCTOR®

SPT7730

8-BIT, 3.0 MSPS, SERIAL OUTPUT A/D CONVERTER

FEATURES

- 8-Bit, 1 kHz to 3.0 MSPS Analog-to-Digital Converter
- Monolithic CMOS
- Serial Output
- Internal Sample-and-Hold
- Analog Input Range: 0 to 2 V Nominal; 3.3 V Max
- Power Dissipation (Excluding Reference Ladder)
  45 mW at +5 V
  16 mW at +3 V
- Single Power Supply: +3 V to +5 V Range
- High ESD Protection: 3,000 V Minimum

APPLICATIONS

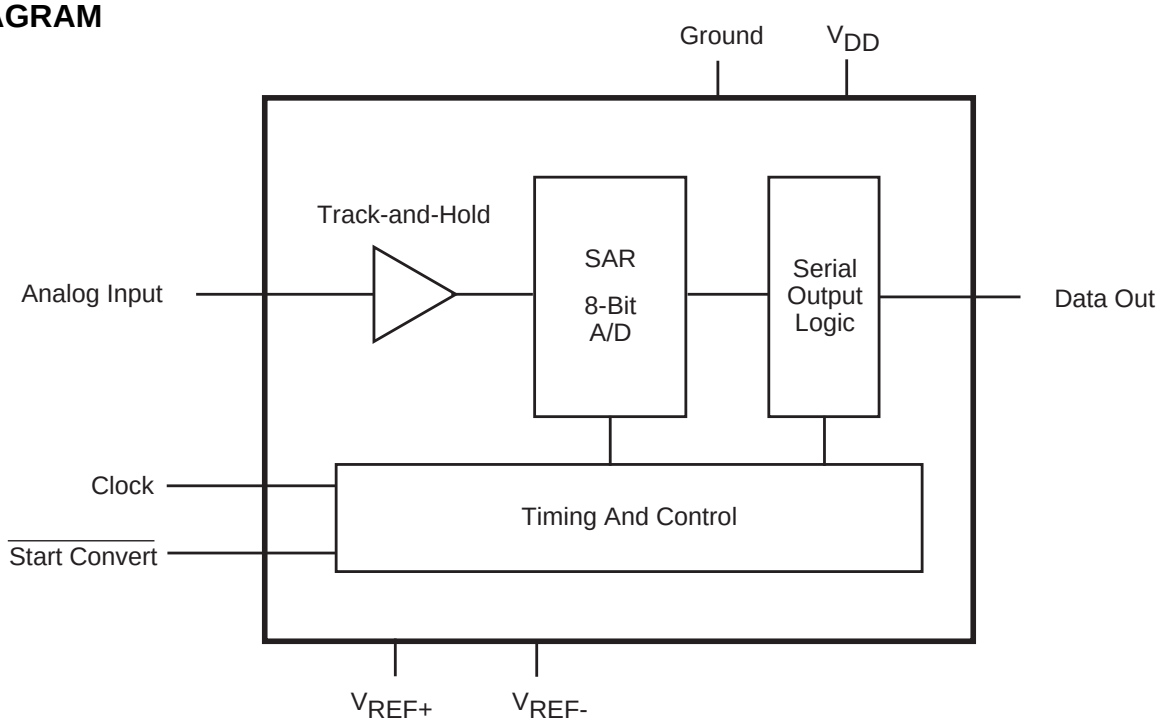
- Handheld and Desktop Scanners
- DSP Interface Applications
- Portable Digital Radios
- Portable and Handheld Applications
- Automotive Applications
- Remote Sensing

GENERAL DESCRIPTION

The Fairchild 8-bit, 3.0 MSPS, serial analog-to-digital converter delivers excellent high speed conversion performance with low cost and low power. The serial port protocol is compatible with the serial peripheral interface (SPI) or MICROWIRE™ industry standard, high-speed synchronous MPU interfaces. The large input bandwidth and fast transient response time allow for CCD applications operating up to 3.0 MSPS.

The device can operate with a power supply range from +3 V to +5 V with very low power dissipation. The small package size makes this part excellent for handheld applications where board space is a premium. The SPT7730 is available in an 8-lead SOIC package over the commercial temperature range. Contact the factory for availability of die and industrial temperature range versions.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages

V_{DD} ..... +6 V

Input Voltages

Analog Input ..... -0.7 to +6 V
$V_{REF}+$ ..... -0.7 to +6 V
$V_{REF}-$ ..... -0.7 to +6 V
Clock and $\overline{SC}$ ..... -0.7 to +6 V

Output

Data Out ..... 10 mA

Temperature

Operating, ambient ..... 0 to 70 °C
junction ..... + 175 °C
Lead, Soldering (10 seconds) ..... + 300 °C
Storage ..... -65 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{DD} = +5.0 V, V_{IN} = 0 to +3 V, f_{CLK} = 36 MHz, f_S = 3.0 MSPS, $V_{REF}+$ = +3.0 V, $V_{REF}-$ = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
DC Performance						
Resolution				8		Bits
Differential Linearity		I		±0.2	±0.5	LSB
Integral Linearity		I		±0.2	±0.5	LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range[1]		IV	$V_{REF}-$ +4%		$V_{REF}+$ -6%	V
Input Resistance		I	5			MΩ
Input Capacitance		IV		5		pF
Input Bandwidth (Small Signal)		IV		30		MHz
Offset		IV	-2		+2	% of FSR
Gain Error		IV	-2		+2	% of FSR
Reference Input						
Resistance		IV	250	280	350	Ω
Voltage Range[1]						
$V_{REF}-$[2]		IV	-4%	0	$V_{REF}+-\Delta$	V
$V_{REF}+$[2]		IV	$V_{REF}-+\Delta$		2/3 V_{DD}	V
$V_{REF}+$ -$V_{REF}-$ (Δ)		IV	1/10 V_{DD}			V
Reference Settling Time		IV			90	ns
Timing Characteristics						
Maximum Conversion Rate		I	3.0	1.0		MSPS
Minimum Conversion Rate		IV	1			kSPS
Maximum External Clock Rate		I	36	12		MHz
Minimum External Clock Rate		IV	12			kHz
Aperture Delay Time		IV		5		ns
Aperture Jitter Time		IV		5		ps
Data Ouput LSB Hold Time	T_{MIN} to T_{MAX}	IV	6	8		ns

[1]Percentages refer to percent of [($V_{REF}+$) -($V_{REF}-$)]

[2]Δ = Minimum ($V_{REF}+$ -$V_{REF}-$)

ELECTRICAL SPECIFICATIONS

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PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Effective Number of Bits						
f_{IN} = 500 kHz		IV		7.5		Bits
Signal-to-Noise Ratio						
f_{IN} = 500 kHz		IV		47		dB
Harmonic Distortion						
f_{IN} = 500 kHz		IV		60		dB
Power Supply Requirements[3]						
+V_{DD} Supply Voltage		IV	3		5.5	V
+V_{DD} Supply Current	V_{DD} = 3.0 V	IV		5.4	7	mA
	V_{DD} = 5.0 V	I		9	10	mA
Power Dissipation	V_{DD} = 3.0 V	IV		16	22	mW
	V_{DD} = 5.0 V	I		45	50	mW

[3]Excluding the reference ladder.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

GENERAL DESCRIPTION AND OPERATION

The SPT7730 is an 8-bit analog-to-digital converter that uses a successive approximation architecture to perform data conversion. Each conversion cycle is 12 clocks in length. When the Not Start Convert ($\overline{SC}$) line is held low, conversion begins on the next rising edge of the input clock. When the conversion cycle begins, the data output pin is forced low until valid data output begins.

The first two clock cycles are used to perform internal offset calibrations and to track the analog input. The analog input is then sampled using an internal track-and-hold amplifier on the falling edge of the third clock cycle. On clock cycles 4 through 12, an 8-bit successive approximation conversion is performed, and the data is output starting with the MSB.

Serial data output begins with output of the MSB. See the Data Output Timing section for details. Each bit of the data conversion is sequentially determined and placed on the data output pin at the clock rate. This process continues until the LSB has been determined and output. At this point, if the $\overline{SC}$ line is high, the data output pin will be forced into a high impedance state, and the converter will go into an idle state waiting for the $\overline{SC}$ line to go low. This is referred to as Single Shot Mode. See Modes of Operation for details.

If the $\overline{SC}$ is either held low through the entire 12 clock conversion cycle (free run mode) or is brought low prior to the trailing edge of the twelfth clock cycle (synchronous mode), the data output pin goes low and stays low until valid data output begins. Because the chip has either remained selected in the free run mode or has been immediately selected again in the synchronous mode, the next conversion cycle begins immediately after the twelfth clock cycle of the previous conversion. See Modes of Operation for details.

TYPICAL INTERFACE CIRCUIT

CLOCK INPUT

The SPT7730 requires a 50% ±10 % duty cycle clock running at 12 times the desired sample rate. The clock may be stopped in between conversion cycles without degradation of operation (single shot type of operation), however, the clock should remain running during a conversion cycle.

POWER SUPPLY

The SPT7730 requires only a single supply and operates from 3.0 V to 5.0 V. Fairchild recommends that a 0.01 µF chip capacitor be placed as close as possible to the supply pin.

DATA OUTPUT SET UP AND HOLD TIMING

As figure 8 shows, all of the data output bits (except the LSB) remains valid for a duration equivalent to one clock period and delayed by 8 ns after the falling edge of clock. Because the data converter enters into a next conversion ready state at the leading edge of clock 12, **the LSB bit is valid for a duration equivalent to only the clock pulse width low and delayed by 8 ns after the falling edge of clock.** Care should be taken to ensure that the LSB is latched into an external latch with the proper amount of set and hold time.

DATA OUTPUT CODING

The coding of the output is straight binary. (See table I.)

Table I - Data Output Coding

ANALOG INPUT	OUTPUT CODE D7 - DO	
+FS - 1/2 LSB	1 1 1 1	1 1 1 Ø
+1/2 FS	ØXXX	XXXX
+1/2 LSB	OOOO	OOOØ
V_{REF-}	OOOO	OOOO

Ø indicates the flickering bit between logic O and 1.
X indicates the flickering bit between logic 1 and O.

ANALOG INPUT AND REFERENCE SETTLING TRACK AND HOLD TIMING

Figure 9 shows the timing relationship between the input clock and $\overline{SC}$ versus the analog input tracking and reference settling. The analog input is tracked from the twelfth clock cycle of the previous conversion to the third clock cycle of the current conversion. On the falling edge of the third clock cycle, the analog input is held by the internal sample-and-hold. After this sample, the analog input may vary without affecting data conversion.

The reference ladder inputs ($V_{REF}+$ and $V_{REF}-$) may be changed starting on the falling edge of the eleventh clock cycle of the previous conversion and must be settled by the falling edge of the third clock cycle of the current conversion. (See figure 9.)

VOLTAGE REFERENCE AND ANALOG INPUT

The SPT7730 requires the use of a single external voltage reference for driving the high side of the reference ladder. The $V_{REF}+$ can be a maximum of 2/3 V_{DD}. For example, if V_{DD} = +5 V, then $V_{REF}+$ max = (2/3) * 5 V = +3.3 V. The lower side of the ladder is typically tied to AGND (0.0 V) but can be run up to a voltage that is 1/10th of V_{DD} below $V_{REF}+$:

$V_{REF}-$ max. = $V_{REF}+$ - (1/10) * V_{DD}.

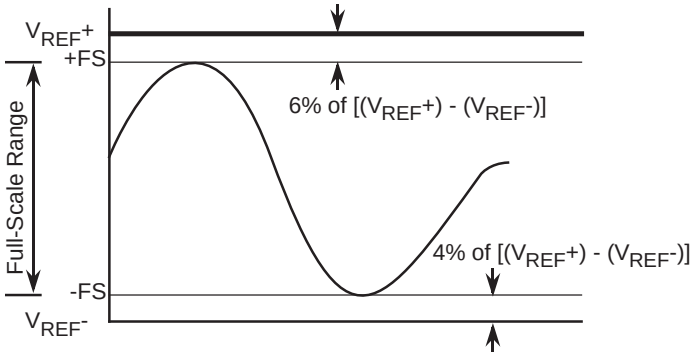
For example,
if V_{DD} = +5 V and $V_{REF}+$ = 3 V, then
$V_{REF}-$ max. = 3 V - (1/10)* 5 V = 2.5 V.

The +Full Scale (+FS) of the analog input is expected to be 6% of [($V_{REF}+$)-($V_{REF}-$)] below $V_{REF}+$ and the -Full Scale (-FS) of the analog input is expected to be 4% of [($V_{REF}+$) - ($V_{REF}-$)] above $V_{REF}-$. (See figure 1.)

Therefore,
Analog +FS = $V_{REF}+$ - 0.06 * [($V_{REF}+$) - ($V_{REF}-$)], and
Analog -FS = $V_{REF}-$ +0.04 * [($V_{REF}+$) - ($V_{REF}-$)].

For example,
if $V_{REF}+$ = 3 V and $V_{REF}-$ = 0 V, then
Analog + FS = 3 V - 0.06 * [3 V- 0 V] = 2.82 V, and
Analog - FS = 0 V + 0.04 * [3 V - 0 V] = 0.12 V.

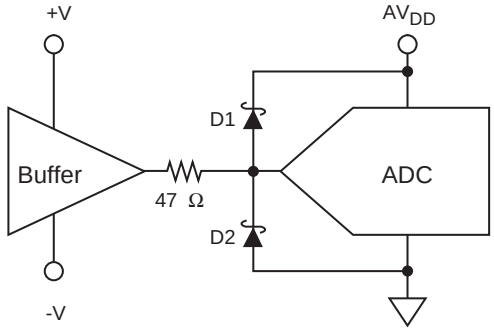
Figure 1 - Analog Input Full-Scale Range



The drive requirements for the analog input are minimal when compared to most other converters due to the SPT7730's extremely low input capacitance of only 5 pF and very high input resistance of greater than 5 MΩ.

If the input buffer amplifier supply voltages are greater than V_{DD} + 0.7 V or less than Ground - 0.7 V, the analog input should be protected through a series resistor and a diode clamping circuit as shown in figure 2.

Figure 2 - Recommended Input Protection Circuit

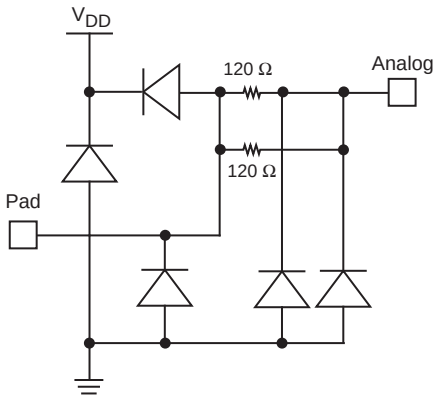


D1 = D2 = Hewlett Packard HP5712 or equivalent

INPUT PROTECTION

All I/O pads are protected with an on-chip protection circuit shown in figure 3. This circuit provides ESD robustness to >3.0 kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

Figure 3 - On-Chip Protection Circuit



MODES OF OPERATION

The SPT7730 has three modes of operation.The mode of operation is based strictly on how the $\overline{SC}$ is used.

SINGLE SHOT MODE

When $\overline{SC}$ goes low, conversion starts on the next rising edge of the clock (defined as the first conversion clock). The MSB of data is valid 8 ns after the falling edge of the fourth conversion clock. (See figure 8.)

The conversion is complete after 12 clock cycles. At the falling edge of the twelfth clock cycle, if $\overline{SC}$ is high (not selected), the data output goes to a high impedance state, and no more conversions will take place until the next $\overline{SC}$ low event. (See the single shot mode timing diagram in figure 4.)

SYNCHRONIZED MODE

When $\overline{SC}$ goes low, conversion will start on the next rising edge of the clock (defined as the first conversion clock). The MSB is valid 8 ns after the falling edge of the fourth conversion clock.

The first conversion is complete after 12 clock cycles. At any time after the falling edge of the twelfth clock cycle, $\overline{SC}$ may go low again to initiate the next conversion. When the $\overline{SC}$ goes low, the conversion starts on the rising edge of the next clock. (See the synchronized mode timing diagram in figure 5.)

The data output will go to a high impedance state until the next conversion is initiated.

FREE RUN MODE

When $\overline{SC}$ goes low, conversion starts on the next rising edge of the clock (defined as the first conversion clock). The MSB data is valid 8 ns after the falling edge of the fourth conversion clock.

As long as $\overline{SC}$ is held low, the device operates in the free run mode. New conversions start after every twelfth cycle with valid data available 8 ns after the falling edge of the fourth clock within each new conversion cycle.

The data output remains low between conversion cycles. (See the free run mode timing diagram in figure 6.)

Figure 4 - Single Shot Mode Timing Diagram

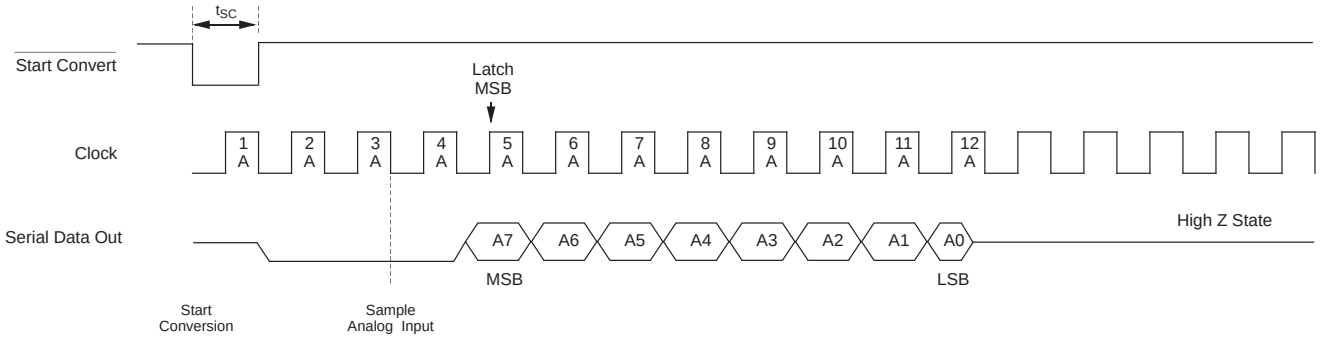


Figure 5 - Synchronous Mode Timing Diagram

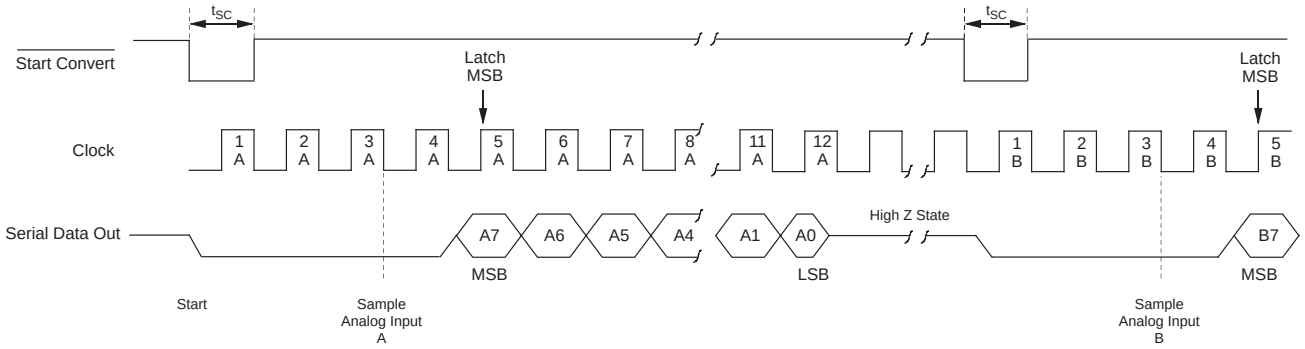


Figure 6 - Free Run Mode Timing Diagram

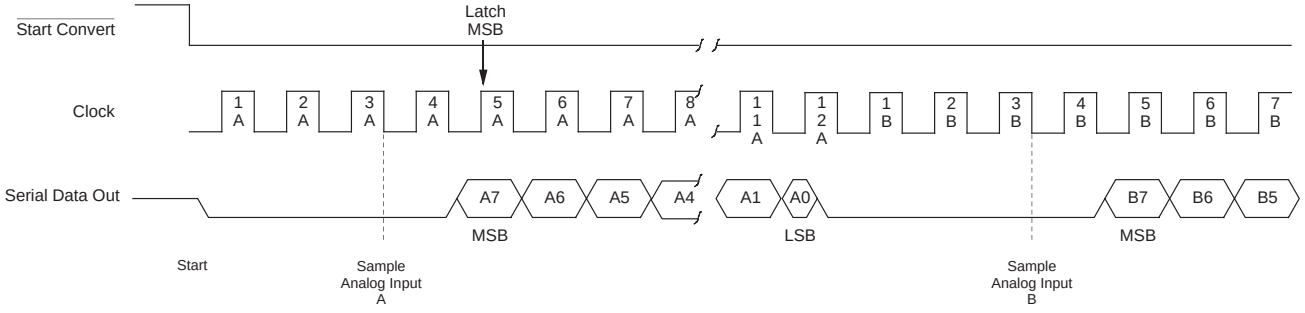


Figure 7 - Typical Interface Circuit

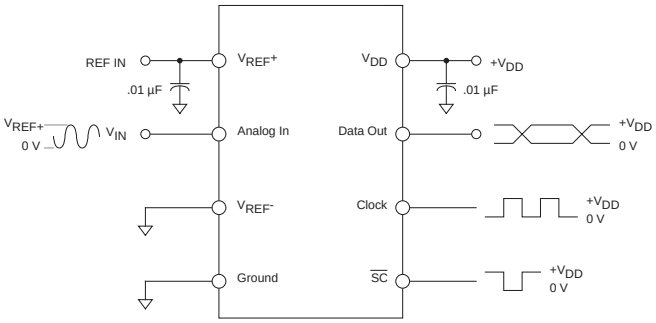


Figure 8 - Data Output Timing

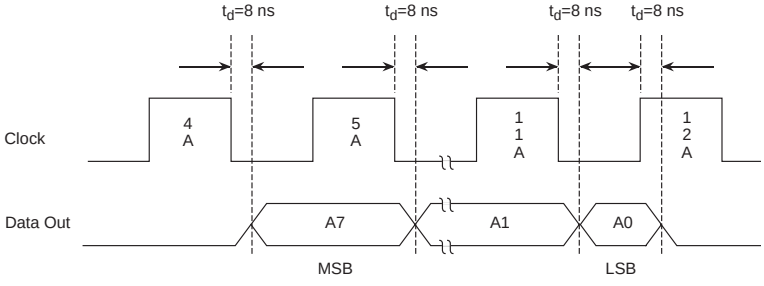
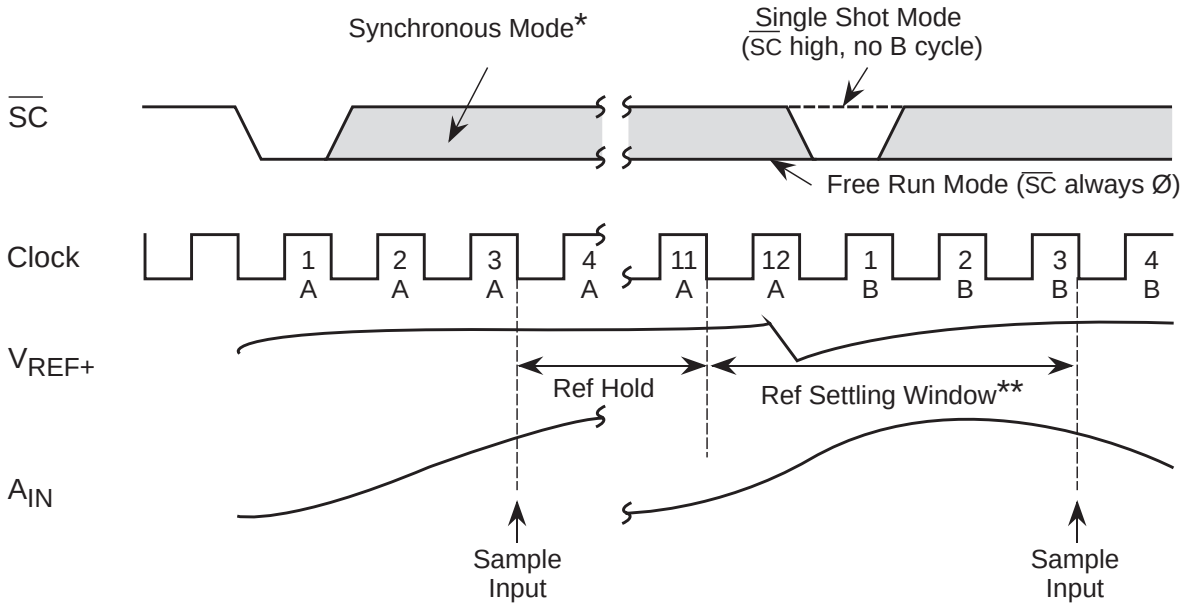


Figure 9 - Analog Input Track-and-Hold Timing and Reference Settling-and-Hold Timing

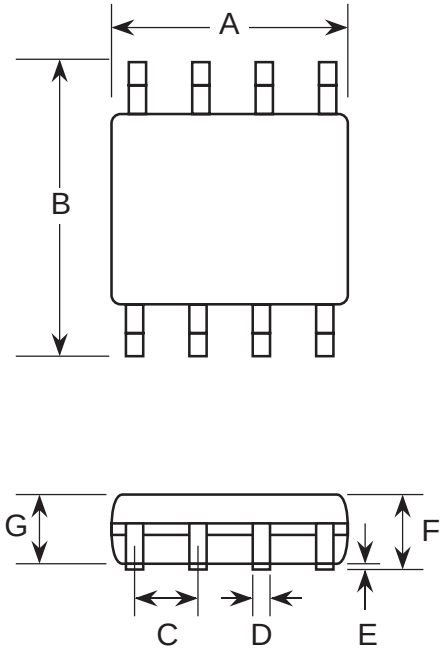


* The rising edge of the $\overline{SC}$ line can occur any time between the rising edge of clock 1A and the falling edge of clock 12A.

** The reference settling window can be extended in the synchronous mode by adding extra clocks between conversion cycles. The example shown is the minimum number of clocks required (12) per conversion cycle.

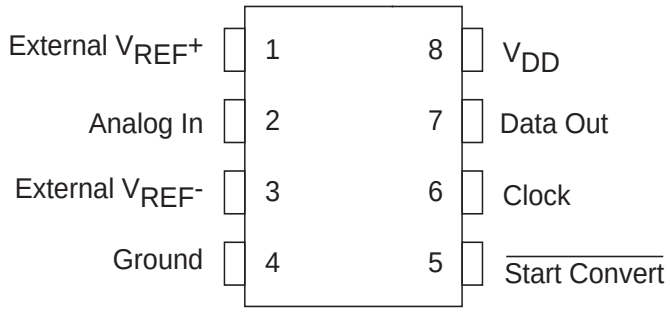
PACKAGE OUTLINE

8-Lead SOIC



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.187	0.194	4.80	4.98
B	0.228	0.242	5.84	6.20
C	0.050 typ		1.27 typ	
D	0.014	0.019	0.35	0.49
E	0.005	0.010	0.13	0.25
F	0.060	0.067	1.55	1.73
G	0.055	0.060	1.40	1.55
H	0.149	0.156	3.81	3.99
I	0°	8°	0°	8°
J	0.007	0.010	0.19	0.25
K	0.016	0.035	0.41	0.89

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
Analog In	Analog Signal Input
$\overline{\text{Start Convert}}$	Start Convert. A high-to-low transition on this input begins the conversion cycle and enables serial data output.
Clock	Clock that drives A/D conversion cycle and the synchronous serial data output
Data Out	Serial Data. Tri-state serial data output for the A/D result driven by the CLOCK input
External $V_{REF}+$	External voltage reference for top of reference ladder
External $V_{REF}-$	External voltage reference for bottom of reference ladder
V_{DD}	Analog and Digital +3 V to +5 V Power Supply Input
GND	Analog and Digital Ground

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT7730SCS	0 to +70 °C	8L SOIC
SPT7730SCU*	+25 °C	Die*

*Please see the die specification for guaranteed electrical performance.