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TMB22153AMS100

Demonstration Board for the TMC22x5yA Multistandard Digital Video Decoder

Features

- Accepts analog composite or YC
- Outputs 10-bit digital RGB, D1, or YC_BC_R
- Locks to studio reference
- R-bus serial interface compatibility
- Raytheon demo board compatibility

Applications

- Evaluation of TMC22x5yA Digital Video Decoder
- Input for Genesis 10-bit Line Doubler board
- Input for DAC and encoder demo boards
- System Breadboarding

Related Products

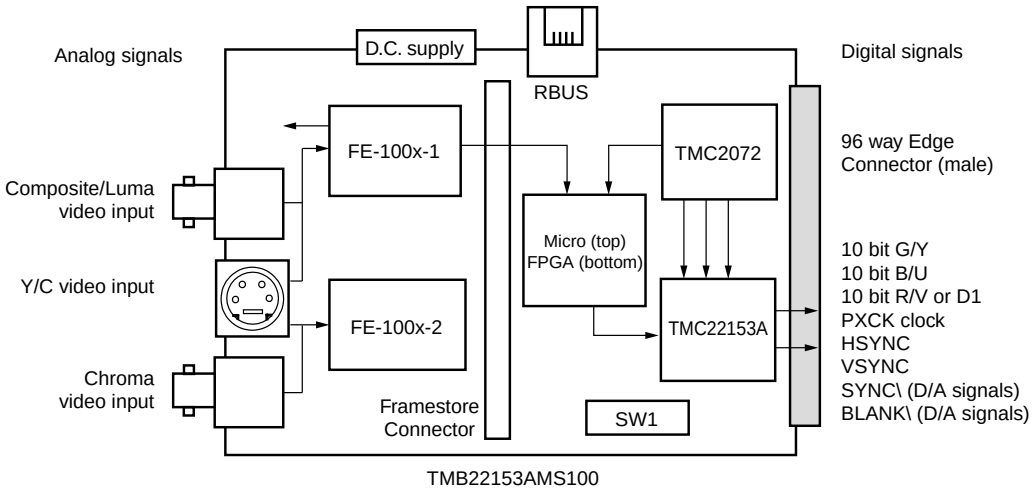
- TMC2069P7C DAC demonstration board
- TMC2074P7C Encoder demonstration board
- TMB2193MS100 Encoder demonstration board
- TMC2070P7C R-bus interface board
- Raydemo software

Description

The TMB22153AMS100 Demonstration Board showcases the TMC22x5yA Digital Video Decoder. The onboard MMC FE-100 dual 10-bit A/D modules generate digitized composite or YC for the decoder. The decoder outputs D1, digital RGB, or YC_BC_R. Clocks and synchronization pulses are generated by Fairchild's TMC2072 Genlocking Video Digitizer.

Preliminary Information

Block Diagram



Rev. 001

Functional Description

The TMB22153AMS100 is designed to demonstrate the performance of the TMC22x5yA Digital Video Decoder. For complete descriptions of the TMC22x5yA, TMC2072, TMC1185, and TMC2242 please refer to part datasheets. The TMB22153AMS100 is designed to be used in conjunction with other Fairchild demo boards, namely the TMC2069P7C DAC, and TMB2193MS100 encoder boards. The 96 pin edge connectors plug easily into each other. When used together, the boards demonstrate a high performance 10-bit digital video decoding system.

TMC22x5yA Digital Video Decoder

The TMC22x5yA accepts digitized video input on two 10-bit buses, “YOVER[9:0]” and “COVER[9:0]”. Based on the status of its control registers, it then outputs the data to the output edge connector of the board in a variety of formats. Please see Table 1 for a listing of board default video standards and output formats that are loadable to the control registers.

After the TMC22x5yA control registers have been initially loaded by the microcontroller, subsequent changes to the control registers may be made through the R-bus interface and Raydemo software.

It is important that the control registers be loaded correctly in order to obtain the desired output. Once the control registers have been set to output the correct data from the TMC22x5yA, then several board switches must also be correctly configured in order to obtain the desired output.

TMC2072 Genlocking Video Digitizer

The TMC2072 Genlocking Video Digitizer accepts analog composite data through the composite input BNC on the left side of the board. A 20MHz clock crystal provides the Genlock with an input clock. The TMC2072 outputs horizontal and vertical syncs, and a 27MHz clock. The clock is used to drive the Decoder and EPLD. Like the TMC22x5yA, the Genlock part must be programmed at startup. Instructions on how to do this are in the “Microcontroller” section of this documentation.

EPLD

An Altera EPF10K10TC144-4 EPLD executes several essential board functions. The EPLD serves as a buffer and multiplexer for data buses and a register for several important control signals. These signals may be cross-referenced to the included schematics. The EPLD control registers may be modified using the Raydemo software. The Raydemo EPLD R-bus address is 0000001. For a more complete description or specification of signals going to or coming from the TMC22x5yA and TMC2072, please refer to the Fairchild Semiconductor Data Book (also available on CD-ROM) or the website at www.fairchildsemi.com.

Microcontroller

An Atmel 89C55 microcontroller is used to program the TMC22x5yA and TMC2072 registers. The microcontroller programs the parts through the R-bus at power up and reprograms them each time the “Reset” button is pushed. Please see Table 1 on the next page for a description of available microcontroller-programmed board configurations.

Table 1. TMB22153AMS100 Demonstration Board Video Standard Selection

P_{3-0}	Input Format	Video Standard	Output Format
0000	composite	NTSC	YUV
0001	Y/C	NTSC	YUV
0010	composite	NTSC	D1
0011	Y/C	NTSC	D1
0100	composite	NTSC	RGB
0101	composite, field-based	NTSC	YUV
0110	composite, field-based	NTSC	D1
0111	composite, frame-based	NTSC	YUV
1000	composite	PAL	YUV
1001	Y/C	PAL	YUV
1010	composite	PAL	D1
1011	Y/C	PAL	D1
1100	composite	PAL	RGB
1101	composite, field-based	PAL	YUV
1110	composite, field-based	PAL	D1
1111	reserved		

Quick Setup/Verification for Composite NTSC Input, YUV Output

1. Configure jumpers:

   If using R-Bus interface, JP2 must be closed (connected)

   Leave JP1 open (unconnected)

   Verify that JP4 is linked to the odd-numbered pins of JP6

2. Configure slider-switches (push red slider TOWARD specified marking on board) :

E1	“FPGA”
E2	“FPGA”
E3	“VS”
E4	“PXCK4\”
E5	“GP”
E6	“GH”
E7	“GV”
E8	“XP”

3. If you have reason to believe the bottom cover has been removed, remove it and configure S4 as follows:

1-7	ON (low)
8	OFF (high)

4. Ensure BNC J1 (VIN1) is connected to composite NTSC signal.

5. Ensure piano-key switches $P_{3\text{-}0}$, Y are in the “LOW” (down) position.

6. Plug in power-supply connector and apply power. LED’s corresponding to applied voltages should light-up.

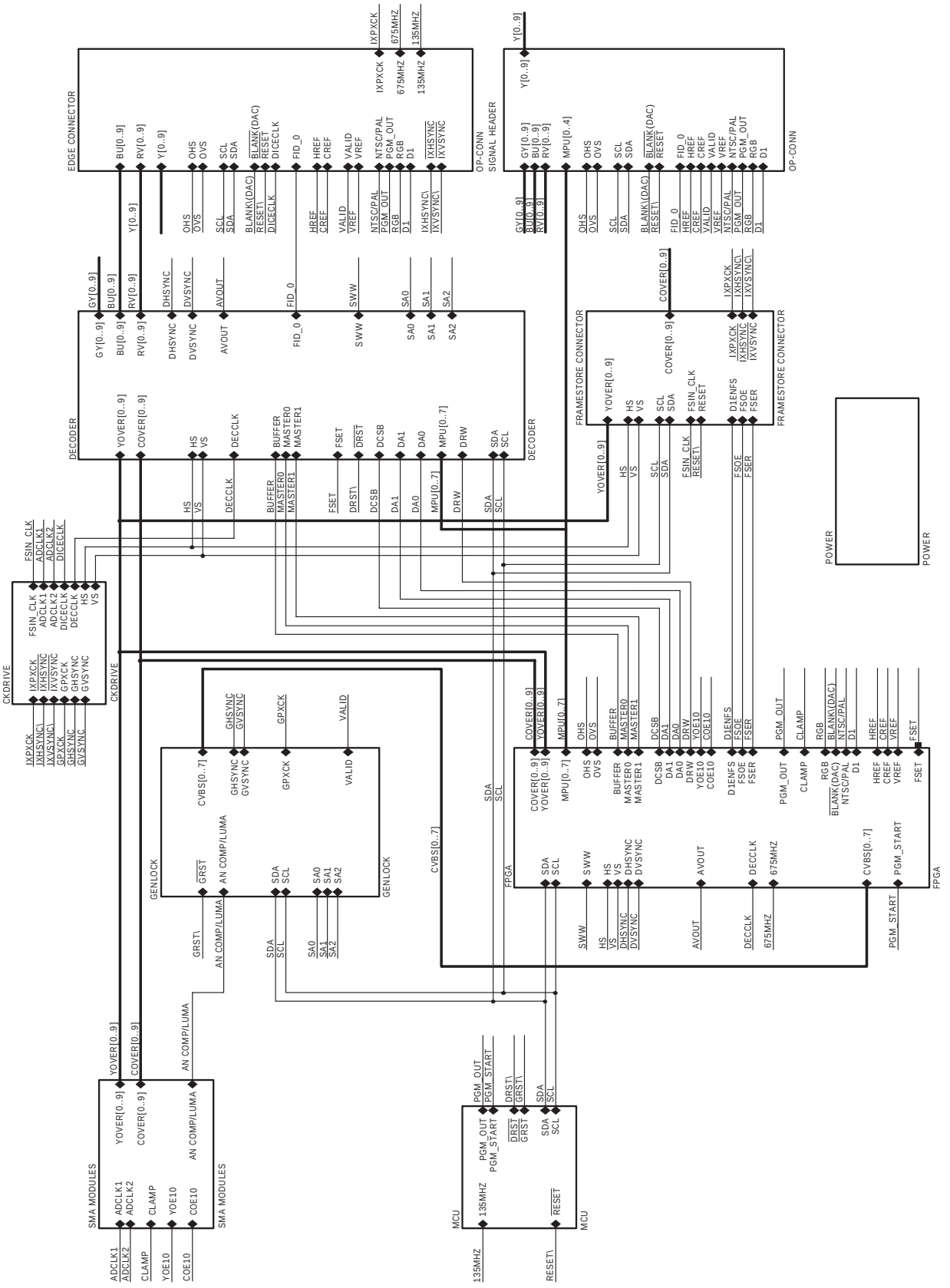
7. Press and release the MRST button (S2). The TMC2072 and TMC22x5yA should both be programmed. To verify the TMC2072 is functioning correctly, check for presence of a clock (TP sync pulses, VS (TP18) and HS (TP17). Likewise, to verify the TMC22x5yA is functioning, check for presence of DHSYNC (TP5) and DVSYNC (TP6).

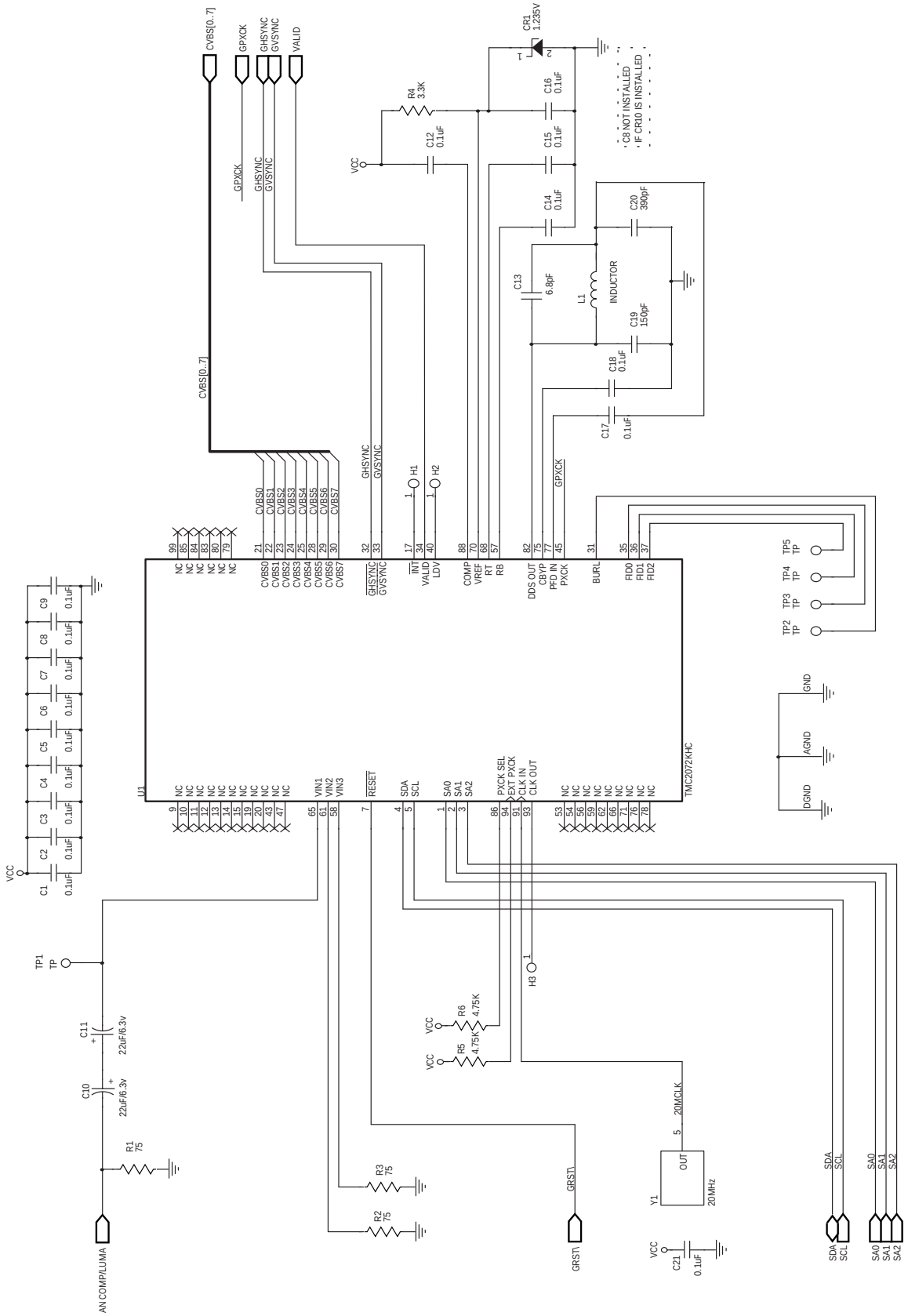
Power Supply Requirements

The TMB22153AMS100 power supply connector is on the top edge of the board toward the left side. The TMB22153AMS100 board requires DC power supply voltages of +5V and -5V.

The +5V supply provides power and voltage references to the TMC22x5yA and /TMC2072, as well as driving TTL logic devices. It is for this reason that a bench power supply with short cable lengths is recommended.

Preliminary Information





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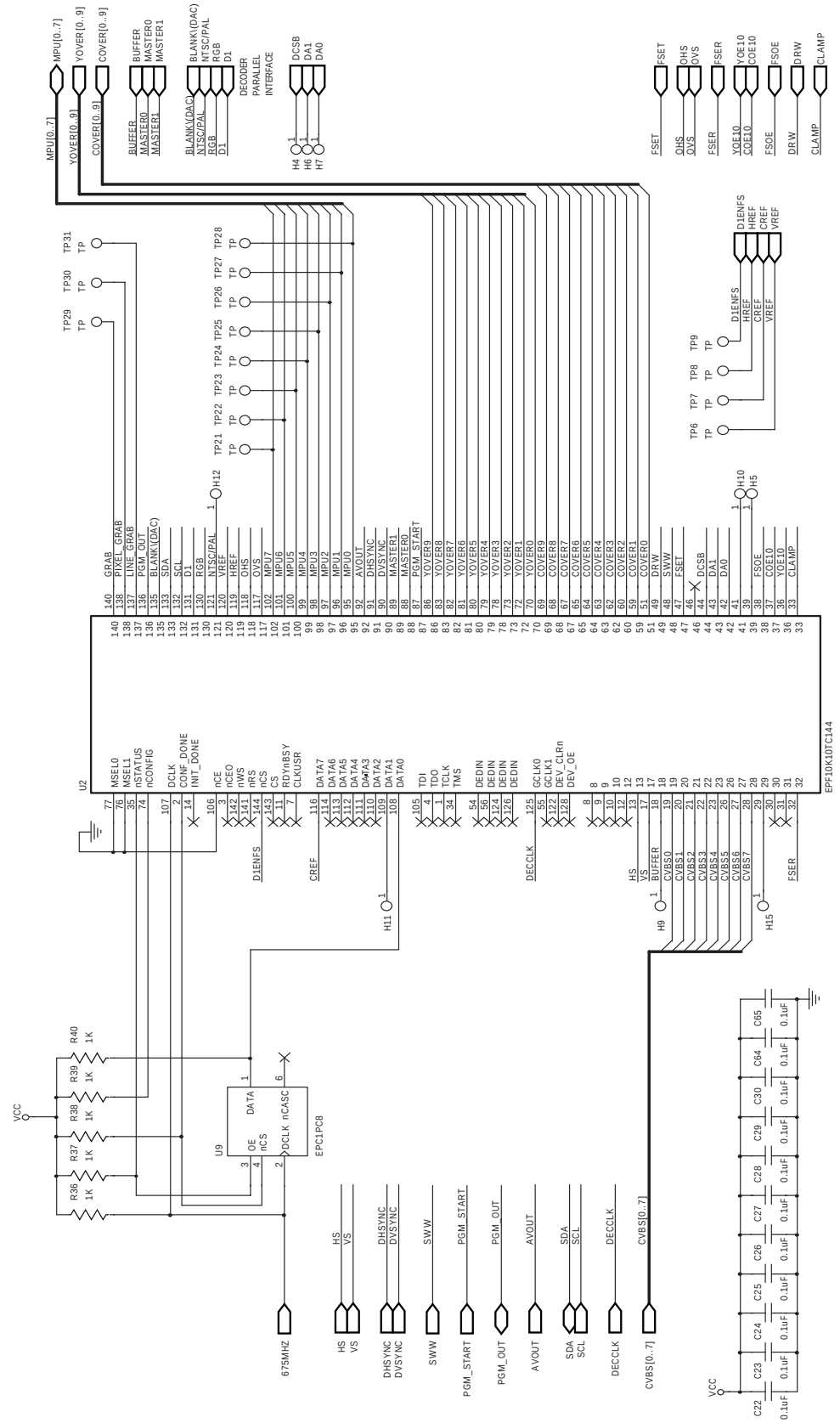

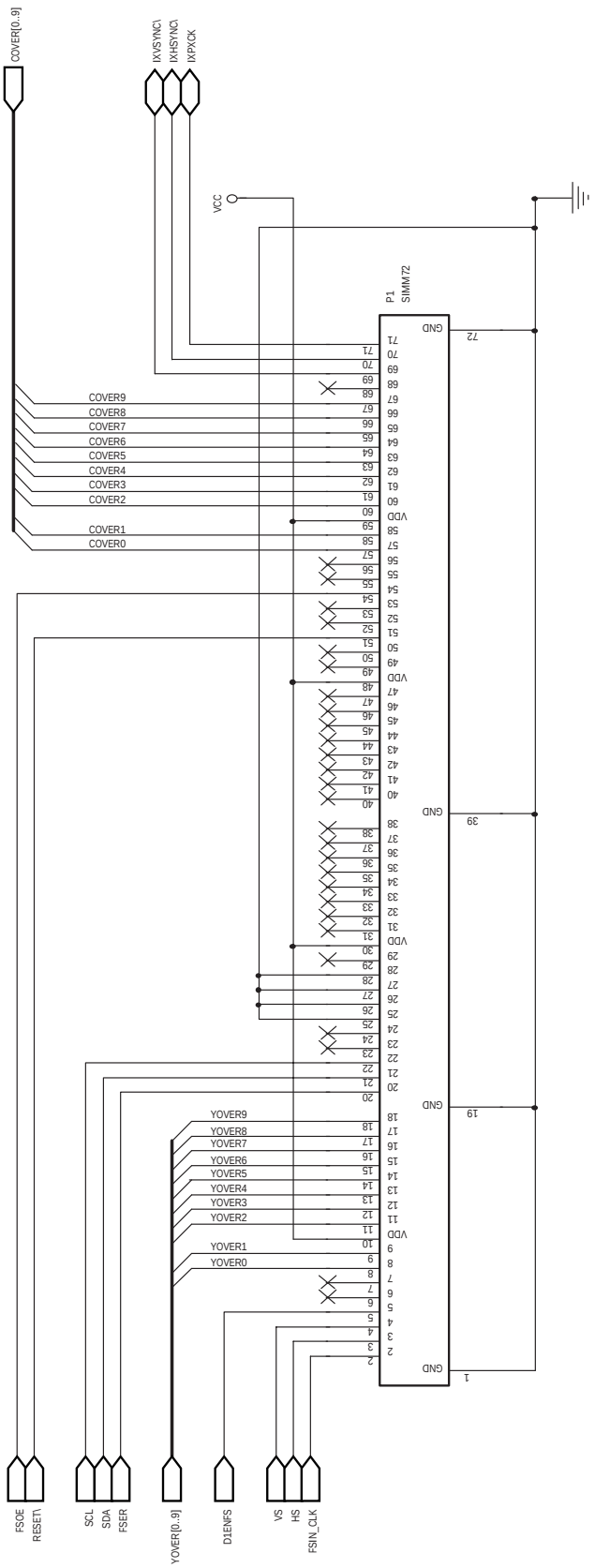

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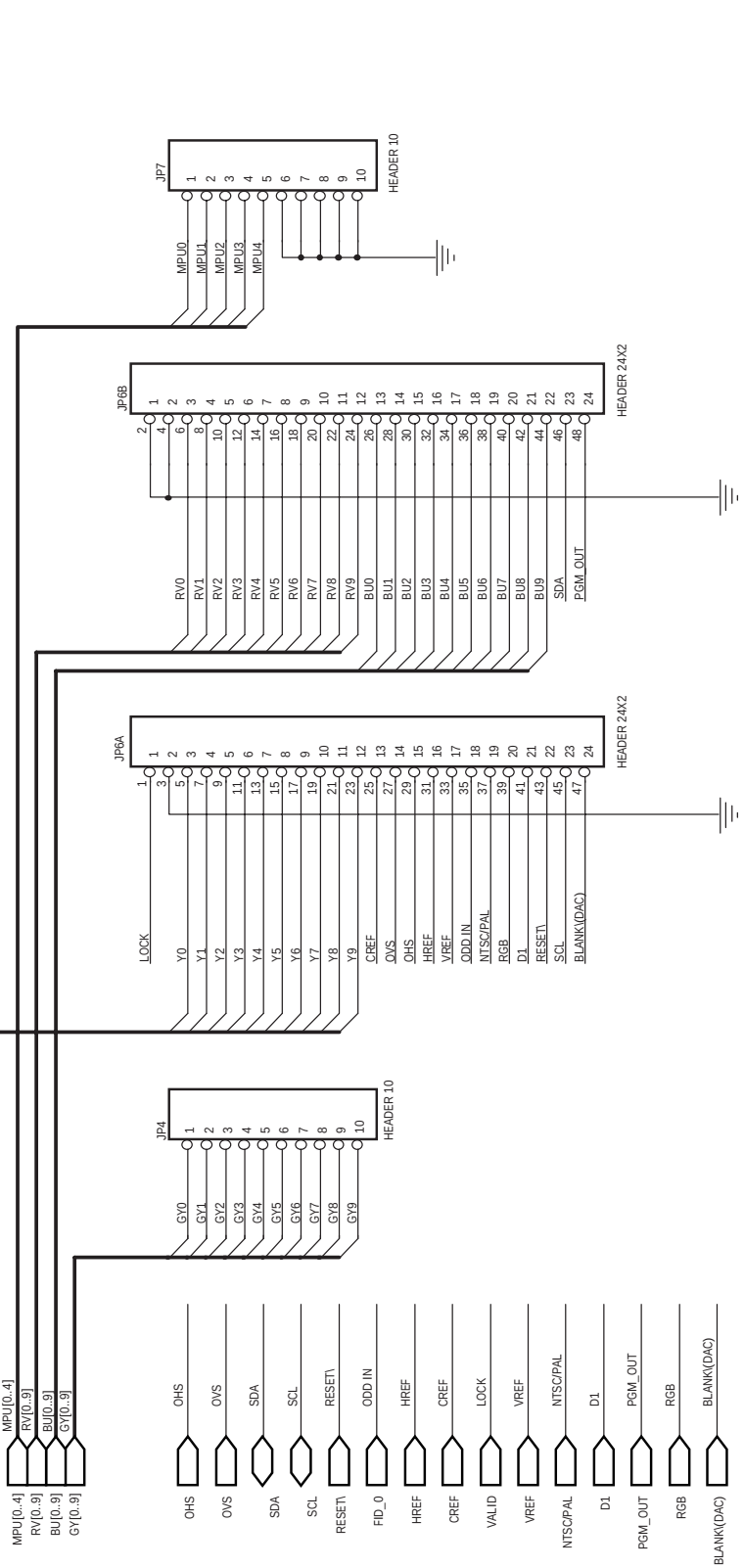

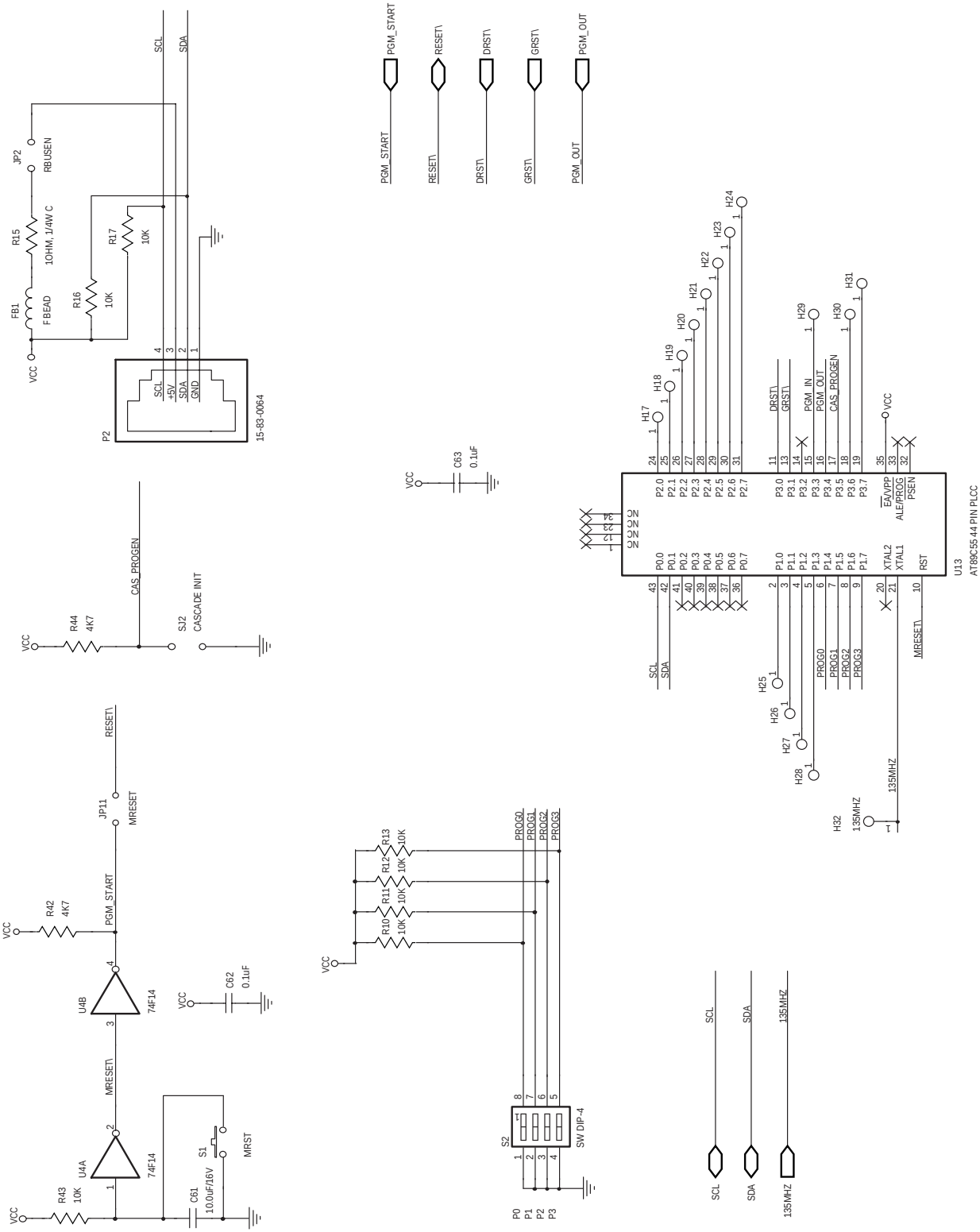

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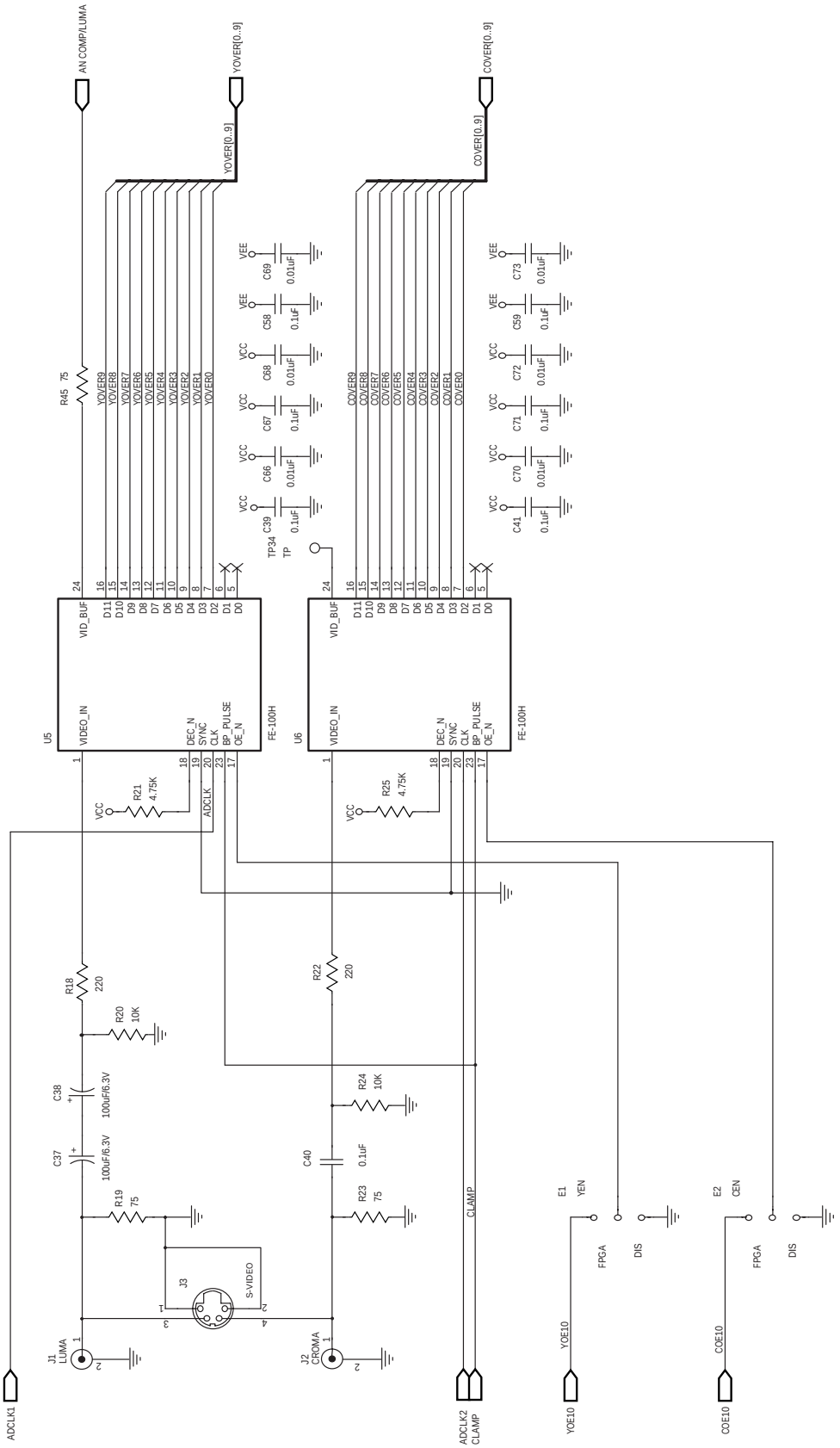

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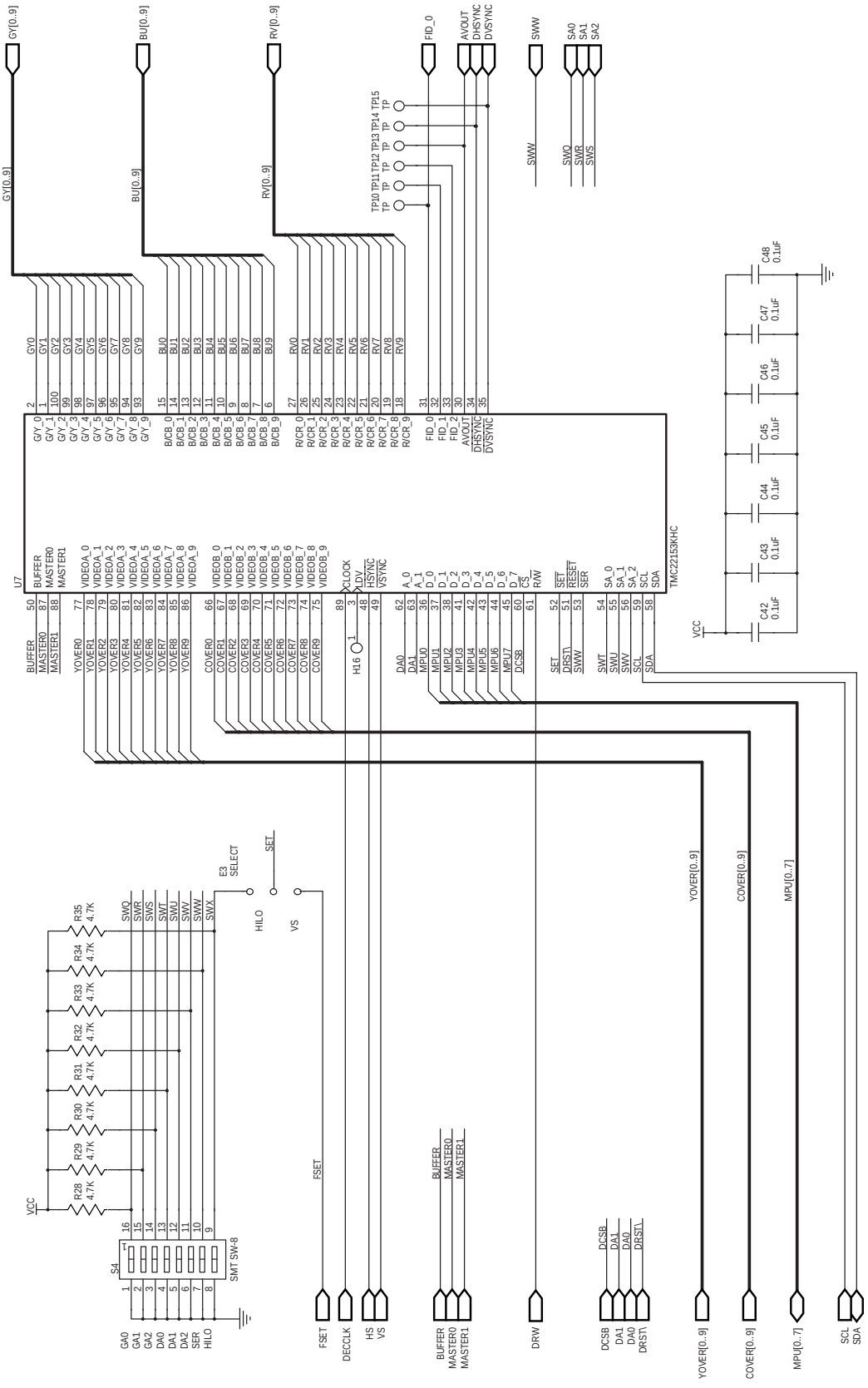

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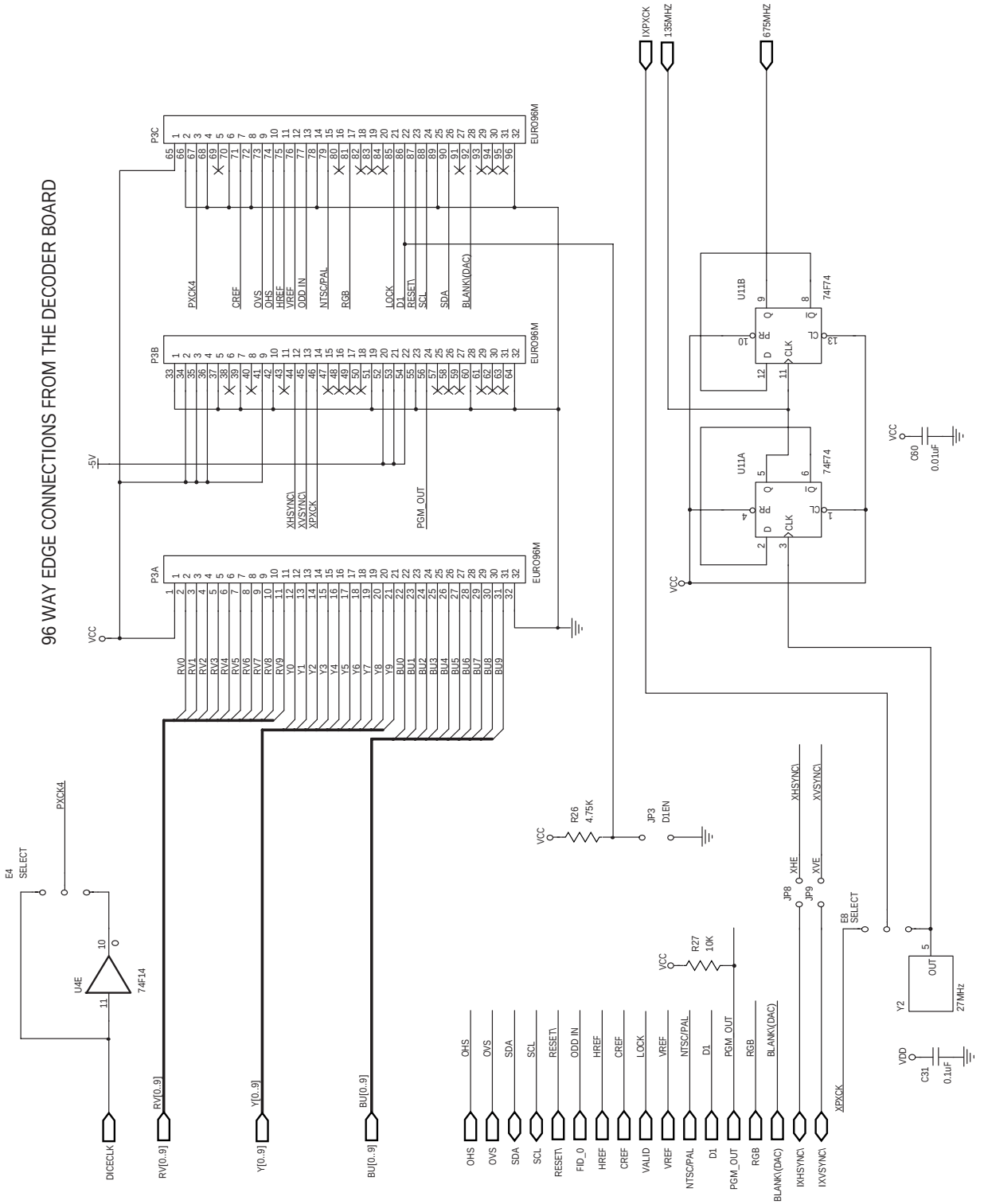
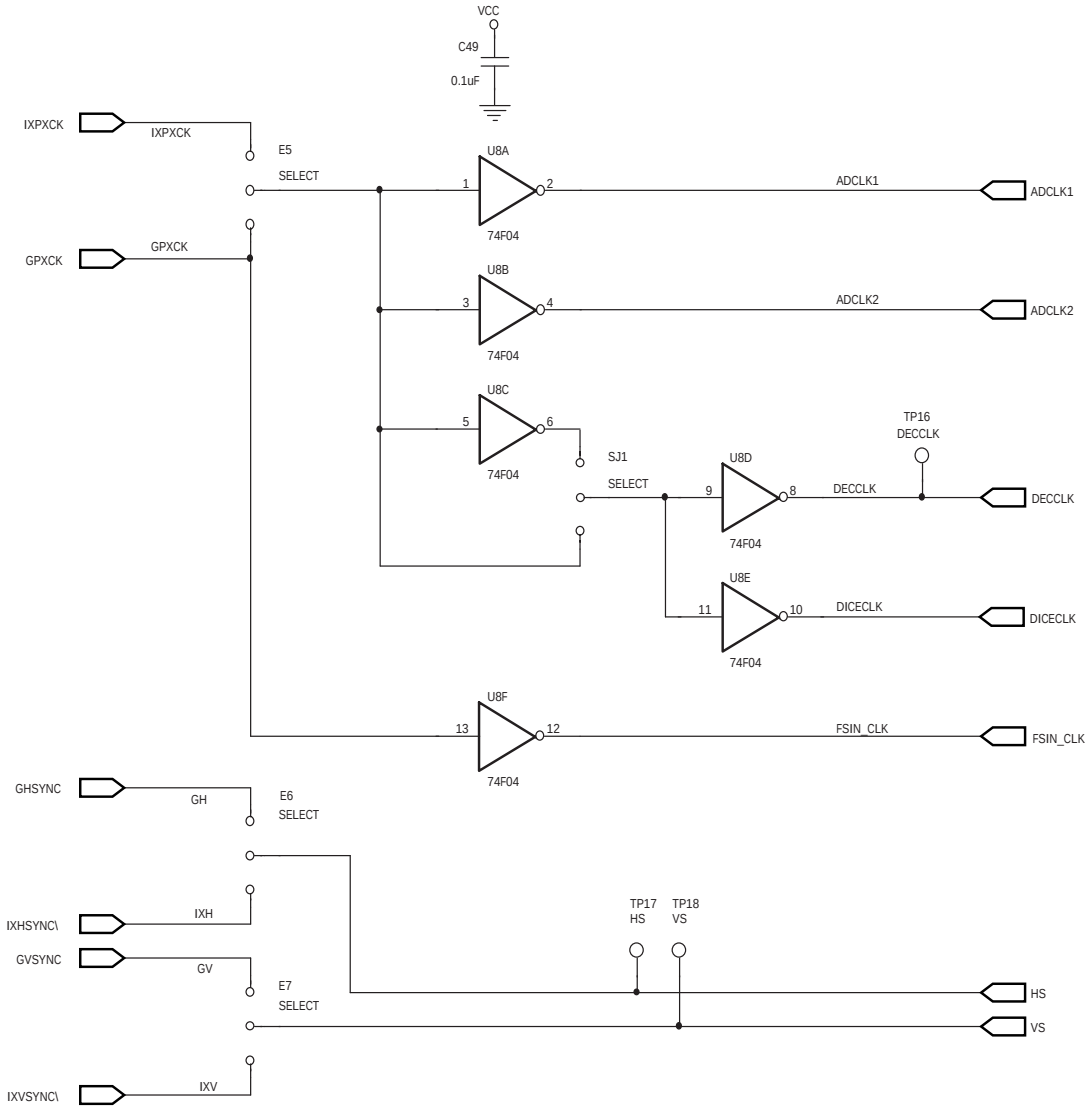
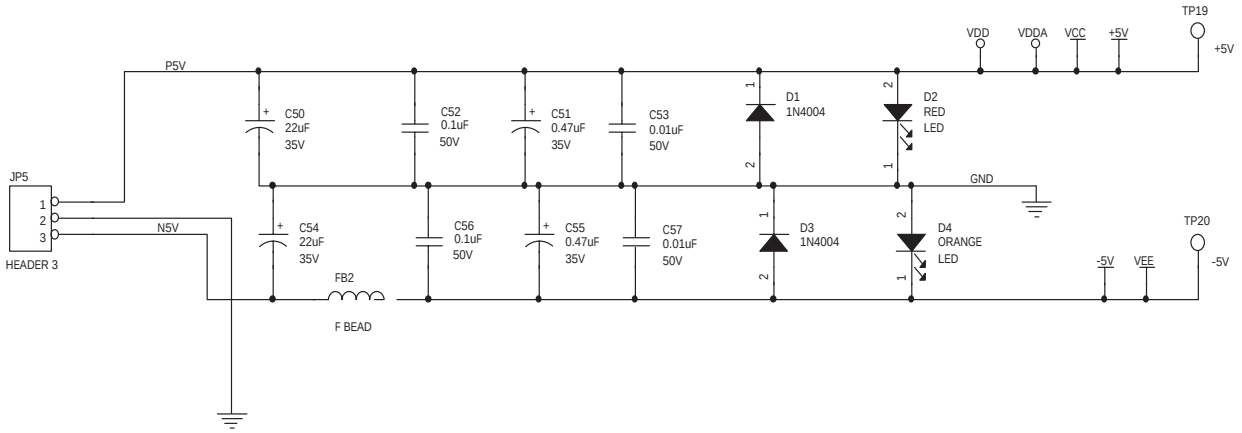
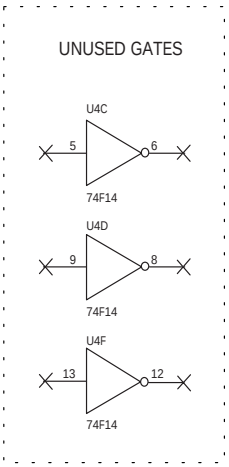
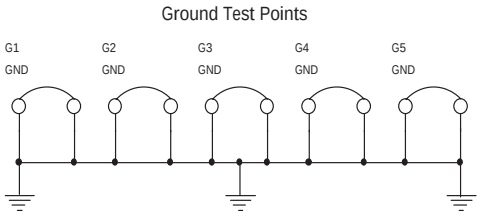










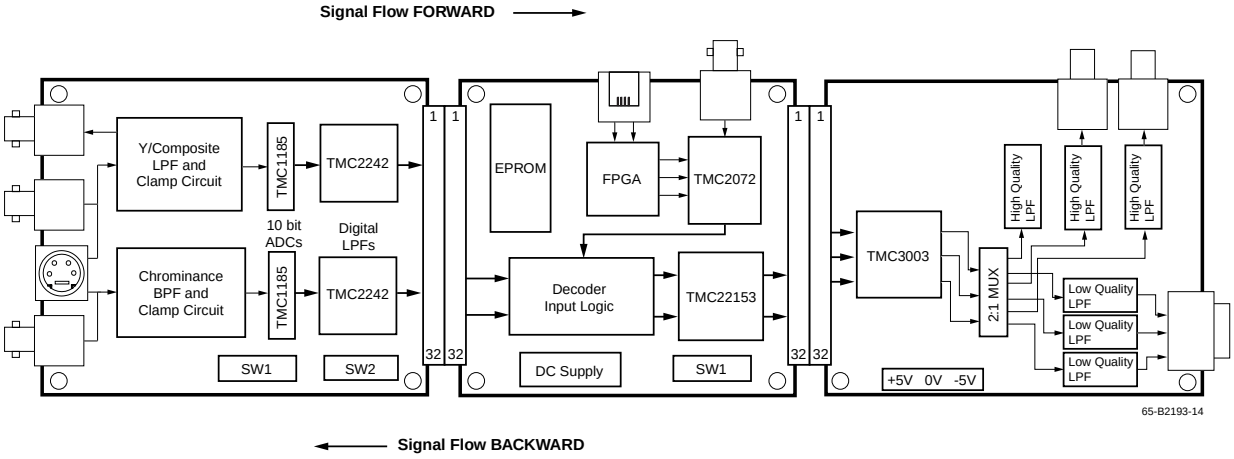
Preliminary Information

OUTPUT

96 way connector (male) description and notes

row A		row B		row C	
1	+5v	1	**GND**	1	**+5v**
2	D1 or R/V [bit 0]	2	**+5V**	2	**GND**
3	D1 or R/V [bit 1]	3	**+5V**	3	PXCK
4	D1 or R/V [bit 2]	4	**+5V**	4	**GND**
5	D1 or R/V [bit 3]	5	**GND**	5	PCK
6	D1 or R/V [bit 4]	6	***Analog Composite/luma***	6	**GND**
7	D1 or R/V [bit 5]	7	**GND**	7	CREF
8	D1 or R/V [bit 6]	8	***Analog chroma***	8	**GND**
9	D1 or R/V [bit 7]	9	XEN	9	VSYNC\
10	D1 or R/V [bit 8]	10	**GND**	10	HSYNC\
11	D1 or R/V [bit 9]	11	XDIR	11	HREF
12	Comp, G/Y, or Luma [bit 0]	12	XHSYNC\	12	VREF
13	Comp, G/Y, or Luma [bit 1]	13	XVSYNC\	13	ODD IN
14	Comp, G/Y, or Luma [bit 2]	14	XPXCK	14	**GND**
15	Comp, G/Y, or Luma [bit 3]	15	XRS [bit 3]	15	NTSC/PAL
16	Comp, G/Y, or Luma [bit 4]	16	XRS [bit 2]	16	CLAMP pulse
17	Comp, G/Y, or Luma [bit 5]	17	XRS [bit 1]	17	RGB
18	Comp, G/Y, or Luma [bit 6]	18	XRS [bit 0]	18	
19	Comp, G/Y, or Luma [bit 7]	19	**GND**	19	
20	Comp, G/Y, or Luma [bit 8]	20	**-5V**	20	
21	Comp, G/Y, or Luma [bit 9]	21	**-5V**	21	LOCK
22	Chroma or B/U [bit 0]	22	**-5V**	22	D1
23	Chroma or B/U [bit 1]	23	**GND**	23	RESET\
24	Chroma or B/U [bit 2]	24	PGM_OUT	24	SCL
25	Chroma or B/U [bit 3]	25	**-12V**	25	**GND**
26	Chroma or B/U [bit 4]	26	**-12V**	26	SDA
27	Chroma or B/U [bit 5]	27	IE (input enable)	27	OE (output enable)
28	Chroma or B/U [bit 6]	28	**GND**	28	BLANK\ (DAC)
29	Chroma or B/U [bit 7]	29		29	
30	Chroma or B/U [bit 8]	30		30	
31	Chroma or B/U [bit 9]	31	**+12V**	31	**+12V**
32	**GND**	32	**GND**	32	**GND**

Output Edge Connector Design notes:



1. Boards with different revision letters may not be compatible; damage may occur if they are connected together.
2. XPXCK is a two times pixel clock fed BACKWARD
3. XHSYNC and XVSYNC are timing reference signals fed BACKWARD
4. The MASTER/SLAVE signal states if a board is a MASTER or a SLAVE board. This signal is fed FORWARD. A MASTER board produces the PXCK, HSYNC, and VSYNC signals, and a SLAVE board expects to receive XPXCK, XHSYNC, XVSYNC, etc.
5. XDIR is fed FORWARD and controls in which direction the XRS[3:0] data flows.
6. PGM_OUT negative going signal pulse for initiating programming of down stream boards, generated once the devices on the board have been programmed. Care must be taken to ensure that multiple devices do not try to drive the RBUS at any given time. The Minimum width of PGM_OUT is 1µS.
7. The RESET pin on the output edge connector should be connected directly to the RESET pin on the input connector. A link should be used to connect any pulse to the RESET line.
8. The MASTER/SLAVE, XDIR, PGM_OUT and RESET pins on the output edge connector should be connected to +5V through a 10k pull up resistor.
9. The CLAMP signal is fed BACKWARD from a MASTER to a SLAVE board. The CLAMP signal should not be fed FORWARD.

Table 4. TMB22153AMS100 Parts List

Item	Qty.	Reference Designator	Description
1	1	CR1	1.235 V
2	47	C1, C2, C3, C4, C5, C6, C7, C8, C9, C12, C14, C15, C16, C17, C18, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C52, C56, C58, C59, C62, C63, C64, C65, C67, C71	0.1 µF
3	2	C10, C11	0.01 µF
4	1	C13	6.8 pF
5	1	C19	150 pF
6	1	C20	390 pF
7	2	C37, C38	100 uF / 6.3 V
8	2	C50, C54	22 µF
9	2	C51, C55	0.47 µF
10	9	C53, C57, C60, C66, C68, C69, C70, C72, C73	0.01 µF
11	1	C61	10.0 µF / 16V
12	2	D1, D3	1N4004
13	1	D2	LED RED
14	1	D4	LED ORANGE
16	9	SJ1, E1, E2, E3, E4, E5, E6, E7, E8	SELECT
17	2	FB1, FB2	F BEAD
18	5	G1, G2, G3, G4, G5	GND LOOP
19	29	H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, H20, H21, H22, H23, H24, H25, H26, H27, H28, H32	PTH
20	5	JP2, JP3, JP8, JP9, JP11	HEADER2
21	2	JP4, JP7	HEADER10
22	1	JP6	HEADER24X2
23	1	J1	BNC LUMA
24	1	J2	BNC CHROMA
25	1	J3	CON S-VIDEO
26	1	L1	INDUCTOR
27	1	P1	HEADER72X2 SIMM72
28	1	P2	15-83-0064
29	1	P3	EURO96M
30	5	R1, R2, R3, R19, R23	75 OHM
31	1	R4	3.3 KOHM
32	5	R5, R6, R21, R25, R26	4.75 KOHM
33	10	R10, R11, R12, R13, R16, R17, R20, R24, R27, R43	10 KOHM
34	1	R15	1 OHM / 1/4W C
35	3	R18, R22, R45	220 OHM
36	10	R28, R29, R30, R31, R32, R33, R34, R35, R42, R44	4.7 KOHM
37	5	R36, R37, R38, R39, R40	1 KOHM
38	1	SJ2	CASCADE INIT
39	1	S1	PUSHBUTTON MRST

Item	Qty.	Reference Designator	Description
40	1	S2	SW DIP-4
41	1	S4	SW DIP-8
42	32	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP34	TP
43	1	U1	TMC2072KHC
44	1	U2	EPF10K10TC144
45	1	U4	74F14
46	2	U5, U6	FE-100H
47	1	U7	TMC22153AKHC
48	1	U8	74F04
49	1	U9	EPC1PC8
50	1	U11	74F74
51	1	U13	AT89C55 44 PIN PLCC
52	1	Y1	20MHz CRYSTAL
53	1	Y2	27MHz CRYSTAL

Notes:

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMB22153AMS100	25°C	27 MHz	Commercial	4" by 5" Printed Circuit Board	TMB22153AMS100

The TMC2070P7C parallel port to R-bus board, interface cable, Raydemo software, and all relevant documentation are included in the TMB22153AMS100 purchase price.

A schematic database is available in OrCAD™ format, along with EPROM maps. More information on the EPLD/FPGA design is also available. Contact the factory.

The TMB22153AMS100 Demonstration Board, design documentation, and software are provided as a design example for the customers of Fairchild. Fairchild makes no warranties, express, statutory, or implied regarding merchantability or fitness for a particular purpose.

Preliminary Information