FAIRCHILD

SEMICONDUCTOR™

74LCX27
Low Voltage Triple 3-Input NOR Gate with 5V Tolerant Inputs

General Description

The LCX27 contains three 3-input NOR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX27 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 2.3V–3.6V V_{CC} specifications provided
- 4.9 ns t_{PD} max (V_{CC} = 3.3V), 10 µA I_{CC} max
- Power down high impedance inputs and outputs
- ±24 mA output drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
   Human body model > 2000V
    Machine model > 200V

Ordering Code:

Order Number	Package Number	Package Description
74LCX27M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74LCX27SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX27MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

IEEE/IEC
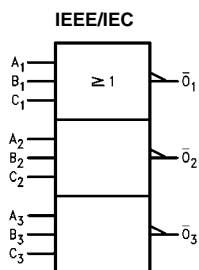
Connection Diagram
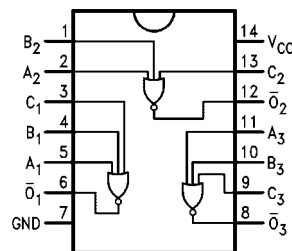
Pin Descriptions

Pin Names	Description
A_n, B_n, C_n	Inputs
$\overline{O}_n$	Outputs

Truth Table

$$\overline{O}_n = A_n + B_n + C_n$$

Inputs			Output
A_n	B_n	C_n	$\overline{O}_n$
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

H = HIGH Voltage Level   L = LOW Voltage Level   X = Immaterial

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74LCX27

Absolute Maximum Ratings(Note 1)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 3)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V – 3.6V		±24	mA
		V_{CC} = 2.7V - 3.0V		±12	
		V_{CC} = 2.3V - 2.7V		±8	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.3 – 3.6	V_{CC} − 0.2		V
		I_{OH} = −8 mA	2.3	1.8		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.3 – 3.6		0.2	V
		I_{OL} = 8mA	2.3		0.6	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.3 – 3.6		±5.0	µA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	µA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.3 – 3.6		10	µA
		3.6V ≤ V_I ≤ 5.5V	2.3 – 3.6		±10	
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.3 – 3.6		500	µA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°CF$, $R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		$C_L = 50pF$		$C_L = 50pF$		$C_L = 30pF$		
		Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	4.9	1.5	5.8	1.5	5.9	ns
t_{PLH}		1.5	4.9	1.5	5.8	1.5	5.9	
t_{OSHL}	Output to Output Skew (Note 4)		1.0					ns
t_{OSLH}			1.0					

Note 4: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Unit
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	−0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	−0.6	

Capacitance

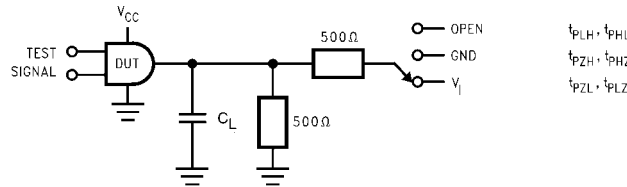| Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	25	pF

AC LOADING and WAVEFORMS Generic for LCX Family

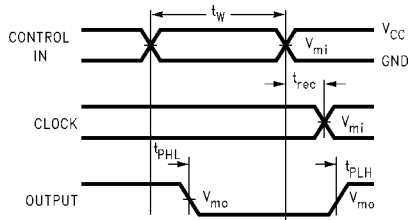FIGURE 1. AC Test Circuit (C$_L$ includes probe and jig capacitance)

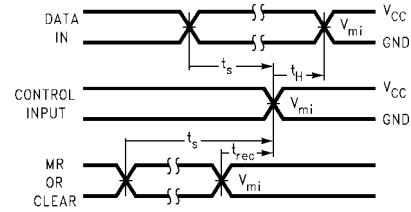| Test	Switch
t$_{PLH}$, t$_{PHL}$	Open
t$_{PZL}$, t$_{PLZ}$	6V at V$_{CC}$ = 3.3 ± 0.3V V$_{CC}$ x 2 at V$_{CC}$ = 2.5 ± 0.2V
t$_{PZH}$,t$_{PHZ}$	GND
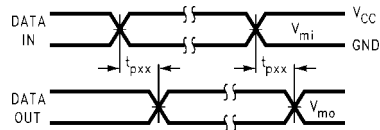
Waveform for Inverting and Non-Inverting Functions
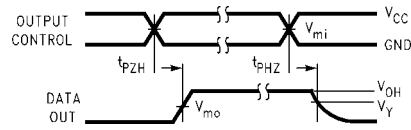
3-STATE Output High Enable and Disable Times for Logic

Propagation Delay. Pulse Width and t$_{rec}$ Waveforms

Setup Time, Hold Time and Recovery Time for Logic
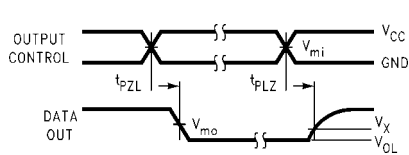
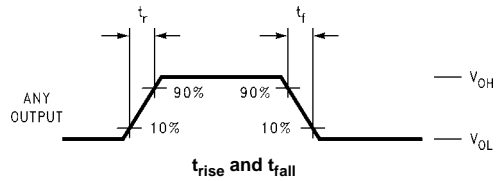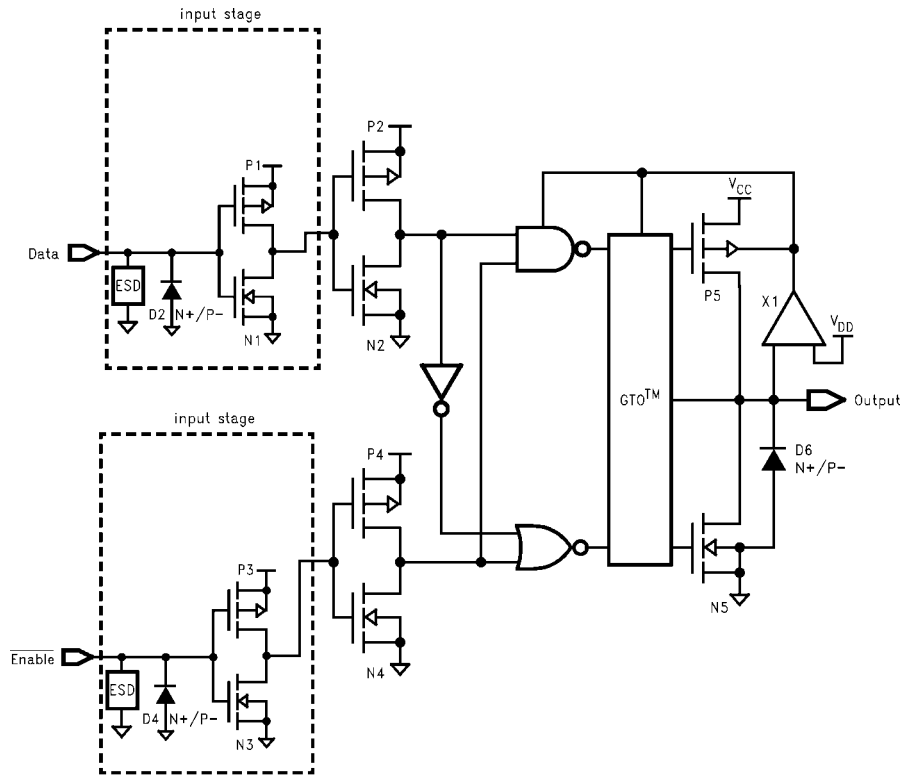**3-STATE Output Low Enable and Disable Times for Logic**

t$_{rise}$ and t$_{fall}$

FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t$_r$ = t$_f$ = 3ns)

Symbol	V$_{CC}$		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V$_{mi}$	1.5V	1.5V	V$_{CC}$/2
V$_{mo}$	1.5V	1.5V	V$_{CC}$/2
V$_x$	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.15V
V$_y$	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.15V

Schematic Diagram Generic for LCX Family

Physical Dimensions inches (millimeters) unless otherwise noted

0.335 – 0.344
(8.509 – 8.738)

14 13 12 11 10 9 8

0.228 – 0.244
(5.791 – 6.198)

LEAD NO. 1
IDENT

1 2 3 4 5 6 7

30°
TYP

0.010 MAX
(0.254)

0.150 – 0.157
(3.810 – 3.988)

0.010 – 0.020
(0.254 – 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 – 0.010
(0.203 – 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS

0.053 – 0.069
(1.346 – 1.753)

0.004 – 0.010
(0.102 – 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP
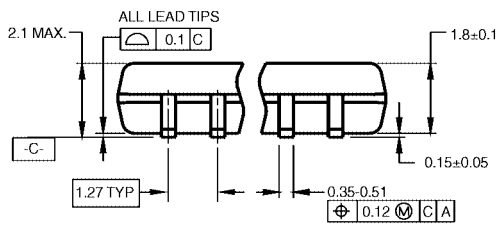
0.014 – 0.020
(0.356 – 0.508) TYP

M14A (REV H)
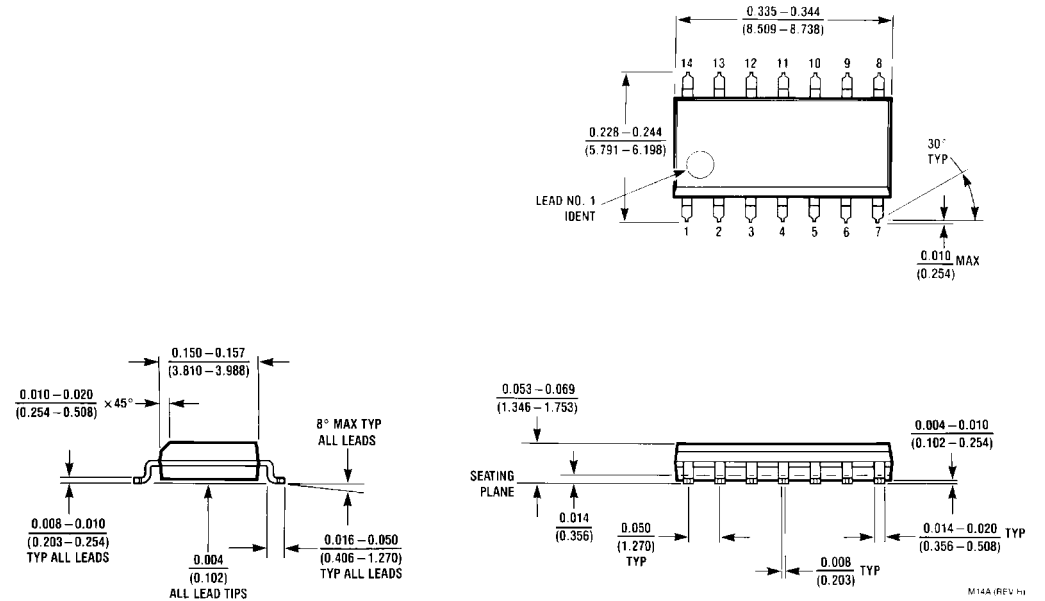
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

10.2±0.1

-A-

1.1 TYP

14   8

7.8

3.9

5.3±0.1

-B-

△ 0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

1   7

LAND PATTERN RECOMMENDATION

14   13   9   8

5.01 TYP

9.27 TYP

(2.13 TYP)

1   2   6   7

1.27 TYP   0.6 TYP

ALL LEAD TIPS

2.1 MAX.

△ 0.1 C

1.8±0.1

-C-

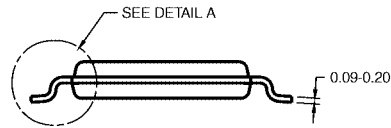0.15±0.05
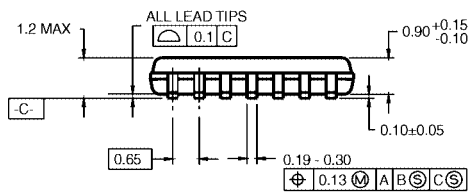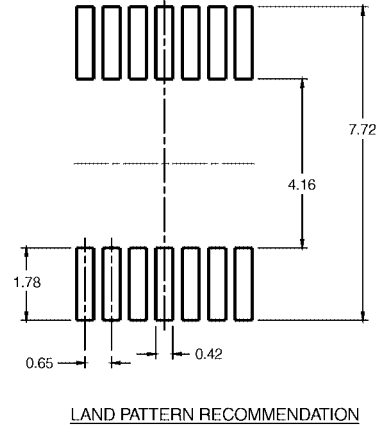
1.27 TYP   0.35-0.51

⊕ 0.12 Ⓜ C A

DIMENSIONS ARE IN MILLIMETERS
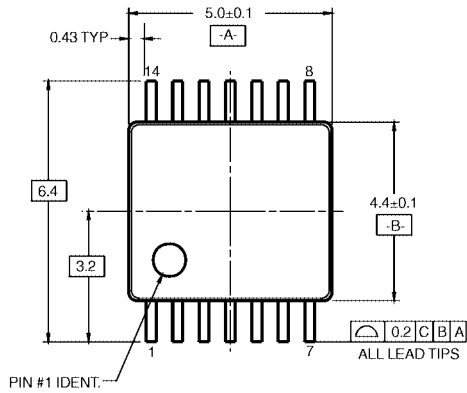
NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

SEE DETAIL A

0.15-0.25

7° TYP

GAGE PLANE

0.25

0°-8° TYP

0.60±0.15

1.25

SEATING PLANE

DETAIL A

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

5.0±0.1
-A-

0.43 TYP

14   8

6.4

3.2

4.4±0.1
-B-

⌒ 0.2 C B A
ALL LEAD TIPS

1   7

PIN #1 IDENT.

LAND PATTERN RECOMMENDATION

7.72

4.16

1.78

0.65   0.42

0.65

ALL LEAD TIPS
⌒ 0.1 C

1.2 MAX

-C-

0.90 +0.15 -0.10

0.10±0.05

0.19 - 0.30

⊕ 0.13 Ⓜ A BⓈ CⓈ

SEE DETAIL A

0.09-0.20

12.00° TOP & BOTTOM

R0.09 MIN

GAGE PLANE

0.25

0°-8°

0.6 ±0.1

1.00

SEATING PLANE

R0.09 MIN

DETAIL A
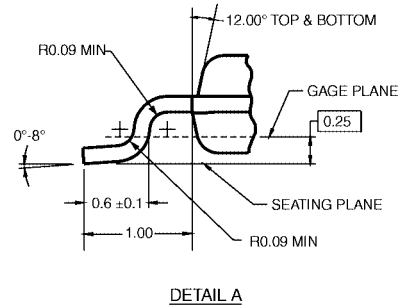
NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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