



January 2001
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74LCX32373 Low Voltage 32-Bit Transparent Latch with 5V Tolerant Inputs and Outputs (Preliminary)

General Description

The LCX32373 contains thirty-two non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the outputs are in a high impedance state.

The LCX32373 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX32373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 5.4 ns t_{PD} max ($V_{CC} = 3.3V$), 20 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

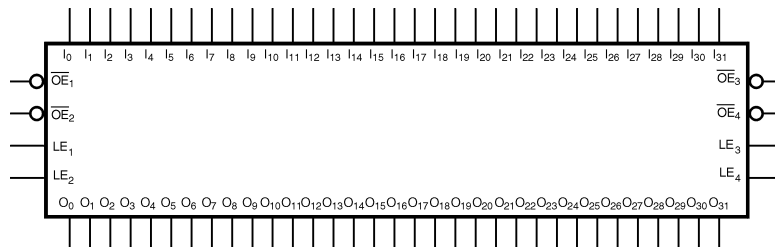
Note 1: To ensure the high-impedance state during power up or down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74LCX32373GX (Note 2)	BGA96A (Preliminary)	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]

Note 2: BGA package available in Tape and Reel only.

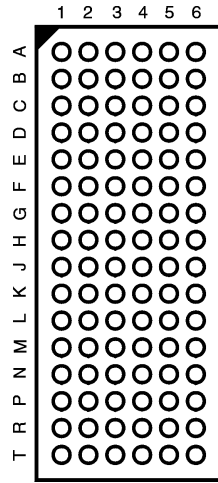
Logic Symbol



74LCX32373 Low Voltage 32-Bit Transparent Latch with 5V Tolerant Inputs and Outputs (Preliminary)

74LCX32373

Connection Diagram



(Top Thru View)

Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
LE_n	Latch Enable Input
$I_0 - I_{31}$	Inputs
$O_0 - O_{31}$	Outputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_1	O_0	\overline{OE}_1	LE_1	I_0	I_1
B	O_3	O_2	GND	GND	I_2	I_3
C	O_5	O_4	V_{CC}	V_{CC}	I_4	I_5
D	O_7	O_6	GND	GND	I_6	I_7
E	O_9	O_8	GND	GND	I_8	I_9
F	O_{11}	O_{10}	V_{CC}	V_{CC}	I_{10}	I_{11}
G	O_{13}	O_{12}	GND	GND	I_{12}	I_{13}
H	O_{14}	O_{15}	\overline{OE}_2	LE_2	I_{15}	I_{14}
J	O_{17}	O_{16}	\overline{OE}_3	LE_3	I_{16}	I_{17}
K	O_{19}	O_{18}	GND	GND	I_{18}	I_{19}
L	O_{21}	O_{20}	V_{CC}	V_{CC}	I_{20}	I_{21}
M	O_{23}	O_{22}	GND	GND	I_{22}	I_{23}
N	O_{25}	O_{24}	GND	GND	I_{24}	I_{25}
P	O_{27}	O_{26}	V_{CC}	V_{CC}	I_{26}	I_{27}
R	O_{29}	O_{28}	GND	GND	I_{28}	I_{29}
T	O_{30}	O_{31}	\overline{OE}_4	LE_4	I_{31}	I_{30}

Truth Table

Inputs			Outputs
LE_n	\overline{OE}_n	I_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

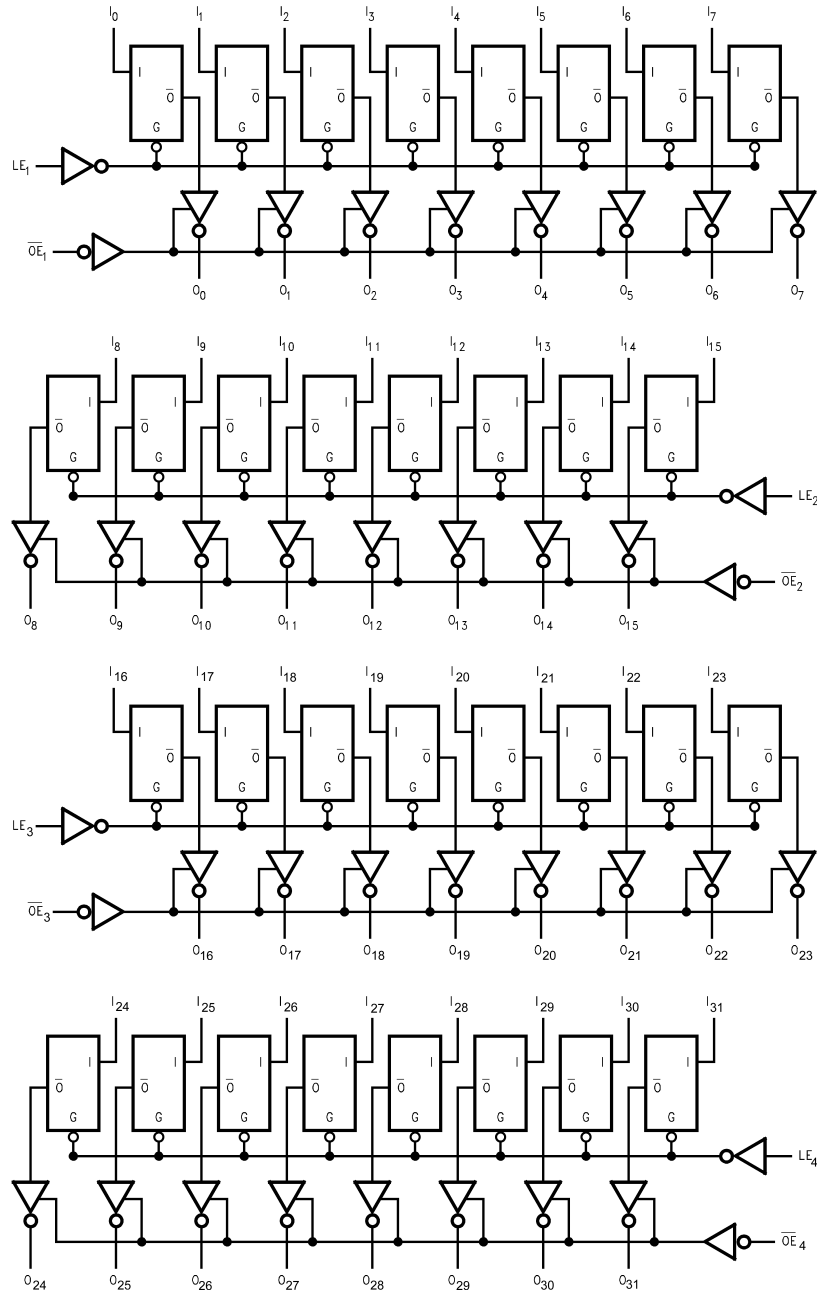
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Functional Description

The LCX32373 contains thirty-two D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 32-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the I_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time

its I input changes. When LE_n is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition of LE_n . The 3-STATE standard outputs are controlled by the Output Enable (\overline{OE}_n) input. When \overline{OE}_n is LOW, the standard outputs are in the 2-state mode. When \overline{OE}_n is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 3)					
Symbol	Parameter	Value	Conditions	Units	
V_{CC}	Supply Voltage	-0.5 to +7.0		V	
V_I	DC Input Voltage	-0.5 to +7.0		V	
V_O	DC Output Voltage	-0.5 to +7.0 -0.5 to $V_{CC} + 0.5$	Output in 3-STATE Output in HIGH or LOW State (Note 4)	V	
I_{IK}	DC Input Diode Current	-50	$V_I < \text{GND}$	mA	
I_{OK}	DC Output Diode Current	-50 +50	$V_O < \text{GND}$ $V_O > V_{CC}$	mA	
I_O	DC Output Source/Sink Current	± 50		mA	
I_{CC}	DC Supply Current per Supply Pin	± 100		mA	
I_{GND}	DC Ground Current per Ground Pin	± 100		mA	
T_{STG}	Storage Temperature	-65 to +150		°C	

Recommended Operating Conditions (Note 5)					
Symbol	Parameter	Min	Max	Units	
V_{CC}	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V_I	Input Voltage	0	5.5	V	
V_O	Output Voltage	HIGH or LOW State 3-STATE	0 0	V_{CC} 5.5	V
I_{OH}/I_{OL}	Output Current	$V_{CC} = 3.0V - 3.6V$ $V_{CC} = 2.7V - 3.0V$ $V_{CC} = 2.3V - 2.7V$		± 24 ± 12 ± 8	mA
T_A	Free-Air Operating Temperature	-40	85	°C	
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$, $V_{CC} = 3.0V$	0	10	ns/V	

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 - 2.7 2.7 - 3.6	1.7 2.0		V
V_{IL}	LOW Level Input Voltage		2.3 - 2.7 2.7 - 3.6		0.7 0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu\text{A}$ $I_{OH} = 8 \text{ mA}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$	2.3 - 3.6 2.3 2.7 3.0 3.0	$V_{CC} - 0.2$ 1.8 2.2 2.4 2.2		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu\text{A}$ $I_{OL} = 8 \text{ mA}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 16 \text{ mA}$ $I_{OL} = 24 \text{ mA}$	2.3 - 3.6 2.3 2.7 3.0 3.0	0.2 0.6 0.4 0.4 0.55		V
I_I	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.3 - 3.6		± 5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.3 - 3.6		± 5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or $V_O = 5.5V$	0		10	μA

DC Electrical Characteristics (Continued)								
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units		
				Min	Max			
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3 – 3.6		20	μA		
		3.6V ≤ V _I , V _O ≤ 5.5V (Note 6)	2.3 – 3.6		±20			
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.3 – 3.6		500	μA		
Note 6: Outputs disabled or 3-STATE only.								
AC Electrical Characteristics								
Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		
		C _L = 50 pF		C _L = 50 pF		C _L = 30 pF		
		Min	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay	1.5	5.4	1.5	5.9	1.5	6.5	ns
t _{PLH}	I _n to O _n	1.5	5.4	1.5	5.9	1.5	6.5	
t _{PHL}	Propagation Delay	1.5	5.5	1.5	6.4	1.5	6.6	ns
t _{PLH}	LE to O _n	1.5	5.5	1.5	6.4	1.5	6.6	
t _{PZL}	Output Enable Time	1.5	6.1	1.5	6.5	1.5	7.9	ns
t _{PZH}		1.5	6.1	1.5	6.5	1.5	7.9	
t _{PLZ}	Output Disable Time	1.5	6.0	1.5	6.3	1.5	7.2	ns
t _{PHZ}		1.5	6.0	1.5	6.3	1.5	7.2	
t _S	Setup Time, I _n to LE	2.5		2.5		3.0		ns
t _H	Hold Time, I _n to LE	1.5		1.5		2.0		ns
t _W	LE Pulse Width	3.0		3.0		3.5		ns
Dynamic Switching Characteristics								
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		Units		
				Typical				
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V			
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	0.6				
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	-0.8	V			
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	-0.6				
Capacitance								
Symbol	Parameter	Conditions	Typical	Units				
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7	pF				
C _{OUT}	Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF				
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC} , f = 10 MHz	20	pF				

AC LOADING and WAVEFORMS Generic for LCX Family

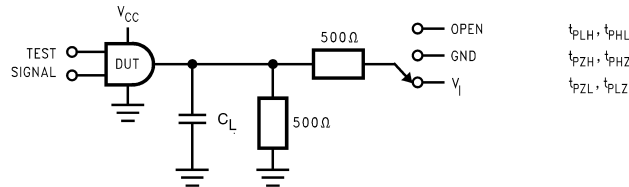
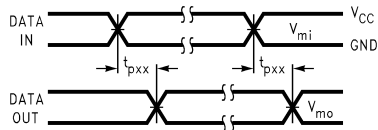
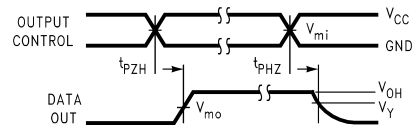


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

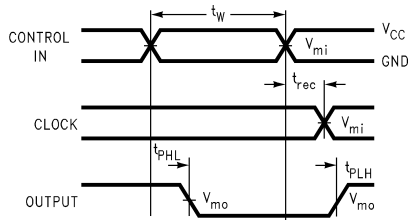
Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$, and 2.7V $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH} , t_{PHZ}	GND



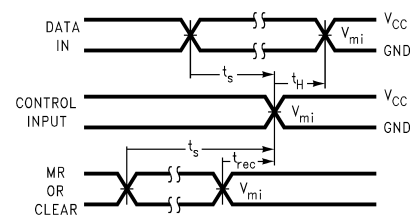
Waveform for Inverting and Non-Inverting Functions



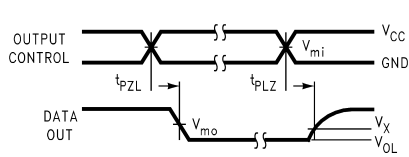
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay, Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

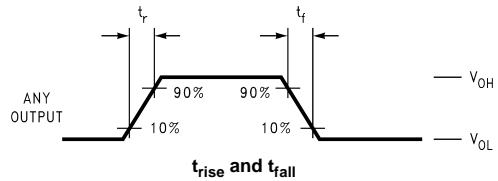


FIGURE 2. Waveforms
(Input Characteristics; $f = 1MHz$, $t_r = t_f = 3ns$)

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	2.7V	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram Generic for LCX Family

